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A Novel Converter for Voltage Balance in Series-Connected Capacitors and Batteries

Research Article

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Abstract: This paper presents a novel concept of a circuit for voltage balance of three series-connected capacitors or batteries, as well as the research results. The problem is related to the control of voltage sharing on series capacitors, supercapacitors or battery banks in energy storage systems or direct current (DC)-link of four-level neutral–point-clamped inverters. The proposed circuit is a switched-capacitor (SC) resonant converter composed of a single capacitor and seven transistor switches. Control of the converter makes it possible to transfer energy between any capacitors, by switching selected transistors. This paper presents the basic concept of the converter, an analysis of control strategies and the simulation results for various cases of voltage balancing.

Keywords: *Capacitor voltage balance • Multilevel converter • NPC four-level inverter • Voltage sharing • Supercapacitor • Battery*

I. Introduction

Series-connected capacitors and batteries are used in energy storage systems or multilevel converters. In both cases, the problem of voltage-sharing control between particular devices is very important. In a bank of supercapacitors, voltage equalisation protects capacitors against overvoltage and increases the energy rate of the recharging cycle. In the case of multilevel neutral-point-clamped (NPC) converters, voltage balancing on the direct current (DC)-link capacitors affects the voltage stresses on semiconductor switches and output voltage modulation quality (Boora et al. 2010; Busquets-Monge et al. 2009; Corzine and Majeethia 2000; Corzine et al. 2002; du Toit Mouton 2002; Grigoletto and Pinheiro 2011; Hasegawa and Akagi 2010; Kou and Corzine 2003; Pou et al. 2005; Rojas et al. 1995; Ruderman and Reznikov 2012; Sano and Fujita 2008; Shu et al. 2013; Shukla et al. 2010; Stala 2011, 2013; Strzelecki et al. 2013; Zhang et al. 2016).

In the literature, there are several ideas for voltage sharing on capacitors connected in series. The problem of neutral-point-voltage balancing has been studied in three-level inverters for years and is mainly managed by appropriate control, with the use of redundant switching states that affect the capacitors' current direction; however, other methods, such as those based on natural balancing, are also recognised (du Toit Mouton 2002; Ruderman and Reznikov 2012; Stala 2011, 2013). In the case of four-level or *n*-level NPC inverters, the problem becomes more complicated but also can be solved by suitable modulation (Busquets-Monge et al. 2009; Hasegawa and Akagi 2010; Pou et al. 2005) or by application of auxiliary active circuits (Boora et al. 2010; Corzine and Majeethia 2000; Corzine et al. 2002; Kou and Corzine 2003; Rojas et al. 1995; Sano and Fujita 2008; Shu et al. 2013; Shukla et al. 2010; Strzelecki et al. 2013; Zhang et al. 2016). Switched-capacitor (SC)-based voltage balancing circuits have been presented in a previous study (Sano and Fujita 2008) for five-level inverters with a DC link composed of four series of capacitors. The auxiliary circuit uses two resonant SC circuits and eight switches. An approach to

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voltage balancing in a diode-clamped multilevel inverter capacitor using capacitor-based circuits is also presented in another study (Shu et al. 2013). Various types of auxiliary circuits using a single supplementary capacitor or a single capacitor per cell are analysed in detail by Shu et al. (2013). A converter with a single resonant cell and *n*-level output has also been presented (Zhang et al. 2016).

Switch-mode-based DC–DC circuits can be also introduced for DC-link voltage balancing. Corzine and Majeethia (2000) propose a specific boost converter for four-level inverter DC-link supply and balancing. The converter operates using an input choke and seven switches. In a previous study (Corzine et al. 2002), a four–level buck converter with fewer switches, which can regulate the voltage of the central capacitor, is presented. A DC–DC switch-mode converter suitable for voltage boosting and capacitor voltage regulation in a four-level NPC inverter has also been previously presented (Kou and Corzine 2003). The converter is composed of two chokes and two switches in the introduced crossing topology. In another study (Strzelecki et al. 2013), a three-level dual DC–DC converter is proposed for DC-link voltage balancing for three capacitors in series. A single-inductor boost converter with multiple outputs is presented by Boora et al. (2010) for control of the DC-link voltages of single-phase NPC inverters. Another approach is the use of flying-capacitor-based choppers (Shukla et al. 2010) for DC-link voltage balance in diode-clamped converters.

In the case of banks of energy, equalisation of the voltages on particular devices can be achieved by the use of passive components, but active systems are very attractive due to their high dynamics, low cost and low losses. Examples of switch-mode equalisers can be found in a few studies (Lambert et al. 2016; Li et al. 2016; Uno and Kukita 2014, 2012, 2015; Uno and Tanaka 2012; Xiong et al. 2016; Ye and Cheng 2015).

The proposed circuit makes it possible to control the voltages on devices in a branch of three series-connected capacitors or batteries. The converter is based on a SC resonant circuit and operates in zero current switching (ZCS) mode. The number of semiconductor switches, as well as the volume of LC components, may be preferable to existing solutions using auxiliary circuits for voltage balancing.

The basic concept of operation of the proposed balancer is presented in Section I of the paper. The analysis and simulation results of selected tests are included in the following sections.

II. Operation of the SC balancer

The proposed SC balancer (Figs.1 and 2) makes it possible to transfer the energy between any of the three capacitors in the series branch. The SC can be charged from a single selected capacitor and discharged to another

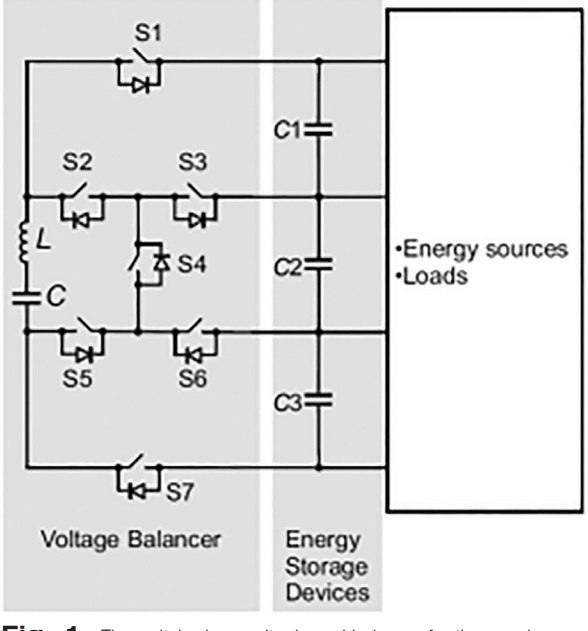


Fig. 1. The switched-capacitor-based balancer for three series-connected capacitors. C_1 to C_3 –series-connected capacitors, S_1 to S_7 – transistor switches, L and C – inductor and capacitor of SC resonant branch

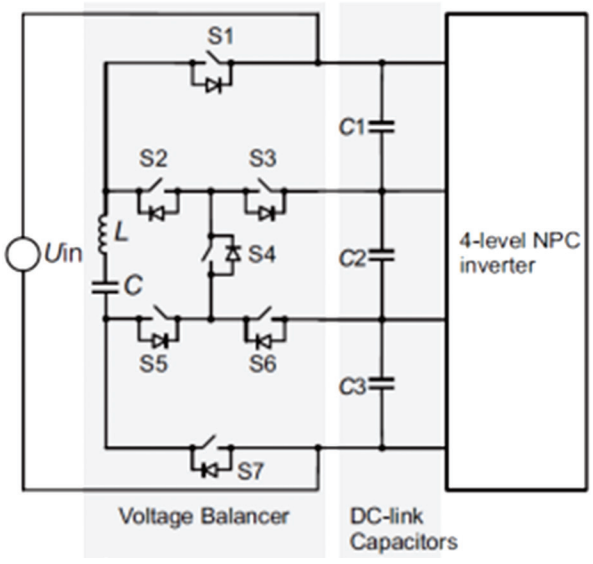


Fig. 2. Application of the switched-capacitor-based balancer for voltage sharing in the DC-link capacitor in the input of a four-level NPC inverter. U_{in} – DC power supply

(Figs. 3–5). In such cases, the energy is transferred, provided that the voltage on the discharged capacitor exceeds the voltage on the charged one. This strategy is sufficient to maintain the equal voltage sharing on the capacitors in the series branch. To increase the rate of energy transfer, the SC can be charged from two or three capacitors and discharged to the selected one (Fig. 6).

Charging and discharging of the SC occurs in the oscillatory LC circuit with the i_{SI} charging current and i_{SII} discharging current being related as follows:

$$i_{SI}(t) = \frac{u_{CD} - u_{Cmin}}{\rho} \sin\omega t = I_{SIm} \sin\omega t; \tag{1}$$

$$i_{SII}(t) = \frac{u_{Cmax} - u_{CC}}{\rho} \sin\omega t = I_{SIIm} \sin\omega t, \tag{2}$$

with the characteristic impedance and the angular resonant frequency given by the following equation:

$$\rho = \omega L = \sqrt{L/C}; \; \omega = \sqrt{1/(LC)}, \tag{3}$$

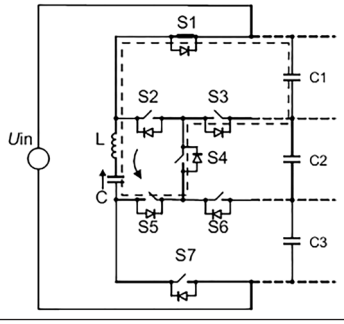
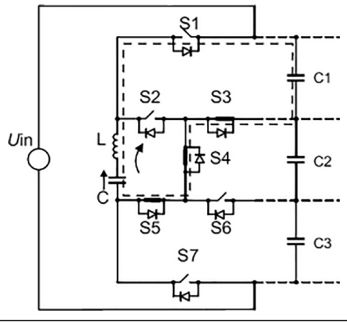
A case of operation		Voltage stress on switches
C_1 discharging	C_1 charging	
		$u_{S6} = u_{C2}$ $u_{S7} = u_{C2} + u_{C3}$ $u_{S2} = u_C$ ($<2u_{in}/3$)

Fig. 3. Charging and discharging the capacitor C_1. Control of the switches and operational conditions

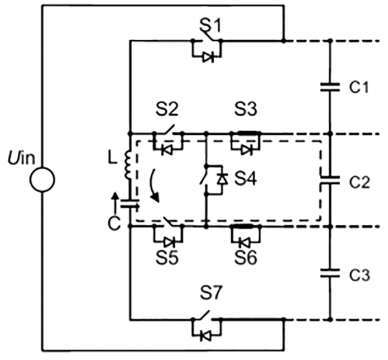
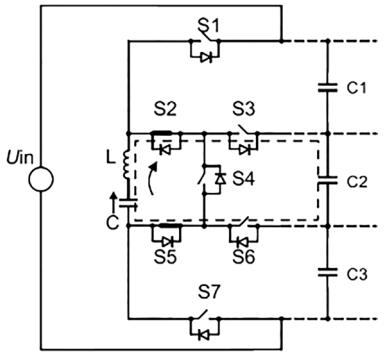
A case of operation		Voltage stress on switches
C_2 discharging	C_2 charging	
		$u_{S1} = u_{C1}$ $u_{S7} = u_{C3}$ $u_{S4} = u_C$ ($<2u_{in}/3$)

Fig. 4. Charging and discharging the capacitor C_2. Control of the switches and operational conditions

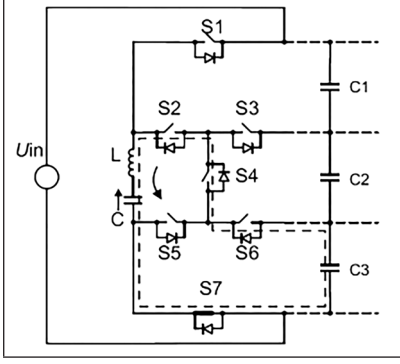
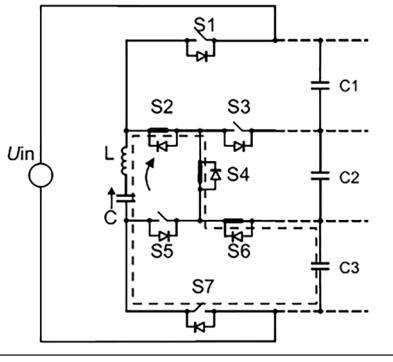
A case of operation		Voltage stress on switches
C_3 discharging	C_3 charging	
		$u_{S1} = u_{C1} + u_{C2}$ $u_{S3} = u_{C2}$ $u_{S5} = u_C$ ($<2u_{in}/3$)

Fig. 5. Charging and discharging the capacitor C_3. Control of the switches and operational conditions

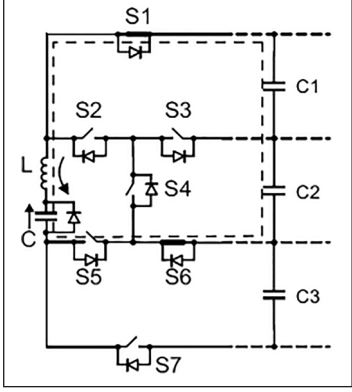
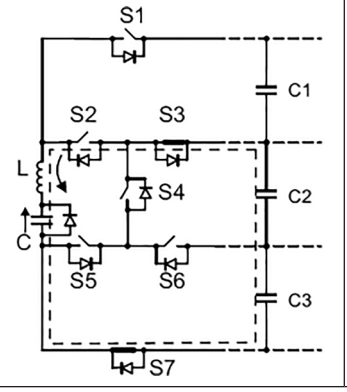
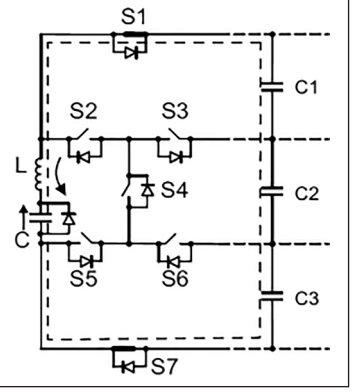
A case of operation		
Switched capacitor charging from C_1 and C_2	Switched capacitor charging from C_2 and C_3	Switched capacitor charging from C_1, C_2, C_3
		

Fig. 6. Switching states for charging the switched capacitor in two and three series-connected capacitors

where u_{CD} is the voltage on a discharged capacitor in the series branch, u_{CC} is the voltage on a charged capacitor in the series branch, u_{Cmin} and u_{Cmax} are the voltages on the SC (minimum and maximum, respectively), L is the inductance of the resonant circuit and $I_{SIm,}$ I_{SIIm} are the amplitudes of the current.

The voltages across the SCs during the charging (u_{CSI}) and discharging (u_{CSII}) cycles are given by the following equations:

$$u_{CSI}(t) = u_{CD} - \left(u_{CD} + u_{Cmin}\right)\cos\omega t \tag{4}$$

$$u_{CSI}\left(T_{SI}\right) = u_{Cmax} = 2u_{CD} - u_{Cmin} \tag{5}$$

$$u_{CSII}(t) = u_{CC} + \left(u_{Cmax} - u_{CC}\right)\cos\omega t \tag{6}$$

$$u_{CSII}\left(T_{SII}\right) = u_{Cmin} = 2u_{CC} - u_{Cmax}. \tag{7}$$

The energy transferred reaches its maximum value when the voltage of the SCs decreases to zero during the discharging period:

$$u_{Cmin} = 0;\ u_{Cmax} = 2u_{CD}. \tag{8}$$

Then, the energy W drained from a discharged capacitor to charge a SC is given by the following equation:

$$W = \frac{1}{2}Cu_{Cmax}^2 = 2Cu_{CD}^2. \tag{9}$$

The balancing process can be complicated and can vary depending on the operational stage. When the SC is fully discharging and charging from nearly the same voltage during particular periods (long-term balancing process), the balanced capacitor voltage can be approximated by a linear function, because in each switching period, the same amount of energy is transferred to the balanced capacitors from the SC. It can occur when the SC is charging from three capacitors and further discharging to a given device. Of course, the dynamics change when the selection of the recharging capacitors varies, which should be controlled accordingly. An exponential term of voltage can be observed when the SC is not fully discharging.

The time constants for the charging process depend on three components: the dynamics of the current rise in the SC branch, the time constant for the series capacitor discharging, the capacitances of the series capacitors and their initial conditions.

When the capacitors remain unbalanced during the balancing process, the voltages across the SC after the charging and discharging stages are the following:

$$U_{Cmax}(n-1) = 2U_{CD}(n-2) - U_{Cmin}(n-2) \tag{10}$$

$$\begin{aligned} U_{Cmin}(n) &= 2U_{CC}(n-1) - U_{Cmax}(n-1) = \\ &= 2U_{CC}(n-1) - 2U_{CD}(n-2) + U_{Cmin}(n-2), \end{aligned} \tag{11}$$

where n denotes a given switching period.

When $U_{CD}(n-1) > U_{CC}(n-2)$, the minimum voltage on the SC decreases until it reaches 0 V (negative voltages can be reduced by the parallel diode on the SC). The dynamics of this process depend on the switching frequency and the characteristic impedance on the resonant SC circuit (Waradzyn et al. 2017).

When the SC is fully discharging in each switching period, the dynamics of the balancing process can be further predicted on the basis of the switching frequency, the amount of energy transferred in each switching period between capacitors and the capacitances of the capacitors in the controlled branch.

III. Simulation results

Simulations of the proposed SC balancer were performed to demonstrate its operation under particular circumstances, the dynamics of the balancing process and the voltage stresses on semiconductor switches. During the basic tests, all the conditions are simulated in open-loop control by switching the appropriate transistors. Figures 7a–7c present data for the following instances: energy transfer from C_1 to C_2 (Fig. 7a), energy transfer from C_1 to C_3 (Fig. 7b) and energy transfer from C_2 to C_3 (Fig. 7c).

In order to validate the operation, the following signals are measured and viewed: voltages on the series capacitors (u_{C1}, u_{C2}, u_{C3}), voltage on the SC (u_{Cbal}), control signals to switches ($ctrl_1$, $ctrl_2$), voltage stresses of semiconductor switches ($u_{SW1}\ldots u_{SW7}$) and the current through the SC (i_{Cbal}). Parameters for the components used in the simulation tests are presented in Table 1.

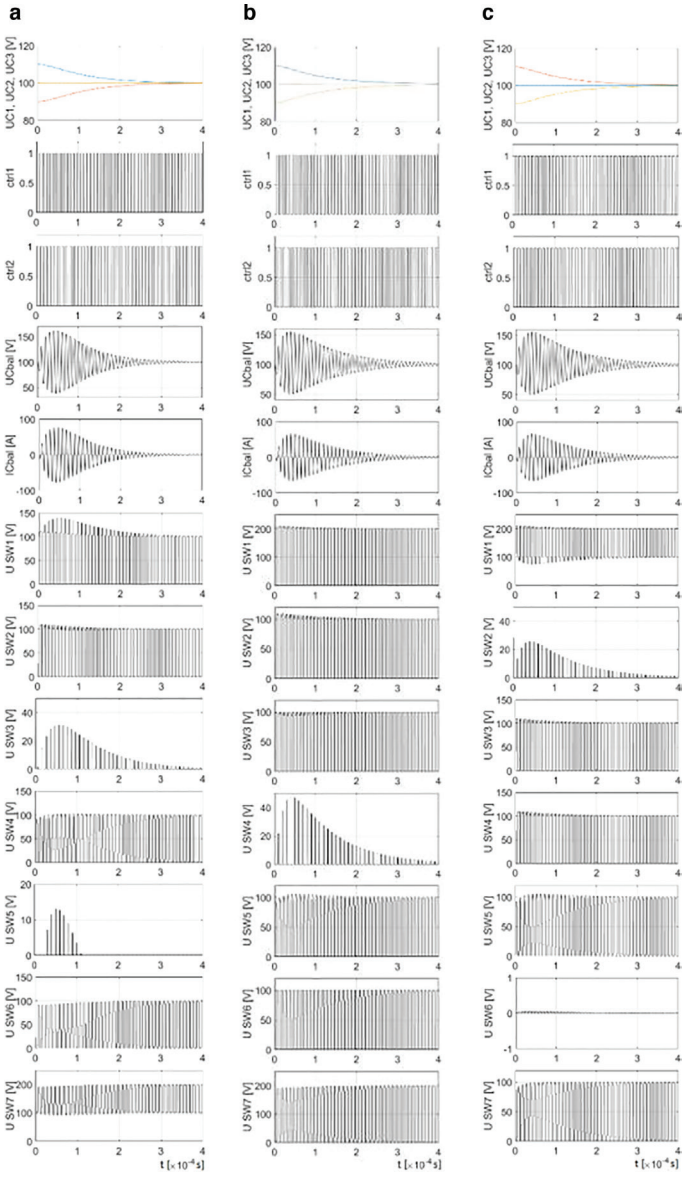


Fig. 7. Energy transfer between capacitors in the branch, with the association of the switched capacitor. Waveforms of voltages on the series capacitors (u_{C1}, u_{C2}, u_{C3}); voltage and current on the balancing capacitor (u_{Cbal}, i_{Cbal}); control signals ($ctrl_1$, $ctrl_2$); voltage stress on switches ($u_{SW1}\ldots u_{SW7}$). Test cases: $u_{C2}(0) = 100\text{V}$, $u_{C3}(0) = 90\text{V}$, $u_{C1}(0) = 110\text{V}$ – energy transfer from C_1 to C_2 (a); $u_{C2}(0) = 100\text{V}$, $u_{C3}(0) = 90\text{V}$, $u_{C1}(0) = 110\text{V}$ – energy transfer from C_1 to C_3 (b); $u_{C2}(0) = 100\text{V}$, $u_{C3}(0) = 90\text{V}$, $u_{C1}(0) = 110\text{V}$ – energy transfer from C_2 to C_3 (c). MATLAB/Simulink results

Table 1. Parameters used for simulation of the balancer

$C1$, $C2$, $C3$	C	L	f_S
208.7 µF	1.3 µF	800 nH	100 kHz

From the results presented in Fig. 7, it follows that:

- Voltages on output capacitors were successfully balanced
- Stresses on switches in the worst case slightly exceed 200 V, which is double the desired balanced value
- Number of active switches (various for different cases) marginally influences balancing time due to their low resistance

The dynamics of the balancing process for various initial voltages are presented in Figs. 8a and 8b, where both the LC branch values and frequencies are maintained constant. By varying the parameters associated with the balancing LC branch, circuit dynamics can be influenced. Two different SC values are simulated, in which the capacitance differs by a factor close to four. Results are presented in Figs. 9a and 9b.

In the proposed balancer, a clamping diode in parallel to the capacitor is introduced, to protect the capacitor against negative values of voltage. Thus, the dynamic of the balancing process is limited by the rate of energy stored in a capacitor charged from 0 V at a given frequency. The clamping diode is also necessary from the protection standpoint. During unbalanced conditions, the discharge and charge of the SC tends to increase in subsequent periods. The clamping diode limits this process and protects the circuit against overvoltage.

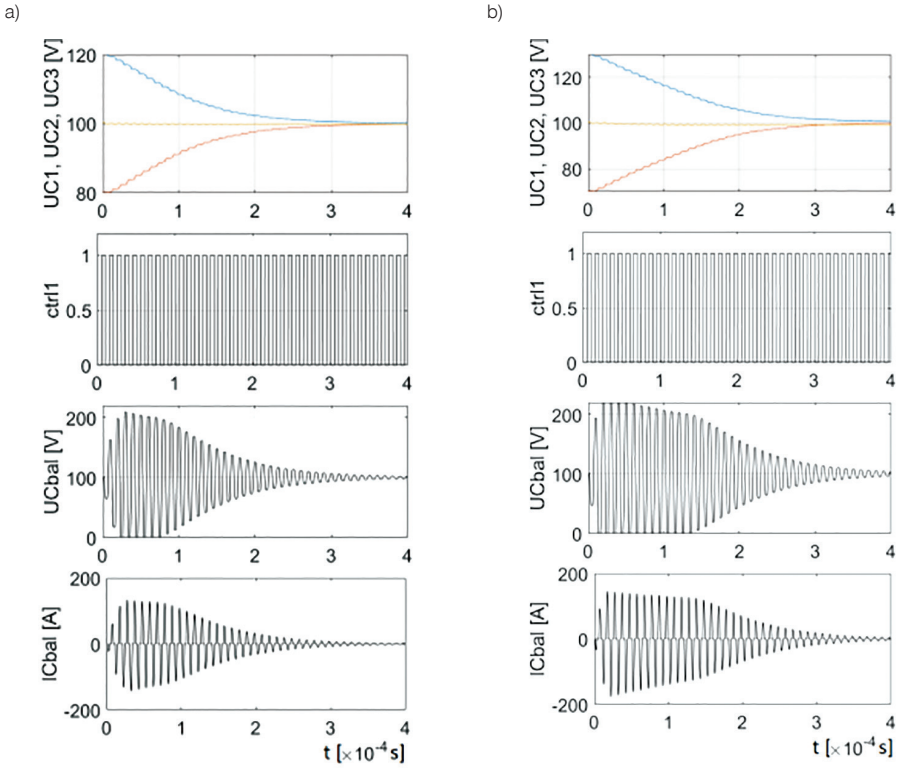


Fig. 8. The impact of initial voltages across series capacitors on the dynamics of the balancing process. Waveforms of voltages on series capacitors (u_{C1}, u_{C2}, u_{C3}); the voltage and current on the balancing capacitor (u_{Cbal}, i_{Cbal}); control signal ($ctrl_1$). Test cases: $u_{C1}(0) = 120$V, $u_{C2}(0) = 80$V, $u_{C3}(0) = 100$V – energy transfer from C_1 to C_2 (a); $u_{C1}(0) = 130$V, $u_{C3}(0) = 70$V, $u_{C2}(0) = 100$V – energy transfer from C_1 to C_2 (b). MATLAB/Simulink results

As stated in Section II, a high rate of energy transfer is possible when two or three capacitors are drained at a time. A simulation of such cases was conducted, and the results are presented in Fig. 10. The results are proof of concept only, because these cases require development of more advanced control systems and further investigation

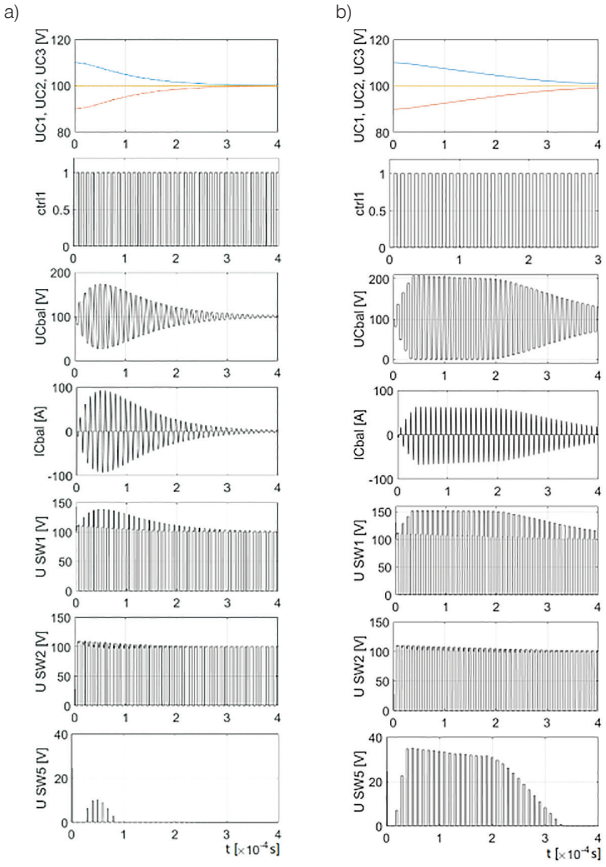


Fig. 9. The impact of switched capacitance on the dynamics of the balancing process. An operation with constant switching frequency for two different capacitance values: 0.3 μF (a) and 1.3 μF (b). Waveforms of voltages on series capacitors (u_{C1}, u_{C2}, u_{C3}), where $u_{C2}(0) = 100\text{V}$, $u_{C3}(0) = 90\text{V}$, $u_{C1}(0) = 110\text{V}$); voltage and current on the balancing capacitor (u_{Cbal}, i_{Cbal}); control signal ($ctrl_1$); voltage stress on the active switches (u_{SW1}, u_{SW2}, u_{SW5}) MATLAB/Simulink results

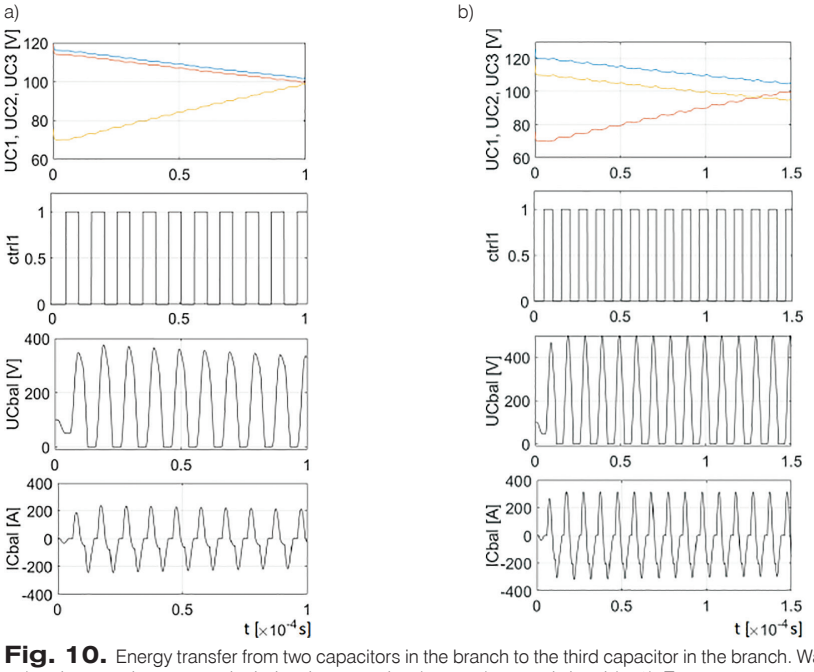


Fig. 10. Energy transfer from two capacitors in the branch to the third capacitor in the branch. Waveforms of voltages on series capacitors (u_{C1}, u_{C2}, u_{C3}); voltage and current on the balancing capacitor (u_{Cbal}, i_{Cbal}); control signal ($ctrl_1$). Test cases: $u_{C1}(0) = 116\text{V}$, $u_{C2}(0) = 114\text{V}$, $u_{C3}(0) = 70\text{V}$ – energy transfer from C_1 and C_2 to C_3 (a); $u_{C1}(0) = 120\text{V}$, $u_{C3}(0) = 110\text{V}$, $u_{C2}(0) = 90\text{V}$ – energy transfer from C_1 and C_3 to C_2 (b). MATLAB/Simulink results

into how capacitor voltage can be fully balanced. The charging of the SC from the two or three capacitors may be used to increase the dynamics of the balancing process, but it may not be able to reach the balanced state. Thus, the precise exchange of energy between single capacitors may be used in the final stage of the balancing process. The results (Fig. 10) show that the rate of change of voltage on discharging capacitors is two times lower than the voltage increase on the charging capacitor. Such a mode of operation can be selected in cases where a single capacitor is fully discharged and requires swift balancing.

IV. Conclusions and next steps

The proposed balancer topology was shown to work as expected. Energy is transferred via a balancing branch between selected capacitors in the output bank, causing their voltages to equalise. The magnitude of the energy can be adjusted by tuning the balancing LC branch and changing the switching frequency of the semiconductors. Simple circuit protection can be introduced by adding a clamping diode parallel to the balancing capacitor. Such a setup limits the circuit dynamics and protects against overvoltage stresses. In addition, a rapid energy handover is possible by charging the balancing capacitor from two or three bank capacitors at a time and returning energy to the capacitor with the lowest voltage. The disadvantage of the proposed circuit is voltage stress on switches, which can reach the sum of the voltages of the two series-connected capacitors.

In future work, the authors would like to build a real circuit and perform a number of tests to compare the circuit operation with the simulation results. Investigations would be also be focused on the selection of the technology for semiconductor switches, dynamics and efficiency analysis and a comparison with other solutions, as well as the development of a closed control loop to secure proper operation in practical applications.

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