

# A Method for ADC Error Testing and its Compensation in Ratiometric Measurements

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Errors induced due to ratiometric measurements are discussed and a simplified compensation method to reduce the various static errors of ADC, voltage reference errors in ratiometry and resistance mismatch errors is proposed. Curve fitting is done for the error samples and the system is modelled in comparison to an ideal system. Static errors and other ratiometric errors, thus modelled are derived into a corrective equation in comparison with an errorless system. Implementation of the proposed method is discussed for a resistance measurement system and analyzed. This paper also discusses the usage of the proposed system with successive approximation ADCs for ratiometric measurement operations against the conventional requirement dual slope ADCs for the same.

**Keywords:** Ratio-metric Measurements, Curve Fitting, ADC Error Testing, Error Compensation

## 1. INTRODUCTION

### 1.1. Ratiometric Conversion for measurement

**R**ATIOMETRIC OPERATION uses the reference voltage that is used for the ADC to drive the signal source in such way that the ratio of the output of that signal source to the reference is independent of the reference voltage [5]. Ratiometric measurements are chosen to avoid conditions where in a variable resistance causes a non-linear response of the voltage input to voltage reference ratio. This is further explained as per Fig.1. Measurement systems invariably use dual slope ADCs as they require ratiometric conversion of the reference voltage.

### 1.2. Effect of voltage reference on ADC performance

The digital output of the ADC is given by

$$D_{out}(ideal) = (A) \times \frac{2^n}{V_{REF}} \quad (1)$$

where,  $A = V_{IN} \pm V_X$  and  $-\frac{1}{2}V_{LSB} \leq V_X < \frac{1}{2}V_{LSB}$

$V_X$  is the normalization voltage to nullify the error due to quantization for the purpose of ideal modeling.

The DC errors of non-ideal ADC are offset voltage error and gain error. The effective  $D_{out}$  may be given from [1] as,

$$D_{out} = (A \pm V_L) \times \frac{2^n}{V_{REF}(1 - GE_{ADC})} \quad (2)$$

$V_L$  is the linearity error voltage of the ADC and varies for each code value, and  $GE_{ADC}$  is the gain error which is the ratio of gain difference between actual gain and ideal gain to the value of the actual gain. Also,  $V_L$  for the first code is the offset error of the ADC. Hence, there is need for error compensation in ratiometric operations when high degree of accuracy is required for measurements. Overall noise due to static errors is not constant but it is dependent on the changes in reference

voltage to input voltage ratio [8]. Thus, such inconsistencies are to be addressed in ratiometric measurement systems.

## 2. METHOD FOR STATIC ERROR MEASUREMENT

### 2.1 Principle of the proposed method

The proposed method maintains implicit estimation of the static errors through a training sequence which is similar to the ramp used in the histogram method and through a curve fitting operation on the samples, a corrective equation is determined.

(1) can be rewritten as

$$D_{out} = A \left( 1 \pm \frac{V_L}{A} \right) \times \frac{2^n}{V_{REF}(1 - GE_{ADC})} \quad (5)$$

From (1) and (5), 
$$\frac{D_{out}(actual)}{D_{out}(ideal)} = y_i \quad (6)$$

Where the required error estimate is  $y_i = \frac{\left( 1 - \frac{V_L}{V_{IN}} \right)}{(1 - GE_{ADC})}$  and

desired to be equal to 1.

## 3. SIGNAL CONDITIONING CIRCUIT

### 3.1 Requirement for signal conditioning

A ratiometric measurement system normally using a dual slope ADC is modelled by the following figure:

The  $D_{OUT}$  for an ADC can be given as,

$$D_{out} = \frac{V_{in+} - V_{in-}}{V_{ref+} - V_{ref-}} \times 2^n \quad (7)$$

Wherein,  $V_{REF+}$  and  $V_{REF-}$  are required. The same case with a successive approximation ADC will require  $V_{REF}$  to be varied as a function of  $V_{IN}$  since,

$$V_{IN} = V_S - V_{REF}$$

Manual variation of the resistance across  $V_{IN}$  is a complex process in real time. Hence a conditioning circuit is proposed to directly convert the input signal to required reference. The proposed circuit maintains the required 180 degree phase difference between the signals applied at  $V_{IN}$  and  $V_{REF}$ . A ramp as test stimuli are generated for measuring the errors.

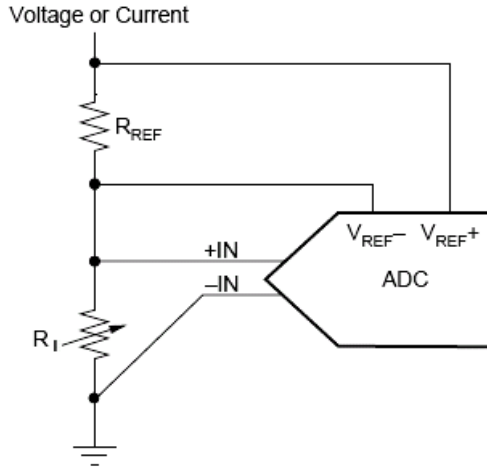


Fig.1 Single-ended system for conversion to ratiometric resistance

### 3.2. Conditioning circuit

Ratiometric operation is implemented by means of an inverting instrumentation amplifier and an adder circuitry, thus making the ratio of  $V_{IN}$  to  $V_{REF}$  a linear one.

The following circuit also implements the test stimuli generation for the error measurement, and a switch may connect it to the external element to be measured in real time. Here, linearity of the signal is stable through the amplifier since the frequency of the test signal to measure the static errors is too small to induce slew rate effects. Thus, the amplifier may be considered as an ideal one.

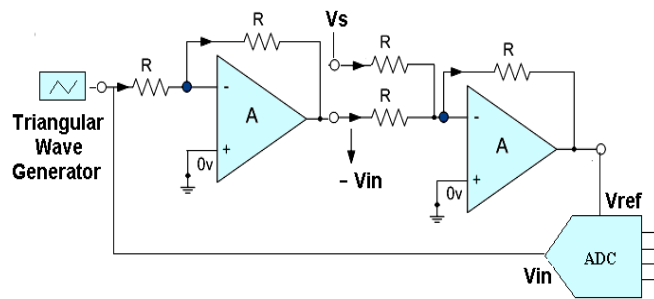


Fig.2 Ratiometric signal conditioning circuit

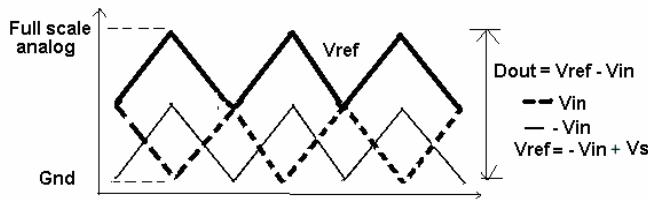


Fig.3  $V_{REF}$  and  $V_{IN}$  generated from circuit in Fig.2

The circuit eliminates the requirement for a  $V_{REF}$  and hence, through this, measurement can be done with a successive approximation ADC as well.

An ideal case signal is required for the initial error measurement. This can be a triangular wave-form which is used to drive both source and  $V_{REF}$ .

## 4. STATIC ERROR COMPENSATION

### 4.1. Post Error compensation

A simple method of ADC error correction is followed by determining the ADC codes for a known ideal case of linearly varying inputs such that the output plot may be predicted through theoretical calculation. An external system may learn the DC error for the ADC through the ideal training sequence and hence apply a linear external corrective estimate. Post correction enables fast ADCs with modest linearity [4].

In [2]-[3], dynamic behaviour models for INL were proposed. Both papers also suggest that the two components can be corrected separately, with different methods. In [2], one component is corrected by a LUT and the second component by using dithering. The dithering technique requires over-sampling. Consequently, this method is not viable in combination with under-sampling. The dynamics in [3] is represented in the model by using slope information from the input signal, which requires a more extensive LUT and a more complex characterization of the ADC.

### 4.2. Simplified solution to post correction

The implementation provided makes use of the Least Mean Square Error to determine the amount of fault in the ADC and then applies curve fitting to determine the correction required for the sampled points. This corrective equation is then used as the base for real time conversion, thus providing an accurate output for the estimate values.

This corrective mechanism can be fabricated on chip with the ADC to effectively minimize DC errors.

Samples taken from the readings obtained may be simplified as a second order equation of the form  $y = a_0 + a_1x + a_2x^2$ . The equation is obtained from the Least Mean Square method,

$$\begin{pmatrix} n & \sum x_i & \sum x_i^2 \\ \sum x_i & \sum x_i^2 & \sum x_i^3 \\ \sum x_i^2 & \sum x_i^3 & \sum x_i^4 \end{pmatrix} \begin{pmatrix} a_0 \\ a_1 \\ a_2 \end{pmatrix} = \begin{pmatrix} \sum y_i \\ \sum x_i y_i \\ \sum x_i^2 y_i \end{pmatrix} \quad (8)$$

Where  $y_i$  is the correction factor as stated in (6) and  $x_i$  is the measured  $V_{IN}$ ;  $n$  is the number of samples acquired. Thus the entire operation may be stored in a micro kernel implementation in the ADC to learn from test ramp signal and predetermined outputs and hence apply corrections to the measured values. This is also advantageous over LUT methods when implementation is done for BIST systems, since this method requires minimal permanent memory storage.

## 5. IMPLEMENTATION IN RESISTANCE MEASUREMENT

## 5.1. Designed prototype description

An implementation of a ratiometric measurement system is done. A data logger based on a micro computer was built to acquire and store resistances measured from different materials[7].

The equipment stores data into an on-board I2C and can be connected to the PC by means of serial communication and hence the data may be uploaded onto the PC.

The proposed circuit was introduced to interface the resistance to the ADC and a MUX was used to switch to the corresponding resistance range as required. A multiplexer circuit is used to switch between the different values of known resistances so that  $V_{REF} \leq V_{IN}$  condition may be avoided. The MUX is controlled by the micro-controller that measures  $D_{OUT}$  from the ADC. Through this, resolution of the ADC is maintained.

The system logs and displays resistance data in real time and also has the provision of being connected to the PC. Stability in measurement is achieved by code polling and by low pass filtering across the ADC.

When an unknown resistance  $R_i$  is connected against a known value of resistance  $R_x$  as shown in Fig.3, and the input is given to an ADC of  $n$  bits, then the digital output may be related to the  $V_{in}$  and  $V_{ref}$  voltages.

The equation from (1) may be simplified to bring its relation directly to resistance as follows,

$$D_{out} = \frac{I(R)}{I(R_x)} \times (2^n - 1) ; D_{out} = \frac{R_i}{R_x} \times (2^n - 1)$$

E.g., when  $n = 12$ ,  $2^n = 4096$ . Thus if  $R_x = 4095 \Omega$ ,  $D_{OUT} = R_i$

But it is required that  $V_{REF} \geq V_{IN}$  for the ADC, thus it is required that  $R_x \geq R_i$ . For this reason we need to go for a multiplexed system. The circuit in Fig.3 can measure resistances up to  $4M\Omega$ . C0 and C1 are control lines for control by the CPU.

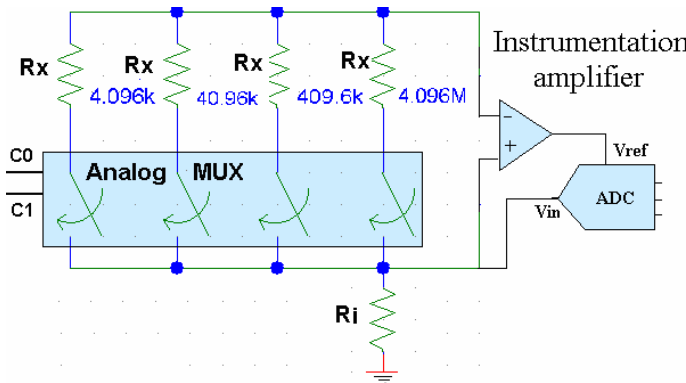


Fig.3 Resistance range circuit

## 5.2. Real time testing and enhancement

During implementation, a chief problem that occurred was the additional dynamic resistance introduced by the MUX due to varying current across the resistors.

This complication results in the actual  $R$  being deterred by an additional factor resulting in an  $R$  value less than the original intended value.

$$D_{out} = \frac{R_i}{R_x + R_{switch}} \times (2^n - 1) \quad (9)$$

Here,  $R/T_{bar}$  is the select line that switches in between the Test circuit and the Resistance measurement circuit. The linear correction circuit can be used for a second set of training data in order to bring into consideration the errors due to the external circuitry.

Thus, by knowing the correct resistance required and determining the correction factor, a curve fit equation was devised based on the finite set of data samples, and this implemented an adaptive ADC that could ensure accurate measurement and conversion of the analog voltage.

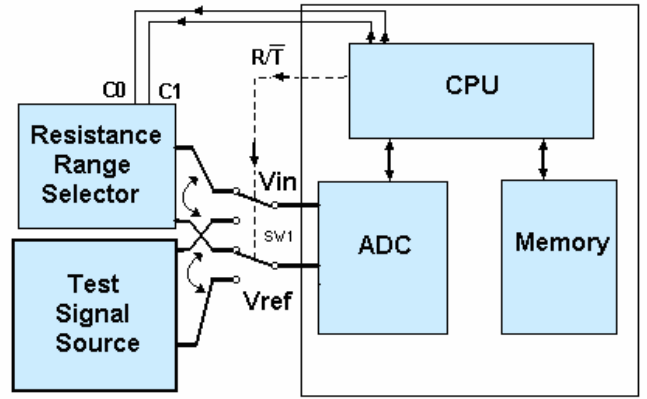


Fig.4 Proposed system implementation

Testing was done using the data logger system and was found effective, the accuracy obtained despite faulty input values.

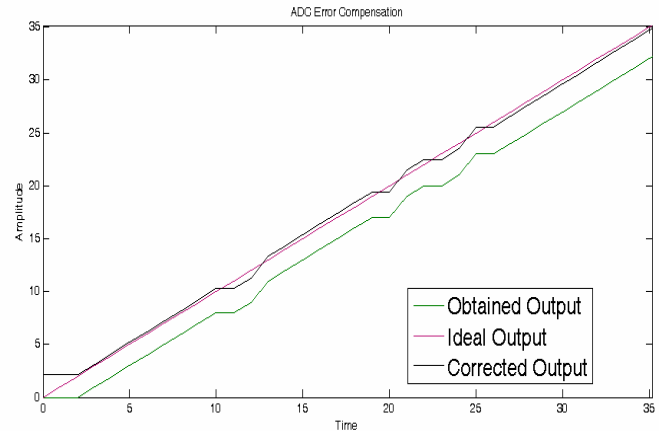


Fig.5 Compensated ADC output

## 6. EXPERIMENTAL RESULTS

The ramp signal of frequency 6 Hz is applied to the ADC MCP3208. A PIC16F877 controller board is used to obtain the digital data from the ADC at a sampling frequency of 48 KHz using SPI protocol. The digital output data is stored in I2C.

A discrete ramp signal of the same frequency (6 Hz) is generated using simulation software with the same sampling frequency (48 KHz). The reference data is obtained from the quantization of the generated discrete samples. A second order curve fitting is performed between the data stored in SDRAM and reference data (in Non-real time) to obtain the coefficients ( $a_0$ ,  $a_1$ ,  $a_2$ ) in (8). It is observed that the 84% of the error is reduced after the 2<sup>nd</sup> order curve fitting. The output plotted with reference to discrete time is shown in Fig.5

## 7. CONCLUSION

We presented a method to reduce ADC static errors and voltage reference errors existing in ratiometric measurements. We obtained real time data from the ADC and curve fitting was done to reduce the errors. Once the coefficients are obtained, they can be used to compensate the errors during real time measurements.

When compared to histogram based methods, this method requires low amount real time data for processing; hence speed and efficiency are increased. The order of the curve fitting equation can be increased to reduce the error further. In this method external error can also be compensated once the ADC is completely modelled. Unlike other methods, this

method provides overall compensation for the ADC static errors in a simple and reliable way.

## REFERENCES

- [1] Bonnie Baker, Miro Oljaca, "How the voltage reference affects ADC performance Texas instruments 'Data acquisition division'".
- [2] L. Michaeli, L. Sochová, and J. Saliga, "ADC look-up table based post correction combined with dithering," in XVIII IMEKO WORLD CONGRESS Rio de Janeiro, Brazil, 2006.
- [3] N. Björzell and P. Händel, "Dynamic behavior models of analog to digital converters aimed for post-correction in wideband applications " in IMEKO World Congress, Rio de Janeiro, Brazil, 2006.
- [4] Niclas Bjorsell and Peter Händel, "Post-Correction of Under-Sampled Analog to Digital Converters" IMTC 2007 Instrumentation and Measurement, Warsaw, Poland, May 1- 3, 2007.
- [5] Russell Anderson, "Understanding Ratio Metric Conversions", Texas Instruments Application Report SBAA110 – March 2004.
- [6] F. Azais, S. Bernard, Y. Bertrand, M. Renovell LIRMM - University of Montpellier II, 'Implement-tation of a Linear Histogram BIST for ADCs'".
- [7] Helfrick, A. D., Cooper, W.D. (1990). Modern Electronic Instrumentation and Measurement Techniques. Englewood Cliffs, USA: Prentice-Hall.
- [8] Miro Oljaca, Baker Bonnie, (2009) "How voltage reference affects ADC performance" Data acquisition, Analog Applications Journal.

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