Materials Science-Poland, 37(2), 2019, pp. 249-256
http://www.materialsscience.pwr.wroc.pl/
DOI: 10.2478/msp-2019-0026

Correlation between surface morphology and potential profile in OFETs with zone-cast TIPS-Pentacene as seen by scanning Kelvin probe microscopy

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Charge-carrier transport in the channel of bottom gate, top contact organic field effect transistors with anisotropic layers of 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-Pentacene) obtained by zone casting was investigated using scanning Kelvin probe microscopy combined with atomic force microscopy. The TIPS-Pentacene continuous layers consisted of thin crystals unidirectionally oriented in the channel. Devices with perpendicular and parallel charge flow in the transistor channel were prepared. It was found that irregularities in the surface morphology at the semiconductor layer in the transistor channel are correlated with the local potential profile, and that the channel resistance strongly depends on the orientation of the TIPS-Pentacene crystals.

Keywords: *organic field effect transistors; scanning Kelvin probe microscopy; zone casting*

1. Introduction

Development of organic electronics observed in recent years was driven mostly by the synthesis of new organic semiconductors with improved physicochemical properties, such as stability, solubility, appropriate HOMO-LUMO levels, etc. Further progress in organic electronic technology requires development of processing techniques that allow producing high performance devices with good reproducibility. It is known that the performance of Organic Field Effect Transistors (OFETs) based on polycrystalline low molecular weight semiconductors depends on the structure of the active layer [1]. Therefore it is important to investigate the correlation between the charge carrier transport and the morphology of the active layer in such devices. The scanning Kelvin probe microscopy technique (SKPM) [2–4] combined with the atomic force microscopy (AFM) [5] offers the possibility to simultaneously monitor the surface potential profiles in the OFET's channel under bias and to correlate them with the surface morphology.

In this contribution, we investigate bottom gate (BG), top contact (TC) OFETs with active channels made of anisotropic layers of 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-Pentacene) obtained by zone-casting technique by means of SKPM and AFM. Zone-casting technique allows us to obtain highly oriented layers of organic semiconductors [6–8]. It was found, that such oriented zone-cast layers show a strong electrical anisotropy of charge carrier mobility in OFET devices. The charge mobility along the zone-casting direction can be more than one order of magnitude higher than in the perpendicular direction [9]. The investigation of anisotropic OFETs based on TIPS-Pentacene semiconductor was published by Park et al. [10]. The anisotropic active layer was obtained by technique consisting in vertical flow of a viscous solution onto the upstanding substrate. The published 2D surface potential map of the TIPS-Pentacene layer illustrates large contrast between crystalline

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regions and regions described by authors as void or amorphous which indicates that the obtained layers were discontinuous. Nevertheless, the charge carrier mobility for the best parallel device was one order of magnitude higher than for the best perpendicular device.

Our investigations were focused on correlation between surface morphology (as seen by AFM), surface potential profile (studied by SKPM) and transistor parameters in OFETs with continuous, unidirectionally oriented TIPS-Pentacene layer obtained by zone-casting.

2. Experimental

The OFET devices were fabricated and investigated in a clean-room environment in normal atmosphere. The transistors were fabricated in the bottom gate top contact configuration, as shown schematically in Fig. 1. Heavily doped Si wafer with thermally grown 150-nm-thick SiO_2 dielectric layer obtained from CEMAT SILICON S.A was used as the gate electrode. The TIPS-Pentacene was purchased from Sigma Aldrich and thin films of this semiconductor were obtained by zone-casting technique from a chlorobenzene solution. The principle of the technique consists in pouring the TIPS-Pentacene/chlorobenzene solution onto a moving substrate via a flat nozzle. In the meniscus formed between the nozzle and the support, a gradient of concentration and of temperature are formed due to the continuous solvent evaporation: these gradients are the driving forces leading to the unidirectional crystallization of the organic semiconductor. The quality and the orientation of the formed crystalline layer depends on several parameters which have to be controlled and optimized: the concentration of the TIPS-Pentacene solution, the temperature of the input solution, the temperature of the substrate, the velocity of the substrate drift, the flow of supplied solution, the height of the meniscus, and the surface energy of the substrate [11]. The thickness of the typical TIPS-Pentacene layer was ca. 200 nm.

After the zone casting procedure, the prepared layers were annealed in vacuum at 100 °C for 4 h in order to remove the residual solvent. Then, 50-nm-thick golden drain-source (DS) electrodes ware evaporated at the top. In this work, the transistor channel length was 50 μm and the channel width was 2 mm. Transistors with two orientations of the DS electrodes with respect to the zone casting direction were prepared: in the first type the current flows along the zone-casting direction, and in the second channel configuration, the current flows perpendicularly to the zone-casting direction. On each zone-cast layer (20 mm × 50 mm), 9 transistors of different orientations were obtained.

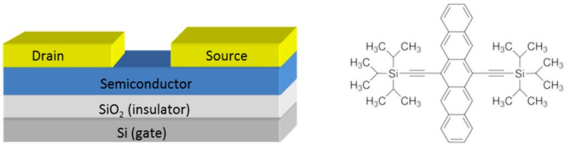

Fig. 1. Schematic view of the bottom gate and top drain-source electrodes field effect transistor (left), and the chemical structure of TIPS-Pentacene (right).

The current-voltage characteristics of OFETs were measured in ambient condition, using needle electrodes and circuits with voltage/current source and dual channel source meter (Keithley 2636A).

Scanning Kelvin probe microscopy combined with the atomic force microscopy was performed with a Cervantes AFM-SKPM head and a Dulcinea controller unit (Nanotec Electronica, Madrid, Spain) which allowed mapping the surface potential profile of the TIPS-Pentacene OFETs under bias simultaneously with the surface topography. The SKPM was operated in air using Arrow EFM Si cantilevers from Nanoworld which were coated by a $PtIr_5$ conductive layer (resonance frequency 75 kHz). The WSxM software [12] was used to drive the Dulcinea controller as well as for the subsequent image analysis. The voltage applied to the DS electrodes was limited by the Nanotec software to ±10 V. In brief, in a first step, the topography profile was measured in tapping mode along the line across the channel between the DS electrodes. Then, along the same scan line, the SKPM signal was acquired by lifting the tip above the surface by 5 nm. An electrostatic force was created due to the surface potential difference between

the biased conductive SKPM tip and the surface of the sample. To determine the local surface potential, a feedback loop was used to eliminate the electrostatic force by application of an adequate voltage to the tip: this potential corresponded to the local surface potential under the tip. Thus, an image of the surface potential of the OFET device could be obtained simultaneously with the topography of the sample.

3. Results and discussion

The orientation of the crystals in the zone-cast layer was checked using Polarized Optical Microscope (POM). Fig. 2 shows typical micrographs obtained for two orientations of the zone-cast TIPS-Pentacene layer in relation to polarization planes of the crossed polarizers. One can observe long crystals grown along the casting direction, what proves that the TIPS-Pentacene molecules exhibit the tendency for unidirectional crystallization. However, the long axis of the TIPS-Pentacene molecules in the crystals is not arranged parallel to the zone-casting direction. The image becomes bright when the zone-casting direction is coincident with the polarization plane. Extinction of image occurs when the sample is rotated of 45°. Dark regions of the POM images are caused by arrangement of the long axis of the molecules in the crystal along the polarization direction of the light. These results indicate that the long axis of TIPS-Pentacene molecules in the layer is inclined close to 45° to the zone-casting direction. Similar effect for the TIPS-Pentacene layer obtained by flow-coating technique has been described in the literature [13, 14].

Representative output and transfer characteristics of the transistors with the channel parallel to the zone-casting direction of the TIPS-Pentacene layer are shown in Fig. 3. The measurements were performed for gate-source V_G and drain-source V_{DS} voltages in the range from 0 V to –30 V. The hysteresis observed in the output characteristics measured for forward and backward sweeps is very small. One can therefore conclude that the hole trapping at the interface between the semiconducting layer and the dielectric layer is very weak.

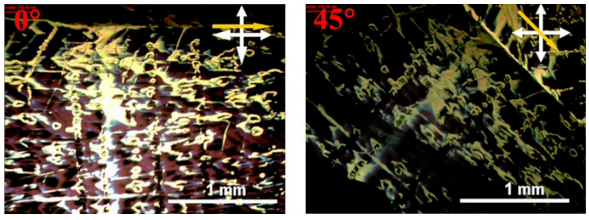

Fig. 2. POM images of the zone-cast TIPS-Pentacene layer on Si/SiO_2 substrate. Yellow arrow indicates the zone-casting direction. White crossed arrows indicate the polarization planes of the polarizer and analyzer.

The charge carrier mobility μ and the ON/OFF ratio were calculated from the saturation region, using the following equations:

$$\mu = \frac{2L}{WC}\left(\frac{\delta\sqrt{I_{DS}}}{\delta V_G}\right)^2 \tag{1}$$

$$\frac{ON}{OFF} = \frac{I_{DSmax}}{I_{DSmin}} \tag{2}$$

where L is the channel length, W the channel width, C the capacitance per unit area, I_{DS} the drain-source current and V_G is the gate voltage. The determined parameters for the parallel device were: $\mu = 0.13\ \mathrm{cm^2 \cdot V^{-1} \cdot s^{-1}}$, ON/OFF $= 10^3$ and $V_{th} = -1$ V and for the perpendicular one it was: $\mu = 0.018\ \mathrm{cm^2 \cdot V^{-1} \cdot s^{-1}}$, ON/OFF $= 10^2$ and $V_{th} = -1$ V. One can see that the charge carrier mobility and ON/OFF ratio for transistor with parallel charge flow were one order of magnitude higher than for the transistor with perpendicular charge flow. The obtained charge carrier mobility is similar to that reported in literature for the devices prepared and measured in ambient conditions, but the threshold voltage is one order of magnitude lower than that presented by Su and coworkers [15] ($\mu = 0.67\ \mathrm{cm^2 \cdot V^{-1} \cdot s^{-1}}$, ON/OFF $6.3 \cdot 10^4$, $V_{th} = -18.9$ V).

The surface morphology of the TIPS-Pentacene layers in the transistors channels was investigated by AFM operated in tapping mode. The TIPS-Pentacene crystals were usually longer than 100 μm, their width was in the range between 10 μm and 30 μm. The channel transistor width

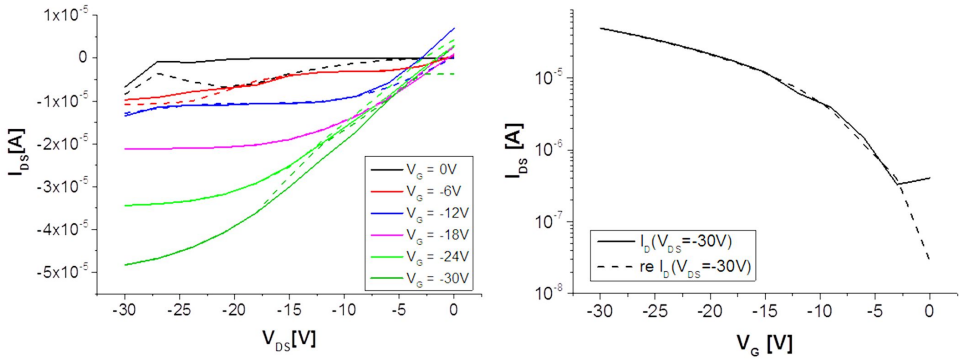

Fig. 3. The output and transfer characteristics of OFET based on TIPS-Pentacene (charge flow parallel to the casting direction) acquired for V_{DS} = –30 V and V_G = –30 V. Solid lines correspond to characteristics measured with increasing drain-source voltage; broken lines correspond to characteristics measured with decreasing drain-source voltage.

50 μm was, thus, shorter than the typical length of the crystal which is important in the "parallel device" where the zone-casting direction is parallel to the charge flow in the transistor channel. Fig. 4 shows the AFM image (left column) and the surface profile (right column) across the transistor channels where the charge flow was parallel (Fig. 4a) or perpendicular (Fig. 4b) with respect to the zone-casting direction. We can observe that in the "parallel device", where the profile was determined along a single crystal, the surface is much smoother (RMS roughness approx. 6 nm and maximum height 25 nm), as compared with the "perpendicular device" in which the profile was obtained across the boundaries of several crystals, the surface RMS roughness was approximately 32 nm and maximum height 163 nm.

Therefore one can assume that when the TIPS-Pentacene single crystals connect directly the drain and the source electrodes, as is the case of the "parallel devices", then the current can flow unhindered between the electrodes and the potential will decrease smoothly along the crystals. However, for the perpendicular orientation, the charge carriers have to travel across several inter-grain boundaries what is seen as disturbance in the surface potential profile. Carlo et al. [16] has demonstrated direct dependence between the semiconductor grains size and charge carrier mobility determined in OFETs. They proved that the potential barrier at the level of grain boundaries is a major reason in the reduction of the charge mobility in devices with small grain sizes. A similar effect of the detrimental influence of grain boundaries on charge transport was also found in highly oriented thin films of regioregular poly(3-hexylthiophene) prepared by directional epitaxial crystallization [17] and mechanical rubbing [18].

In order to determine the correlation between the morphology and the potential map across the channels of the transistors with the oriented TIPS-Pentacene layers, SKPM images (Fig. 5) were simultaneously recorded together with the AFM images shown in Fig. 4a. The SKPM image acquired without applied voltage (Fig. 5a) shows a uniform potential over the surface of the electrodes as well as in the channel; the slight difference between them is related to the different work potentials of the electrode and semiconductor materials. The potential map shown in Fig. 5b, acquired for gate V_G = –5 V and source-drain voltages V_{DS} = –10 V highlights the difference between drain and source electrodes local potentials and smooth, monotonous variation of the potential in the channel. On the basis of such potential 2D maps, the potential profiles for different drain-source voltages and for a constant gate voltage in the "parallel device" were drawn (Fig. 6). It is evident that the main barrier for charge carriers is created at the interface between the source electrode

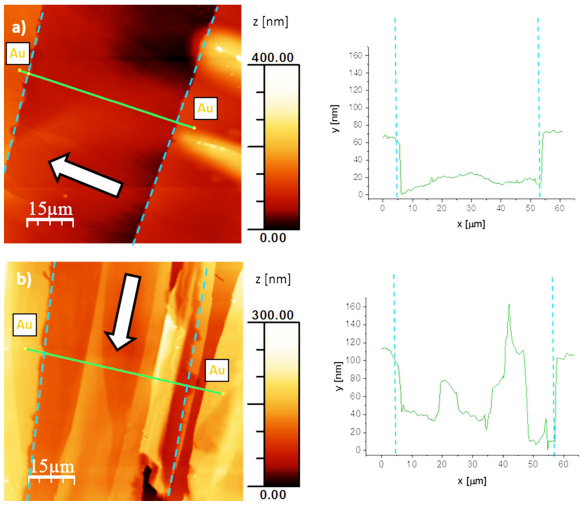

Fig. 4. Left: AFM topography images of the zone-cast TIPS-Pentacene layers in the transistor channel with (a) parallel and (b) perpendicular charge flow in relation to the zone-casting direction. Right: topography profiles along the scan lines indicated by green lines on the corresponding AFM images. The blue dotted lines mark the drain and source electrodes boundaries. The white arrows indicate the direction of the zone-casting.

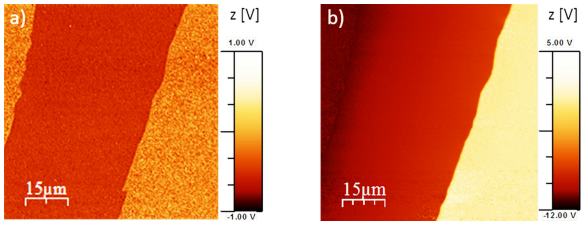

Fig. 5. SKPM 2D local potential map of the transistor channel shown in Fig. 4a: (a) acquired for gate voltage $V_G = 0$ V and drain-source voltage $V_{DS} = 0$ V; (b) acquired for gate voltage $V_G = -5$ V and drain-source voltage $V_{DS} = -10$ V.

and the semiconducting layer. This can be caused by gold diffusion into the TIPS-pentacene during the deposition of metal at high temperatures. The metal may penetrate the semiconductor surface and build some clusters inside the organic layer which are accountable for charge carrier trapping that limits contact injection from source electrode to the TIPS-Pentacene film [19]. The potential profile in the channel is relatively smooth, indicating lack of larger defects, discontinuities or strong trapping. Therefore the charge flow in the transistor channel is uninterrupted. The voltage drop at the drain is very weak.

One can see that in the registered SKPM potential profiles the voltage drop is slightly smaller than the real voltage applied between the drain and source electrodes. Such discrepancy was observed also by Puntambekar et al. [20] and it can be explained by limitation of the precision of SKPM instrumentation.

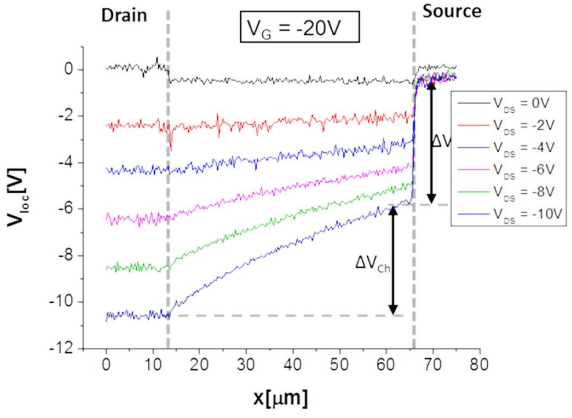

Fig. 6. SKPM local potential profiles acquired for $V_G = -20$ V, sweeping V_{DS} by –2 V steps, for the device with charge transport parallel to the casting direction. Dotted lines show the drain and source electrodes boundaries.

Correlation between the topography and the SKPM potential profile determined along the same line in the transistor channel in the "perpendicular device" is presented in Fig. 7. The topography of semiconductor layer in this device is non-uniform in the channel, due to the polycrystalline morphology (Fig. 4b). Fig. 7 demonstrates how the surface roughness influences the SKPM potential profile obtained at two different locations for the same device. The potential profile in Fig. 7a shows that the major barrier for charge carriers occurs at the interface between the source electrode and the semiconductor. But at another location for the same device (Fig. 7b), the potential drops not only at the electrode/semiconductor interface, but also at some barrier inside the channel which corresponds

to some defects observed in the topography profile as roughness of the crystalline layer.

Similar effect for spin-casted layers of fluorinated 5,11-bis(triethylsilylethynyl) anthradithiophene was reported by Teague et al. [21]. They assigned the barrier in the centre of the channel to a boundary between two grains growing from two opposite electrodes, source and drain, and colliding inside the channel for BG, BC transistor. Discontinuity of the semiconductor layer in the transistor channel resulted in drop of the local potential and in local disturbance of the flow of charge carriers.

In our investigations of transistors we have observed some correlation between the potential drop and the irregularity of surface. Since in the BG, TC transistors the conductive channel is formed at the semiconductor/dielectric interface, one can deduce the morphology heterogeneity visible on the surface over the entire depth of the layer.

Determination of the local potential profiles for given voltages applied to the drain and source electrodes allows calculating the resistance of the source contact and of the semiconducting layer in the transistor channel, respectively. The resistance of the source contact R_S is given by the relation: $R_S = W \cdot \Delta V_S / I_{DS}$, whilst the resistance of the semiconducting layer in the channel is given by $R_{Ch} = W \cdot \Delta V_{Ch} / I_{DS}$, where ΔV_S is the potential drop at the source contact and ΔV_{Ch} is the potential drop in the channel (Fig. 6). The data used in the calculations were taken from the linear part of the output characteristics. The R_S and R_{Ch} resistances calculated per unit area determined for different gate voltages are shown in Fig. 8.

As one can see, both the R_S and R_{Ch} resistances decrease with increasing the gate voltage. This effect is reversible: when $V_G = 0$ V, then the resistance increases again to its original value. One can also see that the R_{Ch} resistance in the "perpendicular device" is by ca. one order of magnitude higher than in the "parallel" OFET. This is understandable, since when the charge carriers have to overcome the crystals boundaries in the channel transistor, then the resistance is much higher.

As expected, the difference between the source contact resistance in the devices with parallel and perpendicular charge flow is relatively low. R_S for the "parallel device" is two times lower than for the "perpendicular device". This difference can be explained by Bullejos et al. [22] unified model for contacts in OFETs. R_S depends directly on contact voltage V_C and in this model V_C is a sum of voltage required for carrier injection through the barrier $V_{Injection}$, voltage generated by ion formation (redox reaction) V_{redox} and charge drift V_{drift}. The equation describing this relationship is shown below:

$$V_C = V_{injection} + V_{redox} + V_{drift} \tag{3}$$

$V_{injection}$ shows a correlation between the work function of the metal electrode and the HOMO level of the active layer. The difference for the presented transistors is quite small (gold work function is –5,1 eV and the TIPS-Pentacene HOMO level is –5,11 eV). Besides, both "parallel" and "perpendicular" devices were fabricated from the same materials. Ion formation V_{redox} is also not crucial in our investigation. The charge drift depends, among others, on carrier mobility. The "parallel" and "perpendicular" OFETs have different charge carrier mobilities, therefore, the contact voltage and the contact/source resistance is different for anisotropic transistors.

Similar trends for channel and source resistance anisotropy was observed by Sakamoto et al. [14] for OFETs based on TIPS-Pentacene fabricated by the flow-coating method. They calculated the resistance by transfer line method.

4. Conclusions

The TIPS-pentacene layers obtained by zone-casting technique were unidirectional and continuous and were successfully used to produce anisotropic OFETs with BG, TC configuration. The combined AFM and SKPM studies revealed correlation between the surface morphology of the organic semiconductor layer and the local potential profile in the transistor channel. The "parallel devices", with rather smooth surface without grain boundaries and defects in transistor channel, exhibited relatively good OFET working parameters and low resistance of the semiconducting layer in the channel. The "perpendicular devices"

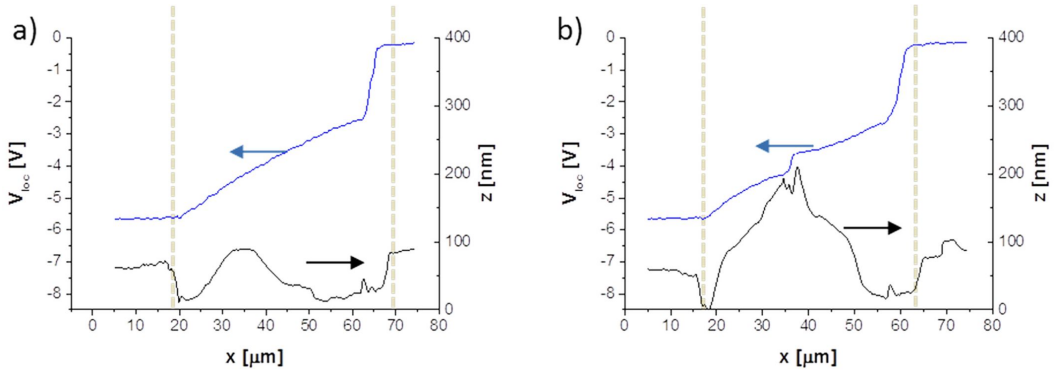

Fig. 7. Potential profiles acquired for $V_{DS} = -5$ V (blue line) and corresponding topography profiles (black line) for two different locations in the same transistor channel where the charge flow is perpendicular to the casting direction. Dotted lines show the drain and source electrodes boundaries.

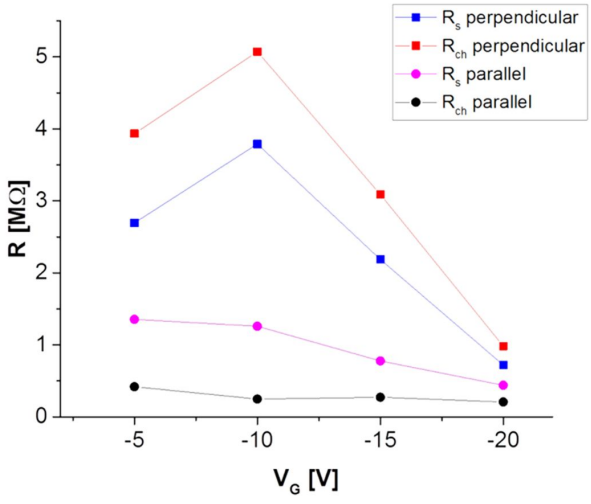

Fig. 8. Source (R_S) and channel (R_{ch}) resistance per unit area determined from the SKPM profiles for $V_{DS} = -5$ V, sweeping V_G by –5 V steps, for the OFETs with channels parallel and perpendicular to the zone-casting direction.

showed considerably worse parameters. Correlation between the step-like changes of surface potential profile and the heterogeneity of the surface indicates, that the defects visible on the surface probably expand through the layer down to the semiconductor/dielectric interface.

Acknowledgements

This work was partially supported by the Polish National Science Centre Project No. 2011/03/N/ST5/04476 and fellow of the Project: "Preparation and implementation of new fields of studies in response to the needs of a contemporary labour market and requirements of knowledge-based economy" co-financed by the European Union under the European Social Fund.

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Received 2018-07-30
Accepted 2019-03-12