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REDUCTION OF ELECTRIC BREAKDOWN VOLTAGE IN LC SWITCHING SHUTTERS

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Liquid crystal display (LCD) industry is among the most rapidly growing and innovating industries in the world. Here continuously much effort is devoted towards developing and implementing new types of LCDs for various applications. Some types of LCDs require relatively high voltages for their operation. For example, bistable displays, in which an altering field at different frequencies is used for switching from clear to scattering states and vice versa, require electric fields at around 10 V/μm for operation. When operated at such high voltages an electrical breakdown is very likely to occur in the liquid crystal (LC) cell. This has been one of the limiting factors for such displays to reach market.

In the present paper, we will report on the results of electrical breakdown investigations in high-voltage LC cells. An electrical breakdown in the cell is observed when current in the liquid crystal layer is above a specific threshold value. The threshold current is determined by conductivity of the liquid crystal as well as point defects, such as dust particles in LC layer, pinholes in coatings and electrode hillocks. In order to reduce the currents flowing through the liquid crystal layer several approaches, such as electrode patterning and adding of various buffer layers in the series with LC layer, have been tested. We demonstrate that the breakdown voltages can be significantly improved by means of adding insulating thin films.

Keywords**:** *electric breakdown, bistable, liquid crystal displays, PEDOT: PSS.*

1. INTRODUCTION

Liquid crystal displays (LCDs) have become indispensable technology in our everyday life. For most of the applications, such as TVs, laptops, tablets and smartphones, the TFT technology is used. For such applications usually nematic LC is used where small electric field values, typically around 1 V/μm, are employed for operating the device [1]. In the switching shutters, the switching field is higher in order to have fast operation of the device. Switching time below 30 ns has been demonstrated with electric field up to 100 V/μm [2]. The required amplitude of the switching electric field also depends on the employed liquid crystal (LC) material. For example, bistable smectic A LC has very high viscosity compared to nematic LC; therefore, up to 14 V/μm high electric field is needed for operation [3], [4]. At large electric fields the electric breakdown is likely to occur. An electrical breakdown in the cell is observed when the electric field intensity E in the LC layer is above a specific breakdown value E_{br}. The E_{br} is governed by the conductivity of the liquid crystal, surface smoothness of the electrodes, defects in coatings as well as point defects, such as dust particles, in the LC layer.

The dielectric breakdown in an LC cell is a complicated process discussed elsewhere [5]. In short, the breakdown occurs due to a sudden decrease in resistance at a particular spot in the LC cell. Such a decrease in resistance may be initiated by an increased charge concentration at one of the electrodes. As the charge is accelerated towards the opposite electrode, an avalanche ionization process or dielectric breakdown may take place. A decrease in the resistance at a particular spot may also arise due to local Joule heating of a defect. In both cases, the current leakage through the defect should be limited in order to reduce the probability of dielectric breakdown to take place in the LC cell.

The reduction of the probability of electrical breakdown can be achieved in multiple ways.

An approach that allows limiting the leakage current in the defect spot was suggested by Palmer [6]. In this approach, in the LC cell there are patterned electrodes. The electrode is patterned in strips such that the resistance of the strips would increase, thus lowering the current in the series. The great benefit of using patterned electrode was that the overall resistance of the cell did not change and, thus, the capacitive charging times of the cell were not affected. Unfortunately, the patterning is visible to the eye since it scatters light. Thus, a compromise between the optical quality and electrical properties should be found.

A seemingly straight-forward way to reduce the current in the series of the LC layer would be to implement buffer layers on the electrodes of the LC cell. The buffer layer considerations have been outlined in the article by Grote and colleagues [7]. To ensure the highest voltage drop on the LC layer while limiting the current in the series of the LC cell, it is suggested to employ claddings with low resistance and high dielectric constants. In standard LCD manufacturing process, typically a hard coat layer based on SiO_x is deposited on an electrode. Polyimide layer is printed on top of hard coat as an alignment layer [8]. As reported earlier by Dierking, an additional polyimide layer increases the electric breakdown voltage, but sputtered SiO_x

decreases it compared with bare ITO [9]. Unfortunately, such an approach, when buffer layers are implemented, increases the overall resistance and the capacitive charging times of the cell.

As reported in multiple investigations [10]–[12], the breakdown probability in the LC cell or similar parallel-plate electrode systems can be significantly reduced by lowering the roughness of the electrode surface. On a rough surface, a local electric discharge may occur due to high local electric field gradients. As mentioned above, this may locally reduce the resistance and, thus, dielectric breakdown may take place. ITO surface roughness can be reduced by depositing PEDOT: PSS smoothing layer on top of it. It also decreases sheet resistance, but transmittance decreases only slightly [13].

In this paper, we describe the results obtained during the implementation of the mentioned methods aimed towards the reduction of dielectric breakdown probability in the LC cells. Several approaches, such as electrode patterning and adding of various buffer layers in the series with LC layer, have been tested in the LCD manufacturing workflow and are described in the experimental and summary parts of this paper.

2. EXPERIMENTAL PART

We have employed three different approaches for reducing the probability of dielectric breakdown in the LC cells. All of them are related to preparation of the substrate surfaces, between which the LC is inserted. In the first approach, the LC is inserted between patterned ITO coated glass substrates. In the second approach, an insulating layer is inserted between the unpatterned ITO coated glass substrate and LC layer. Finally, we have also attempted to reduce the probability of dielectric breakdown by adding a conducting smoothing layer on an unpatterned ITO coated glass substrate. The mentioned implemented approaches have been used in the preparation of LC cells. Cells are made of two 80 x 80 mm substrates processed according to the principles described above. To maintain a constant cell gap, 15 µm plastic ball spacers with density 10 pcs/mm^2 have been used. One-liquid type epoxy XN-21 is used as a gasket material. The gasket lines keep substrates together and prevent LC from flowing out of the cell. Cells have been filled by the vacuum method through a filling port with commercial nematic LC MDA-05-4876 mixed with chiral dopant and sealed with UV glue. Contacts have been soldered on top and bottom electrodes. The electric field intensity in the LC layer can vary from 0 to 17 V/µm (see Fig. 1).

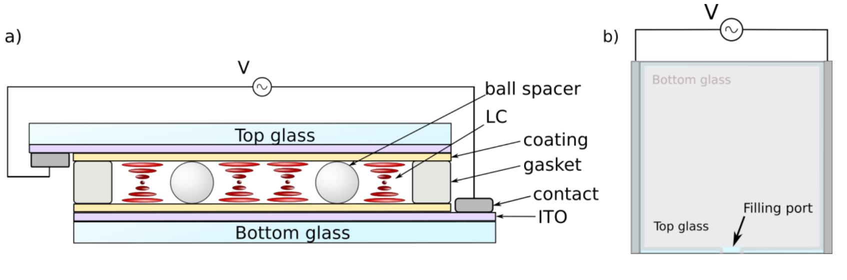

Fig. 1. Schematic picture of LC cell; a) cross-section b) top view.

For electrode patterning, we have used a 1030 nm picosecond fibre laser. The laser ablation method is very fast, simple and precise. By ITO ablation, the electrode has been patterned with 15 micron wide lines as demonstrated in Fig. 2 and then washed in wet cleaner with detergent and brush. Such patterning has allowed us to increase the resistance, which is in the series of a defect point and, thus, to reduce the leakage currents. The resistance R of the patterned electrode in the series with the defect point can be calculated by

$$R = \frac{H}{W} R_0 \qquad (1)$$

where H is the electrode height, W is the electrode width and R_0 is the sheet resistance of the ITO electrode, which is 80 Ω/sq. LC cells comprising patterned ITO electrodes with electrode heights from 0.08 mm to 80 mm have been prepared.

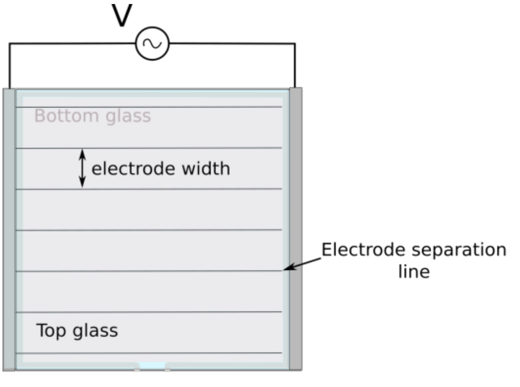

Fig. 2. Top and bottom electrodes patterned with IR laser.

As mentioned previously, the probability to observe dielectric breakdown in the LC cell can be significantly reduced by adding insulating and smoothing layers between the ITO electrode and the LC layer. We have inserted insulating layers between the unpatterned ITO coated glass substrate and LC layer. In the industry, it is common to employ at least two insulating layers – a solid and hard bottom layer, e.g., SiO_x, and a softer LC orienting layer of PI [8]. The hard layer prevents the formation of electrical contact between an electrode and LC layer via dust or other particles during preparation of the cell. The insulating coating layer of SiO_x and/or polyimide (PI) has been applied using the flexoprinting method. In flexoprinting, the material is fed from a dispenser to a doctor roll (see Fig. 3), then the doctor roll transfers the material to an anilox roll. Anilox roll has engraved cells that carry a certain amount of coating. Mask cylinder holds a mask with desired coating dimensions. Coating material is transferred from the anilox roll to the mask and then to glass. At the second stage, glass is transferred to a hot plate, where solvent gets evaporated at 80 °C for 3.5 min. The SiO_x coating is cured in oven at 300 °C for 30 min, but polyimide at 220 °C for 30 min. SiO_x and STN PI have been provided by Nissan (N) and VA PI by Dalton (D). The coatings have been prepared in an industrially clean environment (ISO Class 6).

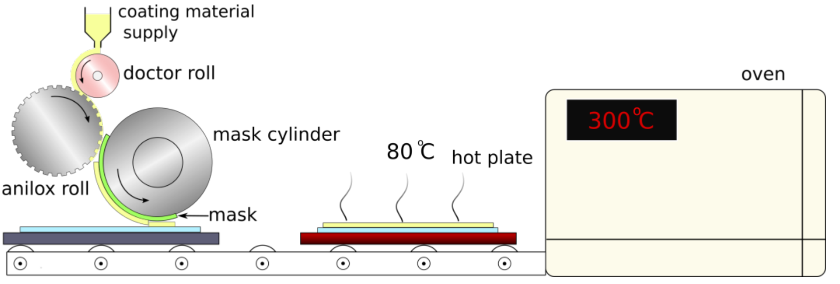

Fig. 3. Flexoprinting and curing process.

Four different sets of samples have been prepared using the flexoprinting method. The insulating layers and their abbreviations are described in Table 1. Table 1 also holds the measured thicknesses of the coatings. The thickness has been measured with a white light interferometer Zygo "NewView 7100".

Table 1

LC Cell Insulating Layers and Their Abbreviations

Coating abbreviation	Explanation	Thickness
PI+PI (VA)	An insulating layer consisting of two VA PI layers on ITO	160±5 nm
SiO_x+PI (STN)	An insulating layer consisting of a SiO_x and one STN PI layer on ITO	157±12 nm
SiO_x+PI+PI (STN)	An insulating layer consisting of a SiO_x and two STN PI layers on ITO	255±23 nm
SiO_x+PI+PI+PI (STN)	An insulating layer consisting of a SiO_x and three STN PI layers on ITO	437±11 nm

In further investigations, we have employed PEDOT: PSS smoothing layers between the ITO electrode and the LC layer in the LC cell. For this application, the screen printing method has been used. Screen printing is a widely used method for solvent based coatings and pastes. Even though the spin coating method is usually used for creating smooth surfaces with PEDOT:PSS, it cannot be employed for covering large areas. In the screen printing method, a mesh is stretched over metal frame (see Fig. 4) and is coated with emulsion leaving open areas, where coating material is pressed through with a squeegee, thus forming a pattern on glass. PEDOT: PSS provided by Hereus has been printed with 180/32 polyester mesh with printing speed of 300 mm/s. After printing PEDOT:PSS coating has been cured in oven at 110 °C for 15 minutes.

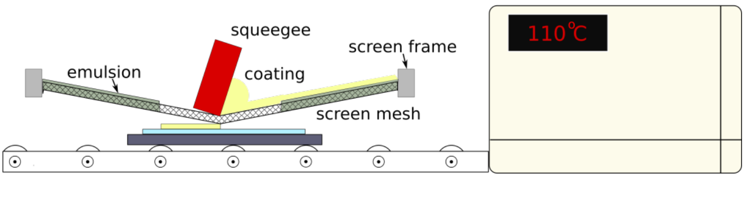

Fig. 4. Screen printing and curing process.

Four different sets of samples have been prepared using the flexoprinting and screen printing methods. The coating layers and their abbreviations are described in Table 2.

Table 2

LC Cells Comprising PEDOT:PSS Layers

Coating abbreviation	Explanation	Thickness
PEDOT:PSS	Single PEDOT:PSS layer	65±52 nm
SiO_x+ PEDOT:PSS	A PEDOT:PSS layer on a SiO_x layer	225±60 nm
PEDOT:PSS+PEDOT:PSS	Two PEDOT:PSS layers	130±104 nm
PEDOT:PSS+SiO_x	A SiO_x layer on a PEDOT:PSS layer	225±60 nm

3. RESULTS AND DISCUSSION

3.1. Electrode Patterning

The measured breakdown voltage as a function of patterned ITO electrode height is shown in Fig. 5. In Fig. 5, the red line indicates the electric field intensity limit of 17 V/µm that we could apply in the cell. We have used a rough approximation of the data points indicated by a blue striped line. As evident from the graph, an LC cell with an unpatterned electrode has a breakdown electric field of around 10 V/µm. As stripes are drawn on the ITO electrode the breakdown electric field intensity decreases. Our first assumption has been that such occurrence may take place due to increased electric field gradients at the edge of the ablated line. However, inspecting the breakdown places at the LC cells we have found that their positions are not related to the location of the ablated lines. Thus, we suggest that the decrease in the breakdown field value is related to the contamination that appears during ITO patterning with the laser beam ablation method. As the number of lines is increased or, in other words, as the electrode height is reduced, the breakdown electric field value of the LC cell is enhanced as expected from the theory.

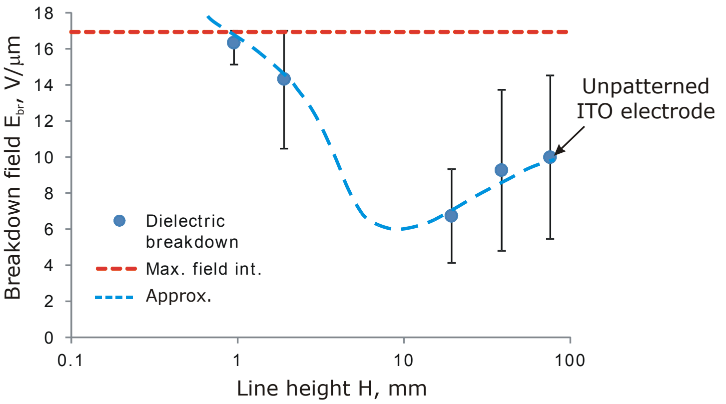

Fig. 5. LC breakdown field intensity as a function of ITO patterned line height.

3.2. Insertion of Insulating Layers

The measured breakdown field intensity for the prepared samples, including LC cells with no insulating coating, is displayed in Fig. 6. From Fig. 6, it can be seen that the breakdown field intensity and its standard deviation have been improved by adding insulating layers. It can be noticed that a coating consisting of SiO_x and PI has improved the dielectric breakdown field intensity by 50 %; however, a coating from two PI layers has enhanced the dielectric breakdown field only by 16 %.

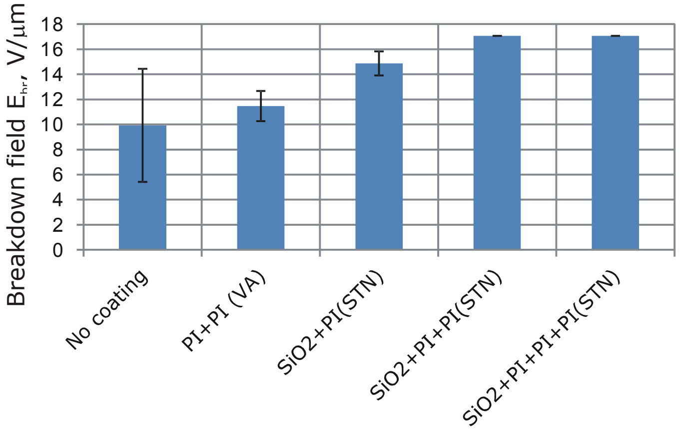

Fig. 6. Breakdown field intensity in the LC cells with various insulating coatings between the ITO electrode and the LC layer.

In order to explain these results, we have performed resistance and AFM measurements of insulating layers. The samples have been made of ITO coated substrates coated with insulating layers used in the LC cells. The layers have been made as single layers, e.g., only PI, only SiO_x, and as bilayers, e.g., PI+PI, SiO_x+PI. In the resistance measurement, a top electrode on the insulating layer under investigation is required. We have firstly implemented a sputtered Al as a top electrode. After the electrode sputtering, the measured resistance of the insulating layer has been below 1 kΩ. Our hypothesis is that during sputtering the Al penetrates through the insulating layer creating low resistance channels. Thus, a different approach to measuring resistance has to be employed. As a top electrode, we have used a liquid metal alloy poured into a Teflon ring placed on the insulating layer. The experimental sample configuration used for measuring the resistance of the thin insulating layers at the room temperature is shown in Fig. 7.

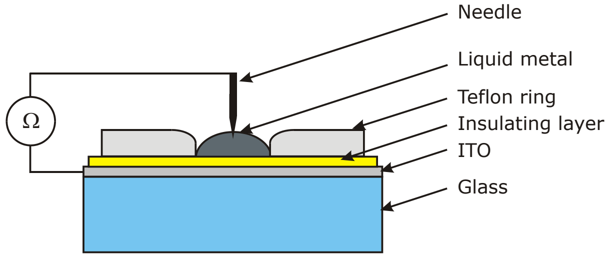

Fig. 7. The experimental setup used for measuring the resistance of the thin insulating layers.

During the resistance measurements of single insulating layers, we have found that after pouring the liquid metal into the Teflon ring the resistance of the film slowly decreases and saturates at around 200 Ω. Such an effect has been observed for every insulating coating consisting of a single layer and it is independent of coating material employed. For bilayer coatings, a similar effect can be observed if the layers are made from PI. Only two-layer insulating coatings made from SiO_x and STN PI have shown high resistance.

The measurements have indicated that an ohmic contact between liquid metal alloy and ITO is formed during the resistance measurements. The explanation of this result has been found after performing the AFM measurements of the thin insulating film. The surface of the layers has proved to be very smooth; however, at some locations of the film we have found small holes, which obviously have formed during the preparation of the film (see Fig. 8). The width of the holes is typically on the order of 100 nm.

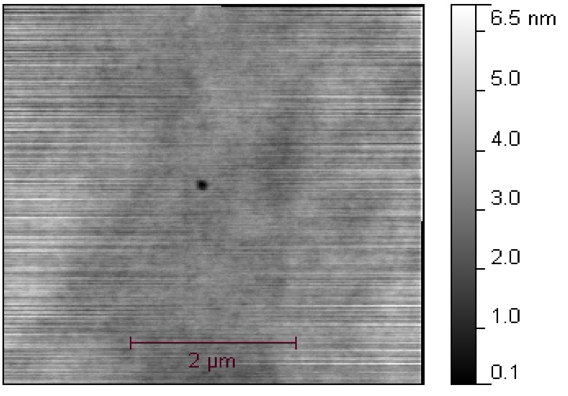

Fig. 8. The AMF image of the SiO_x coating surface.

The resistance measurements suggest that adding only a single insulation layer cannot significantly improve the breakdown field intensity since there will always be a breakdown channel in the film. Coating does not wet the ITO surface where contamination and pinhole are formed around it. It is reasonable to expect that the second coating layer will cover the pinhole in the first layer and operate as an insulating layer. However, we believe that the second PI layer also forms a pinhole on top of pinhole in the first layer, and breakdown channel is still formed despite two layers. PI fills pinholes in SiO_x better than in PI and forms less breakdown channels in coating and improves a dielectric breakdown value. Thus, in order to improve the dielectric breakdown field intensity in the LC cell, it is suggested to use at least one SiO_x layer and one PI layer. It is important to note that by adding VA PI the transmittance improves by 0.3 %. The optical absorption in the film is reduced if an alignment layer VA is employed. The molecules are aligned normal to the PI surface, thus interacting less with the light, which is incident normal to the PI surface. Addition of STN PI on SiO_x coating reduces the optical transmittance by 2.5 %.

3.3. Insertion of Smoothing Layers

As shown in Table 2, the obtained PEDOT:PSS layer is very rough. The standard deviation of layer thickness is around 52 nm or 80 % of the total thickness. For some samples, the PEDOT:PSS is coated on the SiO_x prepared by the flexoprinting method described previously. The measured breakdown field intensity for the prepared samples, including LC cells with no conducting PEDOT:PSS coating, is displayed in Fig. 9. As it is evident from the graph, the breakdown field intensity is reduced, the PEDOT:PSS layer is employed between the ITO electrode and the LC layer. The obtained results clearly indicate that the PEDOT:PSS, if applied with the screen printing method, does not improve the electrical properties of the LC cell. The main cause of the reduction of breakdown field intensity in the cells is the rough surface of the PEDOT:PSS.

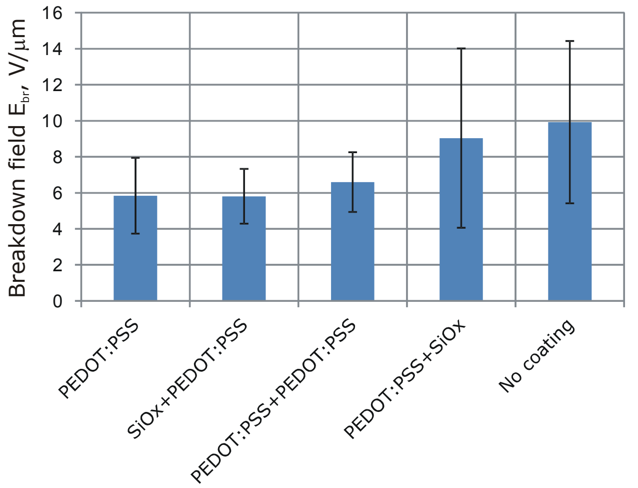

Fig. 9. Breakdown field intensity in the LC cells with various PEDOT and SiO_x coatings between the ITO electrode and the LC layer.

4. CONCLUSIONS

We have presented the results obtained during the implementation of methods for reduction of breakdown probability in the industrially manufactured LC cells.

Three different approaches have been implemented and tested.

In the first approach, an LC cell electrode patterning via laser ablation has been introduced in order to reduce the leakage currents in the cell. Unfortunately, the dielectric breakdown field enhancement is observed only if a critical resistance of the sheet is achieved. This is due to the fact that during laser ablation contamination is produced that increases the probability to observe the dielectric breakdown. Obviously, great care should be taken during cleaning of the electrodes after patterning.

In the second approach, we have inserted electrically insulating coatings between the LC and electrode layer. The insulating coatings of SiO_x and/or PI have been applied using the flexoprinting method. It has been shown that at least two coating layers are required in order to observe the enhancement of the dielectric breakdown field intensity. If two PI coating layers are employed, there is a high probability that pinholes will be formed in both layers causing an electrical contact between the LC and electrode to appear. The coating combination of SiO_x and PI has improved the dielectric breakdown field intensity of the cell by 50 % due to the lack of breakdown channels in coating. It has also been confirmed that a PI alignment layer increases the optical transmittance. We have measured an increase in the optical transmission by 0.3 %.

Finally, in the third approach we have inserted a conductive PEDOT:PSS layer between the LC and electrode layer using the screen printing method. We have aimed to lower the roughness of the electrode surface, thus increasing the dielectric breakdown field in the LC cell. Unfortunately, the PEDOT:PSS coating obtained with the screen printing method has very rough surfaces. The standard deviation of the PEDOT:PSS film thickness is usually around 80 %. Compared to LC cells with no conductive coatings, no enhancement of the dielectric breakdown field is found if the PEDOT:PSS layer is introduced via the screen printing method.

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ELEKTRISKĀS CAURSITES SPRIEGUMA SAMAZINĀŠANA ŠĶIDRO KRISTĀLU ŠŪNĀS

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Kopsavilkums

Šķidro kristālu ekrānu (LCD) industrija ir viena no visstraujāk augošajām industrijām pasaulē. Daudz pūļu un resursu tiek veltīti jauna tipa LCD izstrādē dažādiem pielietojumiem. Atsevišķa tipa LCD funkcionēšanai nepieciešami augsti spriegumi. Piemēram, bistabilos LCD, kuros izkliedējošs (ieslēgts) un dzidrs (izslēgts) stāvoklis tiek iegūts ar dažādu frekvenču maiņsprieguma palīdzību, elektriskā lauka intensitāte šķidrā kristāla slānī var sasniegt pat 10 V/µm. Augstās elektriskā lauka intensitātes dēļ ir liela varbūtība šķidro kristālu (LC) šūnā novērot elektrisko caursiti, kuras laikā LC šūna tiek sabojāta. Šis ir viens no galvenajiem iemesliem, kāpēc šāda tipa ekrāni pagaidām vēl nav komerciāli plaši pieejami.

Šajā darbā mēs skaidrojam rezultātus, kas iegūti, veicot LC šūnu caursites pētījumus. Elektrisko caursiti LC šūnā novēro brīdī, kad strāva tajā pārsniedz noteiktu sliekšņa vērtību. Strāvas stipruma sliekšņa vērtību nosaka šķidrā kristāla īpatnējā vadītspējā, kā arī punktu defekti LC šūnā, piemēram, putekļi, elektrodu raupjums, caurumi u.c. Strāvas stipruma ierobežošanai šūnā šajā darbā tika izmantotas dažādas metodes – buferslāņu iekļaušana, elektroda izlīdzinošā slāņa iekļaušana, kā arī elektroda sadalīšana ar lāzera ablācijas metodi. Tiek demonstrēts, ka elektrisko lauku, pie kura novēro caursiti šūnās, ir iespējams būtiski palielināt, šūnā iekļaujot elektriskos izolējošus buferslāņus un sadalot elektrodu.

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