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PAPERS

Multi-way differential power divider with microstrip output interfaces

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The design and implementation of planar multi-way differential power dividers remain a challenge in terms of the compactness and especially, for the achievable characteristic impedance of the quarter-wavelength transformer when considering large number of outputs. In this work, the double-sided parallel stripline is recommended to realize such a power divider with out-of-phase outputs, and explicit design methods are provided. The proposed multi-way power divider was developed without the use of lump elements on a single substrate. For system applications, a prototype operating at 41.6 MHz with 12 pairs of out-of-phase outputs that utilize the microstrip line as the output interfaces was fabricated and examined. At the center frequency of 41.6MHz, the developed prototype measured insertion losses akin to 14.3 dB as compared with the theoretical data of 13.8 dB. The attainable impedance bandwidth ranges from 10 MHz to 80 MHz under a magnitude imbalance of ±0.3 dB. The isolations of the adjacent outputs are about 13.1 dB as compared with the theoretical values of 14.428 dB, and are better than 34 dB for more distant ones. Parameter measurements are in good agreement with the numerical predications, thus demonstrating the realization of the proposed multi-way power divider.

K e y w o r d s: power divider, multi-way, differential, microstrip

1 Introduction

As an important component of microwave circuit, power dividers has been extensively applied in electromagnetic signal transmission systems. The differential type of power divider allocates one input signal into multiple outputs, where each pair of outputs exhibits out-of-phase characteristics, and all outputs being equal in magnitude for most cases. Such a kind of structure find applications in power amplifiers, mixers and feeding networks of antenna arrays.

The design of multi-way power divider using different methods has been extensively studied by several researchers in recent years. Instead of conventional lumped resistors, a saw-tooth graphene flake is fabricated to obtain good isolation between arbitrary output ports [1]. A planar network with RLC and LC structures are introduced in a four-way power divider, and excellent impedance matching and output isolation can be realized [2]. In [3], the approach of balanced-to-single-ended and single-ended-to-balanced is adopted in 1-to-2^n way power divider. Compared with balanced-to-balanced ones, the circuit size is effectively reduced. By using p-i-n diodes, an N-way reconfigurable power divider is constructed simply with low insertion loss and high isolation between transmission ports [4]. In [5], arbitrary power-dividing ratio for an N-way power divider is developed by using node voltage and current method. Based on microstrip-line Marchand balun, a multiple power divider is miniaturized, and out-of-phase outputs are achieved [6]. Lumped-elements have been utilized in multi-way power divider to feature length-saving or filtering property [7, 8]. Capacitors can be added between the coupled lines to improve the return loss of outputs [9]. At low frequencies, the power divider is designed using lumped-elements to obtain size reduction or high isolation [10, 11]. However, the number of output ports are small, and the amplitude and phase differences between outputs fluctuates due to the tolerance of the lumped-elements.

This article presents a multi-way differential power divider with 12 pairs of differential outputs. The developed differential divider, based on the double-sided parallel stripline, uses the microstrip line as the outputs. This structure only uses a single substrate, thus facilitating the fabrication and assembling, and further, reducing the cost. In this work, the studied differential topology is first analyzed, and several explicit design equations are given as a guide for developing such a kind of multi-way power divider network. A prototype centered at 41.6 MHz, was fabricated and measured. Results indicate the examinations match well with the analysis, thus confirming the studied differential scheme and analysis method.

2 Topology and analyses

To obtain the out-of-phase outputs, the double-sided parallel stripline is adopted in this proposed multi-way power divider. As shown in Fig. 1, the same topology is

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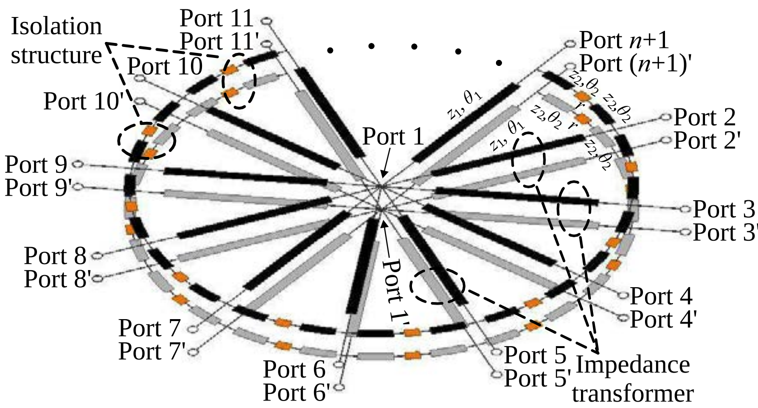

Fig. 1. Topology of the multi-way differential power divider, where the upper and lower structures are shown in black and gray

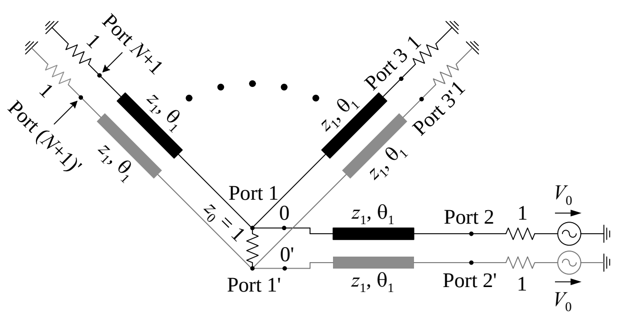

Fig. 2. Equivalent circuit of the studied power divider to analyze the isolation of a differential pair by omitting the closed-ring isolation structure

placed on the top and bottom side of a microwave substrate, including the impedance transformers and isolation structures. The inputs, named port 1 and port 1', are centrally located. The outputs – port 2 to port $n+1$ and port 2' to port $(n+1)$' – are spread outwards in a star-shape distribution. The impedance transformer (normalized impedance and electrical length are marked as z_1 and θ_1), composed of a pair of double-sided parallel stripline, is the key component used to attain the differential pairs. The isolation structure (marked as z_2 and θ_2), with a lumped resistor r centered between two striplines, is connected with adjacent outputs. For such a kind of topology, when the impedance transformers are of quarter wavelengths at the center operation frequency, the normalized characteristic impedances for n-pair output ports are given by [12]

$$z_1 = \sqrt{2n} \tag{1}$$

Figure 1 shows the layout of the proposed power divider network, showing impedance lines and the isolation structures as well as the input and multiple output ports for both upper and lower structures.

Assuming and denoting an identity matrix as E, the scattering matrix can be determined as [13, 14]

$$S = 2(E + \frac{1}{r}M^{-1} - (N + E) \tag{2}$$

Where, M and N are $n \times n$ matrix and given by

$$M = \begin{bmatrix} 2 & -1 & 0 & 0 & \cdots & 0 & -1 \\ -1 & 2 & -1 & 0 & \cdots & 0 & 0 \\ 0 & -1 & 2 & -1 & 0 & \cdots & 0 \\ \vdots & 0 & \ddots & \ddots & \ddots & \ddots & \vdots \\ \vdots & \vdots & \ddots & \ddots & \ddots & \ddots & 0 \\ 0 & 0 & \cdots & 0 & -1 & 2 & -1 \\ -1 & 0 & \cdots & 0 & 0 & -1 & 2 \end{bmatrix} \tag{3}$$

$$N = \begin{bmatrix} \frac{1}{n} & \frac{1}{n} & \cdots & \cdots & \cdots & \cdots & \frac{1}{n} \\ \frac{1}{n} & \frac{1}{n} & \frac{1}{n} & \cdots & \cdots & \cdots & \frac{1}{n} \\ & & & & & & \\ \vdots & \ddots & \ddots & \ddots & & & \vdots \\ \vdots & & \ddots & & & \ddots & \vdots \\ \vdots & & & & \ddots & \ddots & \frac{1}{n} \\ \frac{1}{n} & \cdots & \cdots & \cdots & \cdots & \frac{1}{n} & \frac{1}{n} \end{bmatrix} \tag{4}$$

Notice that the above formulation is valid at the center operation frequency, and the transmission-line pair of the isolation structure (denoted by z_2 and θ_2) as shown in Fig. 1 is omitted here as a result of its very small length compared to the quarter-wavelength transformer, *ie*, $\theta_2 << \theta_1 = 90°$.

For the multiway-outputs (take 11- and 12-way for example), Tab. 1 shows scattering parameters under different conditions. It indicates that a matched output leads to relatively poor isolation between the adjacent ports, while ideal isolations between adjacent ports are achievable at the cost of very poor output return loss, which is less than 3 dB. By setting the output return loss equal to isolation between adjacent ports, a tradeoff can be approached.

Table 1. Scattering parameters of 11-way and 12-way outputs under different conditions, where $i = 2, 3, \ldots, 13$

Number of pairs	Conditions	Normalized r	Results: (Data in braces are in dB)
$n = 11$	$S_{ii} = 0$	1.694	$S_{i,\ i+1} = 0.23$ (12.767) $S_{i,\ i+2} = 0.004$ (49.171) $S_{i,\ i+3} = 0.063$ (24.001) $S_{i,i+4} = 0.083$ (21.667) $S_{i,\ i+5} = 0.088$ (21.13)
	$S_{i,\ i+1} = 0$	17.944	$S_{ii} = 0.718$ (2.882) $S_{i,\ i+2} = 0.086$ (21.276) $S_{i,\ i+3} = 0.091$ (20.85) $S_{i,\ i+4} = 0.091$ (20.829) $S_{i,\ i+5} = 0.091$ (20.828)
	$S_{ii} = S_{i,\ i+1}$	2.781	$S_{ii} = S_{i,\ i+1} = 0.19$ (14.431) $S_{i,\ i+2} = 0.029$ (30.646) $S_{i,\ i+3} = 0.077$ (22.224) $S_{i,\ i+4} = 0.088$ (21.118) $S_{i,\ i+5} = 0.09$ (20.904)
$n = 12$	$S_{ii} = 0$	1.661	$S_{i,\ i+1} = 0.239$ (12.441) $S_{i,\ i+2} = 0.012$ (38.114) $S_{i,\ i+3} = 0.055$ (25.217) $S_{i,\ i+4} = 0.075$ (22.522) $S_{i,\ i+5} = 0.081$ (21.874) $S_{i,\ i+6} = 0.082$ (21.741)
	$S_{i,\ i+1} = 0$	19.95	$S_{ii} = 0.742$ (2.592) $S_{i,\ i+2} = 0.08$ (21.99) $S_{i,\ i+3} = 0.08$ (21.602) $S_{i,\ i+4} = 0.08$ (21.584) $S_{i,\ i+5} = 0.08$ (21.584) $S_{i,\ i+6} = 0.08$ (21.584)
	$S_{ii} = S_{i,\ i+1}$	2.781	$S_{ii} = S_{i,\ i+1} = 0.197$ (14.091) $S_{i,\ i+2} = 0.0218$ (33.239) $S_{i,\ i+3} = 0.0698$ (23.118) $S_{i,\ i+4} = 0.0804$ (21.898) $S_{i,\ i+5} = 0.0827$ (21.655) $S_{i,\ i+6} = 0.083$ (21.613)

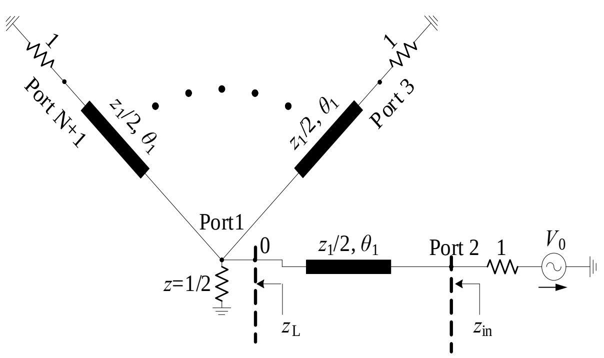

Fig. 3. The odd-mode equivalent circuit to study the isolation of a differential pair

The isolation performances among differential pairs, *ie* $S_{22'}$ in Fig. 1, are discussed here but, for simplicity, the closed-ring shaped isolation structure is not included in the analysis. When the output loads of all differential pairs are terminated as $z_\mathrm{L} = 1$, its equivalent circuit can be described as shown in Fig. 2, showing the equivalent circuit of the studied power divider to analyze the isolation of a differential pair by omitting the closed-ring isolation structure.

In Fig. 2, the even- and odd-mode methods are used to analyze the isolation performance of the differential pair. For the even-mode excitation, in-phase sources are applied to ports 2 and 2', corresponding to inserting an infinite magnetic wall along the halved thickness of the substrate. In this case, the reflection coefficient of port 2 would be

$$\Gamma_{22\,\mathrm{e}} = 1 \tag{5}$$

For the odd-mode excitation, anti-phase sources are applied to ports 2 and 2', corresponding to placing an electric wall along the halved thickness of the substrate. Thus, the stripline is reduced to the microstrip line with a halved thickness, where its odd-mode characteristic impedance $z_{1\mathrm{o}}$ would be [15]

$$z_{1\mathrm{o}} = \frac{z_1}{2} \tag{6}$$

Figure 3 shows the odd-mode equivalent circuit to study the isolation of the differential pair.

In this case, the equivalent circuit shown in Fig. 2 can be further simplified as illustrated in Fig. 3, where the odd-mode reflection coefficient of port 2 is therefore given by

$$\Gamma_{22\mathrm{o}} = \frac{z_\mathrm{in} - 1}{z_\mathrm{in} + 1} \tag{7}$$

where z_in is the input impedance at port 2 that is

$$z_\mathrm{in} = \frac{z_1}{2} \frac{2z_\mathrm{L} + jz_1 \tan\theta_1}{z_1 + j2z_\mathrm{L} \tan\theta_1} \tag{8}$$

and z_L is the load impedance at the reference plane 0 and given by

$$z_\mathrm{L} = \frac{1}{2} || \frac{1}{N-1} \frac{z_1}{2} \frac{2 + jz_1 \tan\theta_1}{z_1 + j2\tan\theta_1} \tag{9}$$

where symbol || denotes the two components in parallel.

To this end, the isolation of a differential pair would be [12]

$$S_{22'} = \frac{\Gamma_{22\,\mathrm{e}} - \Gamma_{22\,\mathrm{o}}}{2} \tag{10}$$

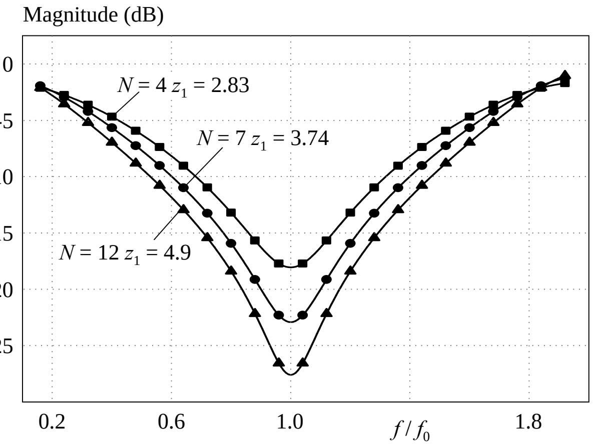

Fig. 4. The isolation of a differential pair for $N = 4$, 7, and 12 pairs

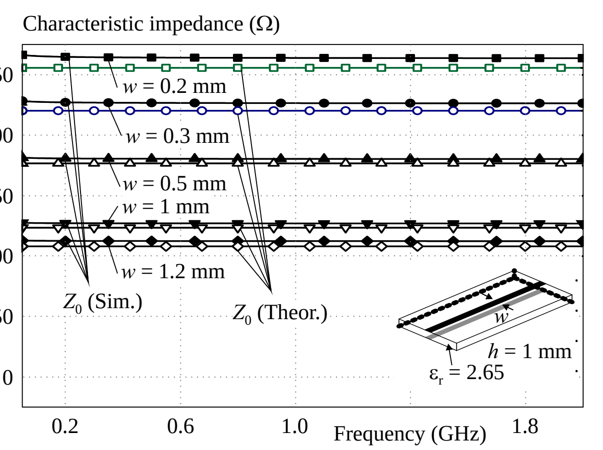

Fig. 5. Characteristic impedances of the broadside-coupled stripline under different line widths

Table 2. Physical parameters of the demonstrator (units: mm)

$l = 83.6$	$d = 24.9$	$w_1 = 22.3$	$w_2 = 0.3$	$w_3 = 1$
$w_4 = 0.75$	$w_5 = 2.7$	$w_6 = 1.2$	$w_7 = 5.8$	$w_8 = 1$

Here, we further specify 4-pair, 7-pair and 12-pair differential outputs to investigate the isolations of a differential pair. Figure 4 plots the calculated results based on the above discussions, where the normalized characteristic impedances, z_1, of the impedance transformer are respectively determined from (1). As shown in Fig. 4, good isolations are observed between a differential pair. Meanwhile, with the increase of the output pairs, the isolation can be further enhanced.

3 Design of power divider with 12 pair differential outputs

A prototype demonstrator is designed. The center operation frequencies is 41.6 MHz. Based on the above studies, the quarter-wavelength transformer has the characteristic impedance of $Z_1 = \sqrt{24}Z_0 \approx 244.949\,\Omega$. Meanwhile, we choose $S_{22} = S_{23}$ from Tab. 1 in this design, thus the isolation resistors is $R = 139.05\,\Omega$ when referring to a system of $Z_0 = 50\,\Omega$ impedance.

Figure 5 shows the characteristic impedances of the broadside-coupled stripline under different line widths as indicated for both calculated and EM simulations.

Based on the studies by Wheeler [16], the characteristic impedances of the transformer pair for several line widths are calculated. Figure 5 records the calculated and electromagnetic (EM) simulated results, where full-wave EM simulator, Ansoft HFSS, is utilized and the microwave substrate has a relative permittivity of $\varepsilon_r = 2.65$ and a thickness of $h = 1$ mm. It is observed from Fig. 5 that very high impedance ($> 250\,\Omega$) can be readily achieved by using this kind of transmission line, and the theoretical calculations presented by Wheeler is in good agreement with the EM simulations. Meanwhile, constant impedances were found within a wide frequency range, indicating its potential advantage for practical applications. From these results, the line width in this design is selected as $w = 0.3$ mm by using the same substrate.

In Fig. 1, the transmission-line pair of the isolation structure denoted by z_2 and θ_2 functions as bridging the isolation resistors among outputs. Hence, its length is designed to be as short as possible. It is achieved by meandering the radially distributed quarter-wavelength transformers, thus leading to compact designs. Notice that due to the complexity of analytic discussions on the closed-ring isolation network when involving the transmission-line pair, no analytic methods were constructed. Consequently, the design guide is initially set to $z_2 = 2$ and θ_2 being small enough, while the exact determinations of z_2 and θ_2 are based on the numerical calculations of the entire network. The small length, θ_2, of the isolation network would introduce extra reactance to the impedance transformer, thus shifting the center operation frequency slightly, which can be shifted back by slightly tuning the length, θ_1, of the transformer.

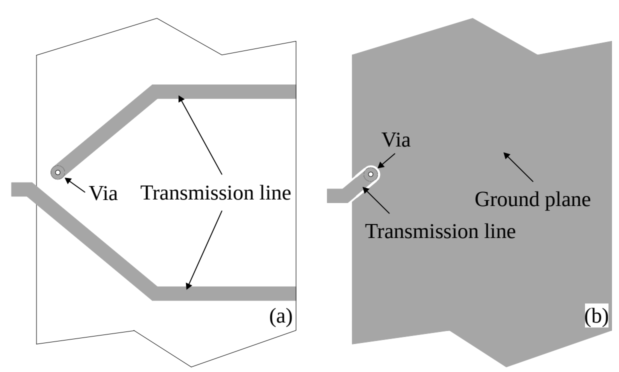

Fig. 6. Microstrip line based differential outputs. (a) – front side, (b) – back side

Table 3. Performance comparisons of power dividers

Reference /Years	Central frequency (MHz)	Bandwidth (%) (return loss < 10 dB)	Number of ways	Number of layers	In phase or out-of-phase	Using lumped element
(1)/2018	2400	35.4	9	2	in phase	no
(2)/2018	1000	50	4	1	in phase	no
(3)/2016	1800	36.1	8	1	out-of-phase	no
(4)/2017	5000	40	4	2	in phase	no
(5)/2019	3450	49.3	6	2	in phase	no
(6)/2019	3400	85.3	4	1	out-of-phase	no
(7)/2018	1000	90	8	1	in phase	yes
(9)/2018	1510	34.4	4	1	in phase	yes
(10)/2013	435	39	5	1	in phase	yes
This work	41.6	40	24	1	out-of-phase	no

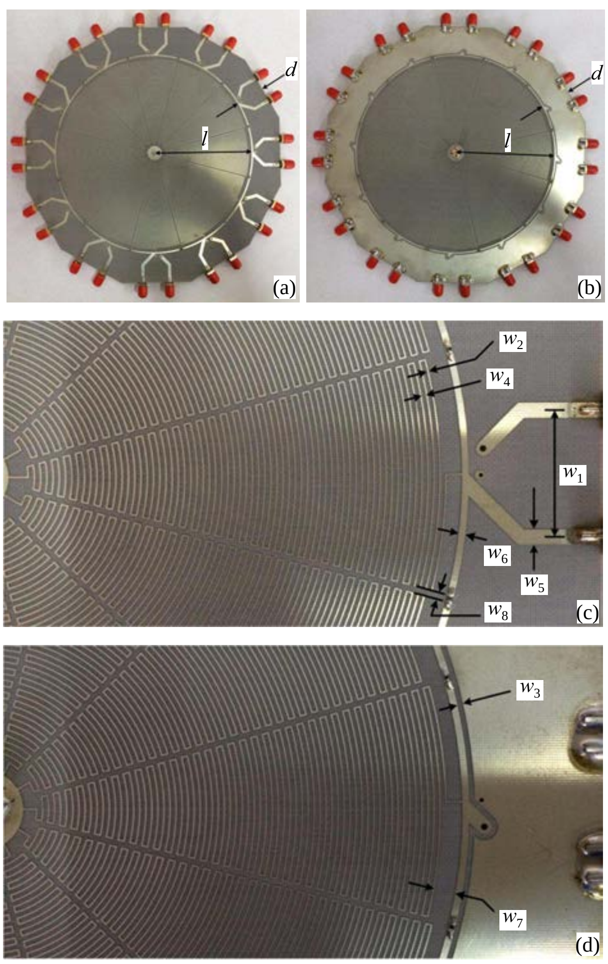

Fig. 7. Photographs of the developed demonstrator: (a) – front side. (b) – back side, (c) – Details of the front side, (d) – details of the back side

The differential outputs of this demonstrator are the microstrip lines. Fig. 6. Shows microstrip line based differential outputs. It is realized by transiting the transmission line of the back side to the front side with the use of vertical interconnections, as shown in Fig. 6.

4 Numerical calculations and experimental results

Based on the above analyses, the required characteristic impedance of the transformer for 12-pair differential outputs is $\sqrt{24}Z_0 \approx 244.949\,\Omega$. This corresponds to a line width of $w = 0.3$ mm on the substrate mentioned above, as plotted in Fig. 5. The $50-\Omega$ microstrip transmission lines are set as line width of 2.7 mm. Figure 7 shows the photographs of the developed demonstrator, the front and the backside.

The radially distributed transformers are meandered for miniaturization, as illustrated in Fig. 7(c). The centrally placed input port is connected with a coaxial cable, where circular disks with optimal radials at both front and back sides of the substrate were optimized for impedance matching and for assembling (soldering). All impedance transformers start with the circular disks. The isolation resistors are all commercially available values of $150\,\Omega$, as compared with the theoretical values of $139.05\,\Omega$. Thus, the theoretical results based on (2) to (4) would be $S_{ii} = 12.919$ dB, $S_{i,\,i+1} = 14.428$ dB, $S_{i,\,i+2} = 31.601$ dB, $(i = 2, \ldots, 13)$. When referred to Tab. 1, it is seen that, the output return losses are slightly degraded under the condition of $S_{22} = S_{23}$. The full-wave EM simulator, Ansoft HFSS, was used to perform the numerical calculations. With optimal simulations, it was found that the transmission-line pair of the isolation network has a length of $\theta_2 = 1.8\,^{\circ}$and line impedance of $Z_2 = 113.2\,\Omega$. It is seen θ_2 is small enough as compared with θ_1, thus confirming the approximate discussions presented above. Table 2 lists physical parameters when referring to Fig. 7.

Photographs of the fabricated demonstrator are shown in Figs. 7(a)-(d), the front and back sides as well as the details of the both. The measurements were carried out by using Agilent N9918A network analyzer. The simulation and experiment results are shown in Fig. 8. From the return losses for the input and output ports described in

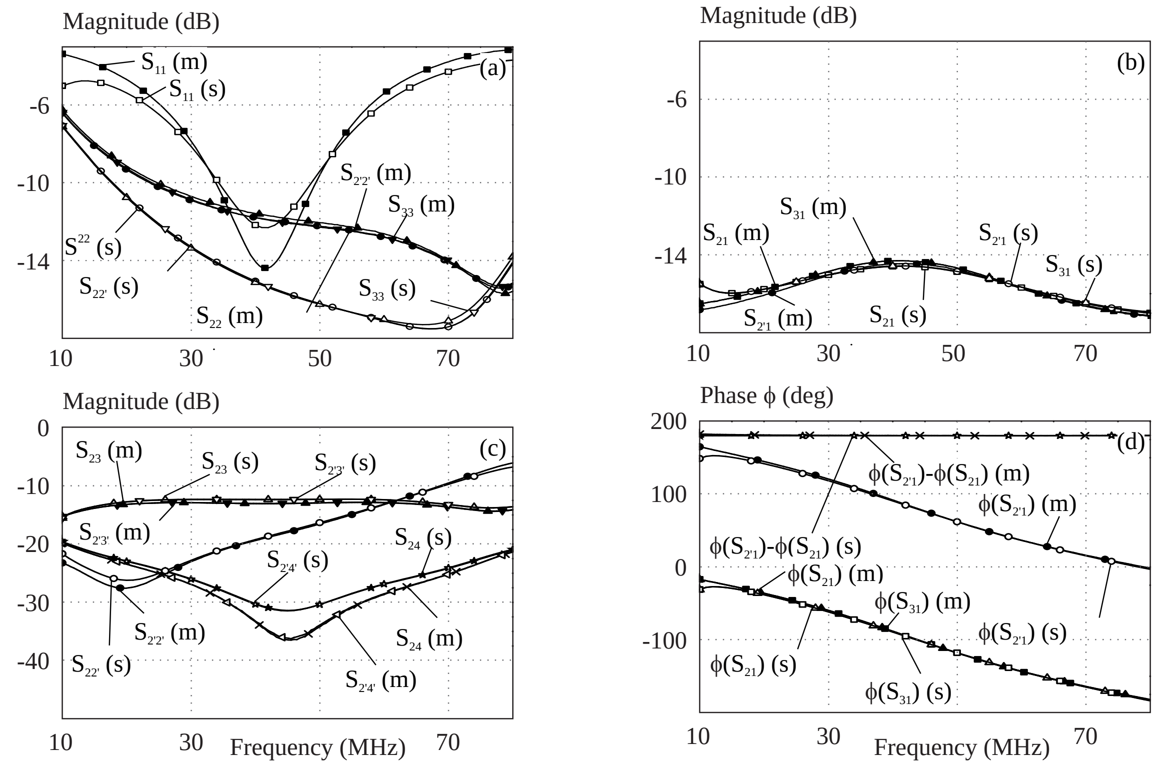

Fig. 8. Simulated (s) and measured (m) results of the demonstrator: (a) – return losses, (b) – insertion losses, (c) – port isolation, (d) – phase responses

Fig. 8(a), it can be seen that the power divider works at the center frequency of 41.6 MHz. Although the outputs are not well matched, the return losses are over 10 dB within a wide range to meet technical requirements for applications. At the center frequency shown in Fig. 8(b), measured insertion losses are approximately 14.3 dB compared with the theoretical data of 13.8 dB. The operation band is from 10 MHz to 80 MHz under a magnitude imbalance of ± 0.3 dB. As shown in Fig. 8(c), the isolations of the adjacent outputs, namely S_{23} or $S_{2'3'}$, are approximately 13.1 dB as compared with the theoretical values of 14.428 dB, while for S_{24} and $S_{2'4'}$, they are better than 34 dB. The isolations of the separated outputs could be further enhanced and not detailed here for brevity. From 10 MHz to approximately 60 MHz, the isolation of a differential pair, $S_{22'}$, is better than 13 dB with the best value being over 27 dB. Fig. 8(d) records the out-of-phase results. The range of 180° phase difference is from 10 MHz to 80 MHz in terms of an imbalance of $\pm 2.5\ ^\circ$. Compared with the previous work [17], measured results indicate that this kind of power divider can also achieve a wide band by using microstrip output interfaces, thus showing the flexibility and compatibility with different system applications.

Table 3 lists some reported power dividers and the proposed contribution for performance comparisons. Compared with other works, this demonstrator exhibits a relatively more out-of-phase outputs and a broad operation bandwidth. Meanwhile, the studied architecture is simple and easy to be integrated for system applications.

5 Conclusion

A multi-way differential power divider has been researched and a prototype developed in this paper. The out-of-phase power output was achieved using the double-sided parallel stripline and specific design approach has been provided. The output interfaces corresponding to the microstrip line were studied. A 12-pair differential output prototype with central frequency of 41.6 MHz was fabricated and measured. Experimental results are in good agreement with the numerical predictions (simulations). The developed differential power divider can be potentially applied to some industrial electronic systems for several applications.

Acknowledgments

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