Voltage mode electronically tunable full-wave rectifier

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The paper presents a new realization of bipolar full-wave rectifier of input sinusoidal signals, employing one MO-CCCII (multiple output current controlled current conveyor), a zero-crossing detector (ZCD), and one resistor connected to fixed potential. The circuit provides the operating frequency up to 10 MHz with increased linearity and precision in processing of input voltage signal, with a very low harmonic distortion. The errors related to the signal processing and errors bound were investigated and provided in the paper. The PSpice simulations are depicted and agree well with the theoretical anticipation. The maximum power consumption of the converter is approximately 2.83 mW, at ± 1.2 V supply voltages.

K e y w o r d s: multiple output current-controlled current conveyor, zero-crossing detector, full-wave rectifier, bipolar transistors, harmonic distortion

1 Introduction

Precision rectifiers are important building blocks for signal processing, conditioning and instrumentation of low-level signals and are extensively used in wattmeters, AC voltmeters, RF demodulators, linear function generators and various nonlinear analogue signal-processing circuits [1–3]. Owing to the threshold voltage of diodes, the conventional diode rectifiers are limited and are only used in specific applications, such as DC voltage supplies. However, simple diode rectifiers cannot be used for applications requiring accuracy in the threshold voltage range, the. This can be overcome by using high precision integrated circuit rectifiers.

Although the use of current-mode (CM) active devices is restricted to current processing, it offers certain advantages such as higher usable gain, more reduced voltage excursion at sensitive nodes, greater linearity, less power consumption, wider bandwidth, better accuracy and larger dynamic range compared to that of their voltage-mode counterparts. The CCII is a reported active component, especially suitable for the class of analog signal processing. However, the CCII can not control the parasitic resistance at x (R_x) port, so – when it is used in some circuits, it unavoidably requires certain external passive components, especially the resistors. This makes it inappropriate for IC implementation, as it occupies a greater chip area, high power dissipation and excludes electronic controllability. On the other hand, the recently introduced second-generation current controlled conveyor (CCCII) has the advantage of electronic adjustability over the CCII [4]. Also, the use of dual-output current-conveyors is found to be useful in the derivation of current-mode single input circuits.

The use of the current conveyor to improve performance of an OA-based circuit was discussed in [5]. Full-wave rectifiers based on a CMOS class AB amplifier and current rectifier operation are described in [6, 7]. This circuit offers a wide dynamic range and shows a broadband operation. CMOS integrated active rectifier concept is an innovative approach for higher efficiencies [8]. These rectifiers provide output voltages nearly at the level of the input voltage combined with low power consumption, which was also achieved through the circuit design proposed here. In [9], a single CCCII-based precision full-wave rectifier circuit is proposed using a three-output CCCII, two MOS transistors and a resistor with large cross-over distortion for a low frequency of 5 KHz. In [10, 11], full-wave rectifier circuits are proposed using two second-generation current conveyors (CCIIs) and four diodes.

In 2006, Yuce *et al* [12] proposed a full-wave rectifier deploying two plus-type second-generation current conveyors (CCII+s) and three n-channel metal-oxide semiconductor field-effect transistors (MOSFETs). Also, Minaei and Yuce [13] proposed a voltage-mode (VM) full-wave rectifier with high-input impedance using a dual-X second-generation current conveyor (DXCCII) and three n-channel MOSFETs in 2008. The circuits presented in [12, 13] require no passive components and they operate in VM. Some current-mode (CM) full-wave rectifiers have been reported in the literature [14–18]. However, the reported rectifiers usually employ at least two active elements and/or four diodes, and additional sub circuits. For example, in [15], the circuit uses two CCII+s and four diodes. The structure in [16] employs one current conveyor and one universal voltage conveyor (UVC) and two diodes. In [17], the proposed circuits employ at least two current and/or voltage conveyors as active elements and two diodes. A CM full-wave rectifier circuit employing one active element — namely current differencing transconductance amplifier (CDTA) — is reported in [18]. However, the circuit in [18] requires four diodes and one re-

Table 1. Comparison of the rectifiers

Reference	Type of active components	Number of diodes	Number of resistors	Auxiliary bias sources	Cascability property	Modes of operation
[2]	4 CCCIIs, 3 MOSFETs	–	–	yes	no	VM
[12]	2 CCIIs, 3MOSFETs	–	–	no	no	VM
[13]	1 DXCCII, 3 MOSFETs	–	–	yes	no	VM
[14]	2 Opamps	2	5	no	no	VM
[15]	2 CCIIs	4	2	no	no	VM
[16]	1 CCIIs, 1 UVCs	2	–	no	yes	CM
[17]	1 CCIIs, 1 UVCs	2	–	yes	yes	CM
[18]	1 CDTAs	4	1	no	no	CM
[20]	4 OTAs	-	–	yes	yes	CM
[22]	1 CDTAs	2	1	no	yes	CM
[23]	1 DXCCIIs	2	1	no	yes	CM
[24]	1 MYC-CDTA	–	–	no	no	CM
Proposed circuits	1 DOCCCIIs, ZCD, 2 MOSFETs	–	1	no	yes	VM
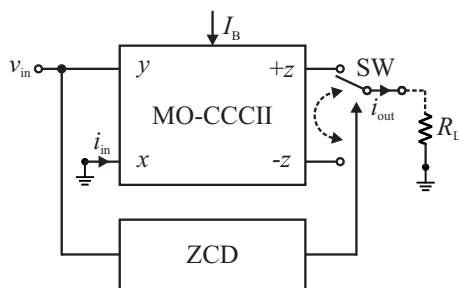
Fig. 1. The proposed circuit of the full-wave rectifier
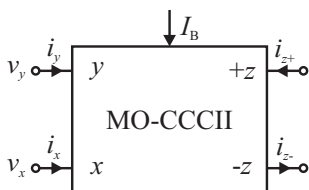
Fig. 2. Electrical symbol of MO-CCCII

sistor. Other rectifier examples can be found in [19–23]. The circuits reported in [19, 21] are designed based on MOS transistors. Although these circuits have fairly simple structures, the circuit in [19] requires a floating input voltage source and the circuit in [21] needs three external bias current sources which should be realised separately. The circuit in [20] employs an excessive number of OTAs as active elements and the circuits of [22, 23] use CDTA or DXCCII which have more complex internal structures with respect to CCII, OTA and DVCC. The circuit in [24] employs a current mode full-wave rectifier based on single modified Z-copy current difference transconductance amplifier (MZC-CDTA) and two switches.

This paper presents the principles of operation, and the detailed circuit design of the new bipolar realisation of the full-wave rectifier. The features of the proposed circuit are: it employs one MO-CCCII, one zero-crossing detector, and one resistor connected to source voltage, which

is suitable for fabrication in a monolithic chip. Unlike the rectifier described in [2, 3], which was realised using the CMOS technology, the one described in this paper involves a simpler and more accurate control structure. Besides, the proposed circuit does not require a more precise bias voltages realization and complex transistor pairing, which was typical of the realisations described in [2, 3]. The rectifier circuit provides the operating frequency of up to 10 MHz, with increased linearity and precision in processing of input signals. The performance of the proposed circuit is illustrated by PSpice simulations, showing a good agreement with the calculation. The circuits proposed in this work have been compared to similar circuits reported in the literature. The results are depicted in Table 1.

2 Proposed full-wave rectifier circuit

Figure 1 presents the proposed circuit of the full-wave rectifier.

Generally, a MO-CCCII is a multiple-terminal active building block, as shown in Fig. 1. The electrical symbol of the MO-CCCII is shown in Fig. 2.

The port relations of the MO-CCCII can be presented by

$$i_y = 0\,;\ v_x = v_y + i_x R_x\,;\ i_{z+} = +i_x\,;\ i_{z-} = -i_x\,. \quad (1)$$

The schematic bipolar realization is shown in Fig. 3 [25]. According to equation (1), the MO-CCCII has a unity voltage gain between terminal y and x and a unity current gain between terminal x and z. The R_x is an inner resistance of a translinear mixed loop (Q_1 to Q_4) with grounded resistor equivalent controlled by bias current I_B. In this case, the parasitic resistance R_x at the terminal x can be expressed by
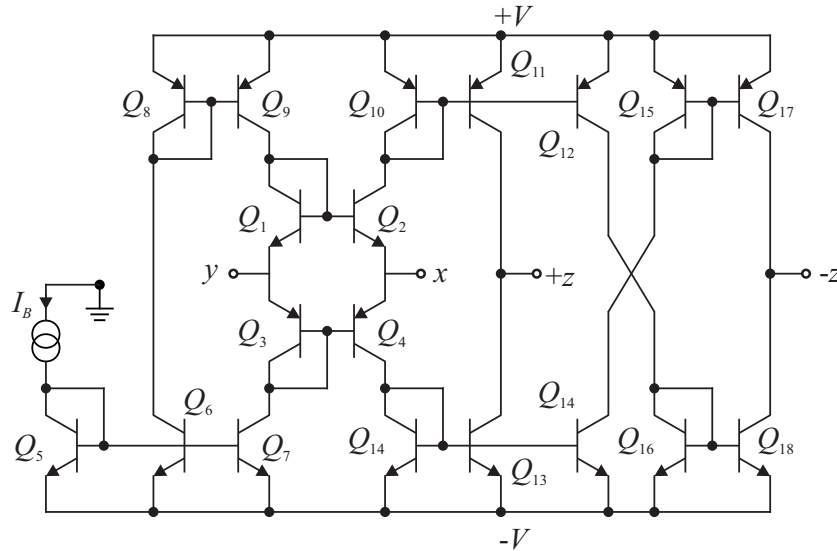
$$R_x = \frac{V_T}{2I_B} \quad (2)$$

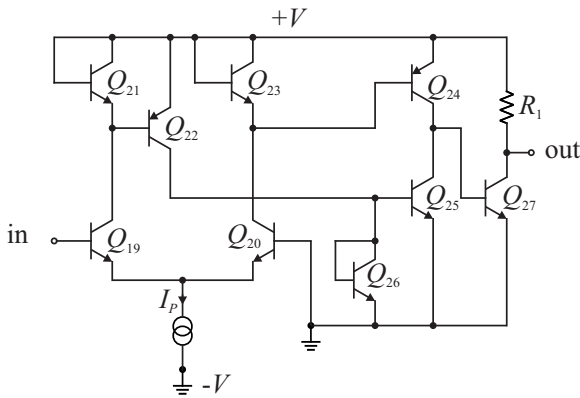**Fig. 3.** Bipolar realization of MO-CCCII

Fig. 4. Bipolar realization of comparator

where $V_T = 26$ mV at $27\,°$C is the usual thermal voltage given by kT/q, $k =$ Boltzmann's constant $= 1.38 \times 10^{-23}$ J/K, $T =$ the absolute temperature (in Kelvin's), and $q = 1.6 \times 10^{-19}$ C and I_B (Fig. 1) is the bias current of the conveyor which remains tunable over several decades.

Precision in processing of the input voltage signal is directly dependent on the manner in which ZCD is able to reliably detect the moment when the input signal changes the polarity. This required the construction of new bipolar detector circuits, as shown in Fig. 4. The transistors Q_{19} and Q_{20} will promptly follow the variations in input voltage, thus reducing the total delay time of the comparator. The resistor R_1 has one end attached to the source from which it is powered together with the detectors. The resistor can be coupled to the source of the different voltage level, if this should prove necessary due to the demands of analog switches-two complementary MOS transistors.

By the routine analysis of the proposed full-wave circuit shown in Fig. 1 and using the properties of MO-CCCII, for $v_{\text{in}} > 0$, the $z+$ current (v_{in}/R_x) to pass on to the load. For $v_{\text{in}} < 0$, $z-$ current ($-v\,in/R_x$) passes

on to the load, thus inverting the negative cycle of input

$$i_{\text{out}} = \begin{cases} i_{z+} = \frac{v_{\text{in}}}{R_x}, & v_{\text{in}}(t) \geq 0, \\ i_{z-} = -\frac{v_{\text{in}}}{R_x}, & v_{\text{in}}(t) \prec 0. \end{cases} \tag{3}$$

Unidirectional current flows through the load in either case, resulting in a full-wave rectified output.

Depending on the detected sign of the input signal (practically by detecting the negative half-period of input processing signal), over the ZCD (Fig. 1), the position of the switch SW (two complementary MOS transistors) can be determined. The control voltage signal, obtained on the output of the ZCD, defines the position of the switch SW and brings the current either from port $z+$, or from port $z-$ of the MO-CCCII. Such control enables the current input from the port $z+$ on the load at the interval at which the input voltage signal is positive, *ie* from the port $z-$ when the input voltage is negative. The output voltage v_{out} for input v_{in} is

$$v_{\text{out}} = \begin{cases} \frac{R_L}{R_{\text{in}}} v_{\text{in}}, & v_{\text{in}} \geq 0, \\ -\frac{R_L}{R_{\text{in}}} v_{\text{in}}, & v_{\text{in}} < 0. \end{cases} \tag{4}$$

where $R_{\text{in}} = R_x$. The equation (4) we can present in form

$$v_{\text{out}} = \frac{R_L}{R_{\text{in}}} |v_{\text{in}}|. \tag{5}$$

Based on (5), it is obvious that the voltage value at the output of the proposed circuit corresponds to the rectified value of the input sinusoid signal with amplification or rectifier with attenuation. In the proposed circuit, rectification is not performed by diodes, which implies fewer ripples, compared with the known diode rectifier circuits [14–18]. It is also possible to perform low-voltage (below threshold level of the diode) rectification using the proposed circuit.
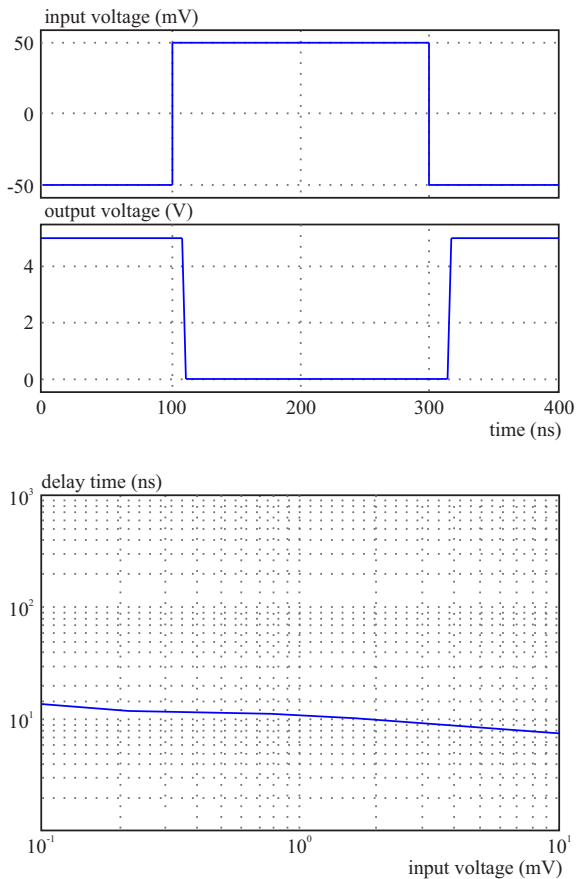
Fig. 5. (a) — Output voltage waveforms for proposed ZCD, (b) — Average delays time against input voltage
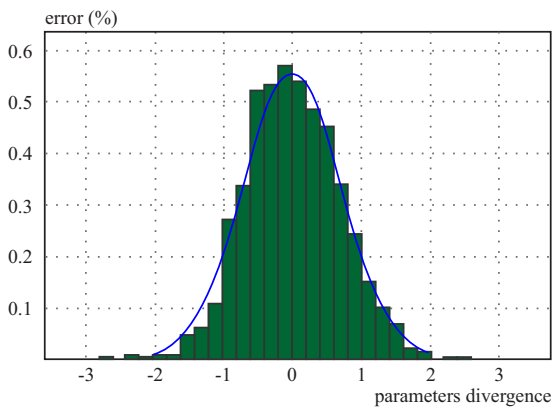

Fig. 6. The distribution of errors, for the divergence in the value of the parameters, from their nominal values

Non-ideal effects

The effects of MO-CCCII and comparator non-idealities on the full-wave rectifier performance are to be considered in this section. By considering the non-ideal MO-CCCII characteristics, (1) can be rewritten as

$$i_y = 0\,, \; v_x = \alpha v_y + i_x R_x\,, \; i_{z+} = +\beta_p i_x\,, \; i_{z-} = -\beta_n i_x$$
$$(6)$$

where $\alpha = 1 - \varepsilon_v$ and ε_v ($|\varepsilon_v| \ll 1$) represents the voltage tracking error from y to x terminal, $\beta_p = 1 - \varepsilon_p$ and ε_p ($|\varepsilon_p| \ll 1$) denotes the current tracking error from x to

$z+$ terminal, while $\beta_n = 1 - \varepsilon_n$ and ε_n ($|\varepsilon_n| \ll 1$) stands for the current tracking error from x to $z-$ terminal of the MO-CCCII, respectively. Generally, these tracking factors remain constant and frequency independent in low to medium frequency ranges. The typical values of the non-ideal current transfer gains and the transconductance inaccuracy factor α, β_p and β_n, range from 0.9 to 1, with an ideal value of 1. However, at higher frequencies these tracking factors become frequency dependent. Given the non-idealities, currents generated from MO-CCCII can be defined as

$$I'_{\text{out}} = i_{z-} - i_{z+} = (\beta_p - \beta_n)\frac{\alpha v_{\text{in}}}{R_{\text{in}}} =$$

$$\begin{cases} 2\beta_p \frac{\alpha v_{\text{in}}}{V_T} I_B = 2\beta_p q \frac{\alpha v_{\text{in}}}{kT} I_B\,, & v_{\text{in}}(t) \geq 0 \\ -2\beta_n \frac{\alpha v_{\text{in}}}{V_T} I_B = -2\beta_n q \frac{\alpha v_{\text{in}}}{kT} I_B\,, & v_{\text{in}}(t) \prec 0 \end{cases} \quad (7)$$

which results in an absolute error

$$Error = |i_{\text{out}} - I'_{\text{out}}|\,. \qquad (8)$$

The error (8) is a function of input voltage signals and varies depending on its contents. A way to express the error is to consider the values of the observed parameters as random quantities characterized by their PDFs (Probability Density Function). Therefore, the interval having a 2ε width, around the nominal value of the observed parameters needs to be defined and associated with a certain distribution, *eg* uniform distribution.

From (7), the tracking errors slightly change the output current of the proposed full-wave circuits. However, the above relation does not include the error in determination of the interval in which the input voltage signal is negative (the ZCD error), which also defines the precision of the proposed rectification process. Figure 5a shows the waveform of the output voltage in response to an input voltage step of $\pm 50\,\text{mV}$ for the proposed comparator. In Fig. 5b, the average delay times of the proposed comparator as a function of the input voltage amplitude is reported. As can be seen, at low input voltages, the response time of the proposed circuit is very small. As the input voltage is increased, the delay time are reduced, since the enhanced output voltage swing (due to the higher voltage values) cause Q_{19} and Q_{20} completely turn-off.

Simulation results confirm the fact that proposed ZCD circuits is capable of processing the input signal with a high precision. We suppose that the incremental sensitivities of the output current i_{out} at parameters α, β_p, β_n and T are: 1; 1; 1 and -1 (all the active and passive sensitivities are of an equal unity in magnitude). Thus, the proposed circuit exhibits a low sensitivity performance.

The Monte Carlo approach [26] gives the lower and upper limits of interval which contains 95 % of error samples. The Monte Carlo analysis in PSpice was used for simulations with a given error on different parameters and components (Monte Carlo predicts the behaviour of a circuit statistically when part values are varied within their tolerance range for 5 %), Fig. 6. This test is very useful for visualizing how the circuit will run with imperfect parameters as are used in reality. The number of individual simulation was 2000.

Table 2. PR200N and NP200N transistor parameters

NP200N
.MODEL NX2 NPN RB = 262.5 IRB = 0 RBM = 12.5 RC = 25 RE = 0.5 IS = 242E − 18 EG = 1.206 XTI = 2 XTB= 1.538 BF = 137.5 IKF = 13.94E − 3 NF = 1.0 VAF = 159.4 ISE = 72E − 16 NE = 1.713 BR = 0.7258 IKR = 4.396E − 3 NR = 1.0 VAR = 10.73 ISC = 0 NC = 2 + TF = 0.425E − 9 TR = 0.425E − 8 CJE = 0.428E − 12 VJE = 0.5 MJE = 0.28 CJC = 1.97E − 13 VJC = 0.5 MJC = 0.3 XCJC = 0.065 CJS = 1.17E − 12 VJS = 0.64 MJS = 0.4 FC = 0.5

PR200N
.MODEL PX2 PNP RB = 163.5 IRB = 0 RBM = 12.27 RC = 25 RE = 1.5 IS = 147E − 18 EG = 1.206 XTI = 1.7 XTB = 1.866 BF = 110.0 IKF = 4.718E − 3 NF = 1 VAF = 51.8 ISE = 50.2E − 16 NE = 1.65 BR = 0.4745 IKR = 12.96E − 3 NR = 1 VAR = 9.96 ISC = 0 NC = 2 TF = 0.610E − 9 TR = 0.610E − 8 CJE = 0.36E − 12 VJE = 0.5 MJE = 0.28 CJC = 0.328E − 12 VJC = 0.8 MJC = 0.4 XCJC = 0.074 CJS = 1.39E − 12 VJS = 0.55 MJS = 0.35 FC = 0.5
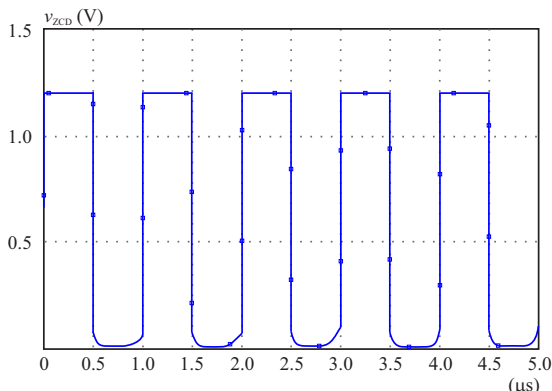

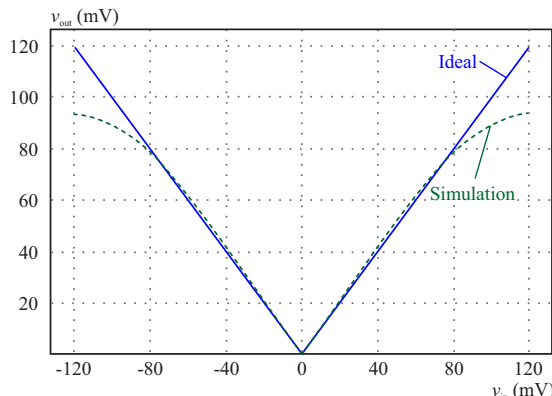**Fig. 7.** Time-domain response of proposed ZCD

Fig. 8. DC transfer characteristics for the proposed rectifier circuit

3 Simulation results

To confirm the given theoretical analysis, the proposed voltage-mode bipolar full-wave circuit in Fig. 1 was simulated using the PSpice program. The MO-CCCII and ZCD were realized by the schematic bipolar implementations given in Figs. 3 and 4, with the transistor model parameters of PR200N (PNP) and NP200N (NPN) of the bipolar arrays ALA400 from AT&T [27], Tab. 2. The supply voltages and the values of the bias currents were $+V = -V = 1.2\,\text{V}$ and $I_P = 300\,\mu\text{A}$ respectively, whereas the input voltage was within the range of $\pm100\,\text{mV}$. Parameters of National Semiconductor bipolar circuits AH510 [28] were used as analogue current switch during simulation.

Time response of the proposed ZCD circuits is shown in Fig. 7, where the input voltage signal was with 1 MHz frequency and 20 mV peak. Resistor $R_1 = 1\,\text{k}\Omega$ was used in the process of simulation. It is clear that the proposed solution detectors perform detection polarity of the input voltage signal in a very precise way, and the error that is due to imprecision in detection can be neglected in practical applications.

The DC characteristic of the proposed circuit for a frequency of 100 kHz is shown in Fig. 8. Based on Fig. 8, it can be concluded that the proposed circuit retains a linear character in a wide voltage range.

Figure 9 shows the wave form of the signal at the output of the circuit shown in Fig. 1 (voltage v_{out}), at different frequencies. For these simulations, the input signal
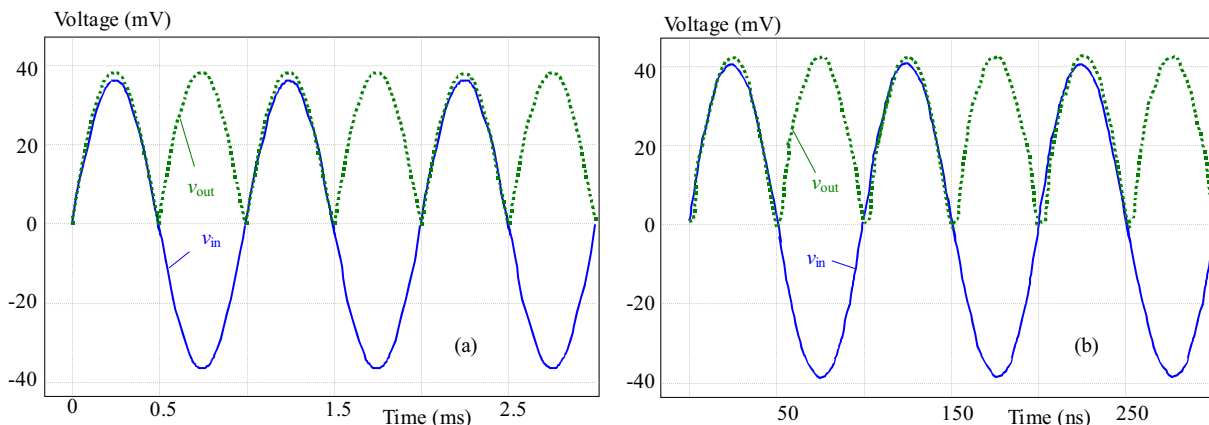

Fig. 9. Time-domain response of the proposed full-wave rectifier for different frequencies of (a) — 1 kHz and (b) — 10 MHz
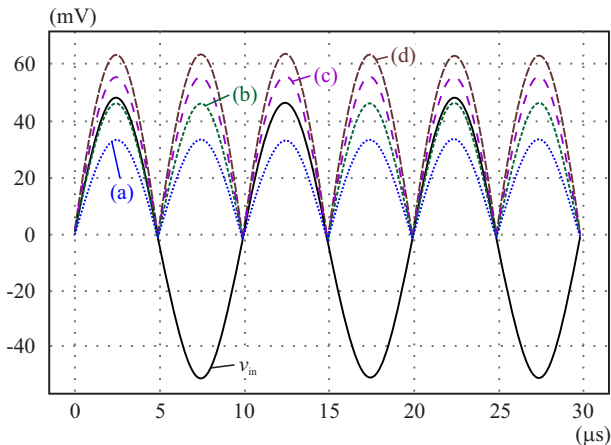
Fig. 10. Tunability of the gain of the proposed rectifier with changing the bias current I_B (a) — $I_B = 200\,\mu A$, (b) — $I_B = 130\,\mu A$, (c) — $I_B = 115\,\mu A$, (d) — $I_B = 100\,\mu A$

Fig. 11. Total harmonic distortion (THD) versus frequency at input amplitude voltage of 50 mV

is taken as a sinusoidal voltage signal with 40 mV peak value and different frequencies of 1 kHz and 10 MHz are selected. Figure 9 shows that the output waveform of the proposed rectifier is in a good agreement with the theoretical ones at low and high frequencies. However, with the increased frequency of the processed signal, the deviations are increased as well.

The total power dissipation was 2.83 mW. Small power consumption of the proposed circuits occurs due to the application of low-voltage current mode and transconductance mode integrated circuits, along with the use of bipolar transistor technique. Applying the current mode signal processing to solve the issues under consideration is a sensible approach to the problem. However, similar and sometimes lower power consumption can be achieved using CMOS technology instead of the bipolar one.

To test the tunability of the gain of the proposed rectifier circuit, the bias current of the MO-CCCI (I_B) is changed and the results are shown in Fig. 10. For these simulations, the input signal is taken as a sinusoidal voltage signal with 100 kHz frequency and 50 mV peak value, while the load was $R_L = 100\,\Omega$.

Harmonic Distortion

A further indication of the performance of each of the full-wave rectifiers can be gleaned by examining the distortion already present in a full-wave rectified signal. When a sinusoidal signal of frequency f is applied to a full-wave rectifier, the steady-state response at the output ideally consists of harmonic components at $2f$, $4f$, $6f$, *etc.* The harmonics in the signal causes the distortion in the output of the circuit. Because of its periodic nature, these harmonic components can be analyzed by the Fourier series. The magnitude of each harmonic of a waveform as shown in Fig. 11 is obtained with fast Fourier transform using PSpice.

The total harmonic distortion, or THD, of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all
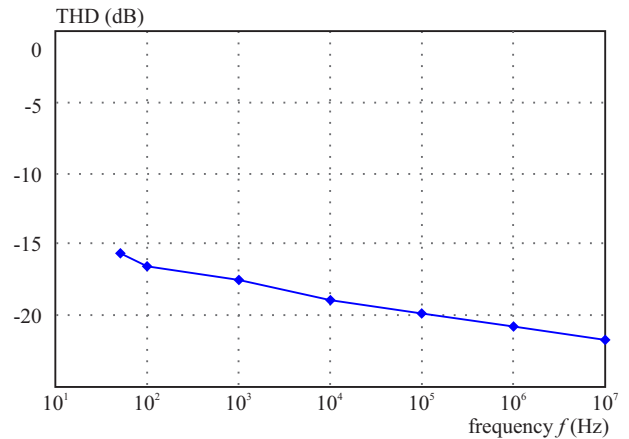
harmonic components to the power of the fundamental frequency

$$THD(\text{dB}) = 20\log(V_{THD})\,,\ V_{THD} = \sqrt{\frac{\sum_{n=2}^{N} V_n^2}{V_1^2}} \quad (9)$$

where V_1 is the fundamental frequency voltage content, V_n is nth the harmonic voltage content, and $n = 2, 3, 4, \ldots$. In the case of a full-wave rectifier, the steady-state response at the output consists of even harmonics.

Figure 11 shows the total harmonic distortion of the output voltage of the proposed circuit, Fig. 1. The THD of the proposed circuit is -15.6 dB at 50 Hz and -20.8 dB at 1 MHz with an input signal of 50 mV. The THD is significantly lower than in [2, 29, 30] (the THD of previously reported circuit slowly increases with frequency), because for higher frequency ranges, the switching ON and OFF of diodes becomes sluggish due to its higher impendence and more distortions.

4 Conclusions

In this paper, new full-wave rectifier topologies are given. The circuit employs only two active component and one resistor which is advantageous from the integration point of view and operates in VM. The workability of the proposed circuits is demonstrated by PSpice simulations using the bipolar arrays ALA400 from AT&T technology parameters. The effects of the non-idealities of the active elements are also investigated. The proposed circuit has a high precision, low power consumption and wide bandwidth.

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