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COMMUNICATIONS

ONE WAY OF OUTPUT VOLTAGE HOLD CIRCUIT IMPROVEMENT AT LOW RESISTANCE COMPARATOR

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The article presents a way of improvement the important performances of an electronic low resistance comparator. The practical usage of a realized instrument prototype shows some disadvantages: the time until the result appears at the display is to long (the stationary state establishing sequence should be shorter) because of the negative influence of parasitic voltages. Modification of output voltage hold circuit gives quite convenient instrument response time. The parasitic voltage disturbance is decreased to acceptable value, even though the comparator is modified for multirange measurement. The paper describes some details of a solution and its conformation in practical usage.

K e y w o r d s: low resistance comparator, output voltage hold circuit, establishing sequence

1 INTRODUCTION

The authors designed and realized an electronic low resistance comparator. That instrument uses the same amplifier to amplify both voltages: at the ends of referent resistor, and at the measuring one as well [1]. The multiplexer is applied to separate those voltages at the amplifier input. The amplified output voltages are demultiplexed and lead to two A/D converter inputs (U_R to refferent input and U_X to measuring one). It could be also an instrument with comparasion capability [2, 3]. Figure 1 shows the multiplexer and output voltages (U_R and U_X at referent and measuring resistors R_R and R_X, respectively) [4].

The generated voltages are lead to appropriate capacitors of hold circuit and should be stabile during the measuring periods. The instrument measuring cycle consists of 10 steps, Fig. 2. One step of measuring cycle takes $T = 20$ ms, and equals to power network time period. The measuring cycle time is 0.2 s and ordering of unique operation is shown in Fig. 2. Measuring current is switched off in first 4 steps (80 ms), and on in following 6 steps (120 ms), [4]. The duration of both input voltages is 40 ms each, and than the pause of 160 ms is beginning. In that time periods the voltages have to be conducted to the outputs as fast as possible with minimal errors. It means that the capacitor discharging current has to be too small. Technical data fir IC LTC1050 guaranties polarizations (bias) current about 10 pA. But, the imperfect analog switches and the current leak on the printed circuit board can increase that current many times [5].

To reach the declared (wanted) measuring precision, the output voltages have to be established with errors of about 1 ppm. Assuming the exponential voltage growing at the capacitors, there is a need of 15 relative time constants to reach the stabile stationary state (ramp-up time). In our case, with component values of: $R = 180\,\mathrm{k\Omega}$, and $C = 1\,\mu\mathrm{F}$, the time constant is $T = 0.18$ s. The capacitor charge takes 2 of 10 measuring steps and the process is 5 times slower and the effective time constant is about 1 s. It implies the stationary state achievement time of 15 seconds. It is too long and has to be shorted.

The power network AC parasitic voltage (50 Hz) makes also the problems by measuring. In the time intervals while the analog switches are on, part of this voltage is carried to the capacitors and caused the waves on output voltage. In the original circuit (Fig. 1) that voltage can produce a DC component provoking a systematic measuring error. The charge injection effect makes the instrument performances worse [6]. The proposed improvement of previous circuit reduces the current leak to acceptable level.

2 PROPOSED SOLUTION FOR IMPROVEMENT OF OUTPUT VOLTAGE HOLD CIRCUIT

The redesign of output voltage hold circuit is done, to overcome the described problems and to make the instrument performances better. The functional principles of the new hold circuit are illustrated and can be explained using Fig. 3.

The integrated circuit IC1, resistor R_1 and capacitor C_1 make the first integrator. The IC2 is copper stabilized circuit with very small offset voltage (about $1\,\mu\mathrm{V}$) and

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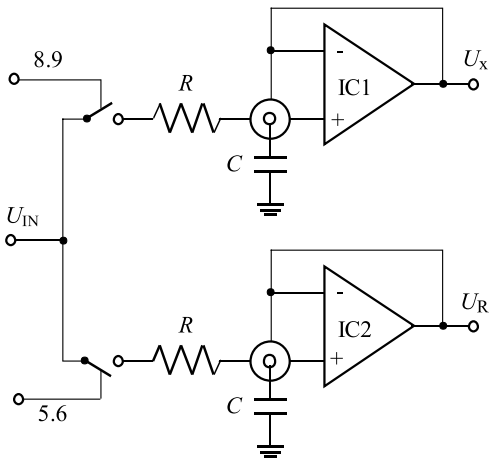

Fig. 1. The output demultiplexer and voltage hold circuits

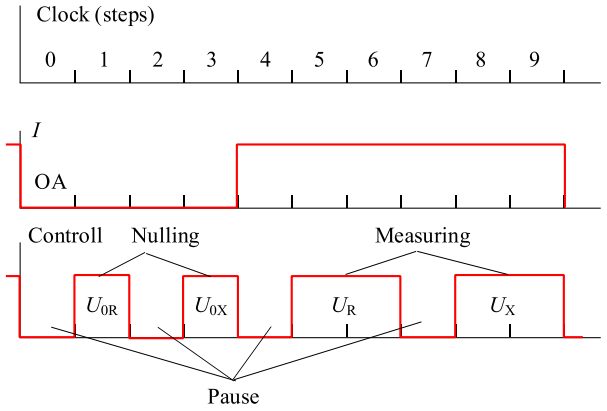

Fig. 2. The measuring cycle timing diagram

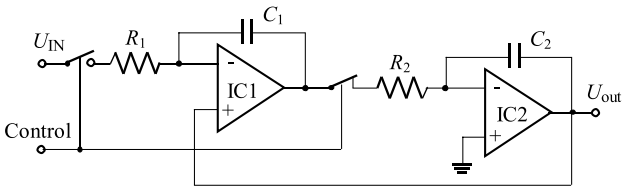

Fig. 3. The new output voltage hold circuit

also small polarization (bias) current (about 10 pA). Together with resistor R_2 and capacitor C_2 it builds the second (output) integrator, which makes a feedback. Its input voltage offset is not critical, but for slower capacitor C_2 discharging, it is necessary its polarization current to be small (below 100 pA). The amplified measuring voltage U_{IN} that is originated on resistors (R_R or R_X), without parasitic voltage components, is lead to the input of that circuit. The circuit operates on the following way. Assume that all of capacitors are discharged before instrument switched on; initial state. At the start, in first measuring interval, the output voltage equals to the IC2 offset voltage, U_{Offset2}. The integration takes two controller steps ($2T = 40$ ms). After integration time the input voltage at capacitor C_1 reaches value of

$$U_{\mathrm{Int1}} = -\frac{1}{R_1}C_1\int_0^{2T}\left(U_{\mathrm{IN}} - U_{\mathrm{offset2}}\right)\mathrm{d}t = -\frac{2T}{R_1}C_1\left(U_{\mathrm{IN}} - U_{\mathrm{offset2}}\right) \quad (1)$$

where T is integration period, one step ($T = 20$ ms). When integration completes the input switch becomes off and input one, on. Now the second operational amplifier (OP) runs as an integrator and raises its voltage until the output voltage of first integrator becomes equal to the input offset voltage of second OP, U_{offset2}. At that point the second integrator output voltage equals $-U_{\mathrm{Out1}}$.

$$U_{\mathrm{Out1}} = -U_{\mathrm{Int1}} + U_{\mathrm{offset2}}\,. \quad (2)$$

Expressions (1) and (2) give the next relations

$$U_{\mathrm{Out1}} = \frac{2T}{R_1C_1}\left(U_{\mathrm{IN}} - U_{\mathrm{offset2}}\right) + U_{\mathrm{offset2}}\,, \quad (3)$$

$$U_{\mathrm{Out1}} = \frac{2T}{R_1C_1}U_{\mathrm{IN}} + \left(1 - \frac{2T}{R_1C_1}\right)U_{\mathrm{offset2}}\,. \quad (4)$$

Choosing the resistor and capacitor values so to satisfy equitation $R_1C_1 = 2T$, the last expression becomes simply

$$U_{\mathrm{Out1}} = U_{\mathrm{IN}}\,. \quad (5)$$

It means that the output voltage reaches the true value, already after the end of the first measuring cycle (200 ms) and it is independent of output amplifier (IC2) offset voltage. Because $T = 20$ ms, the time constant should be $R_1C_1 = 40$ ms ($R_1 = 20\,\mathrm{k\Omega}$, and $C_1 = 2\,\mu\mathrm{F}$, for example). The small difference of values above does not make the instrument ramp-up time significant longer. But, if the standard components values are in a question, the additional adjustment (tuning) is needed.

If the time constant is not exactly equal to 40 ms, after the first measuring cycle remains some difference between those two voltages $U_{\mathrm{IN}}U_{\mathrm{Out1}}$ (10% for example). In the next measuring cycle that voltage (difference) is integrated and added to previous voltage, and the new difference should be now about 1%. The difference is decreasing in next cycles, and the output voltage becomes successive better. On that way the difference between input and output voltage of 1 ppm could be reached after 6 measuring cycles, 1.2 s ($6 \times 0.2\,\mathrm{s} = 1.2\,\mathrm{s}$). It is necessary to emphasize that the input offset voltage of second OP das not influence on the measuring error. Because the output voltage accuracy is defined by first OP offset voltage, this offset voltage has to be as small as possible. In realized comparator as first OP LTC1050 (Liner Technology) IC is used with offset voltage of about $1\,\mu\mathrm{V}$. By the maximal output voltage of 5 V, in the stationary state the error is about 0.2 ppm.

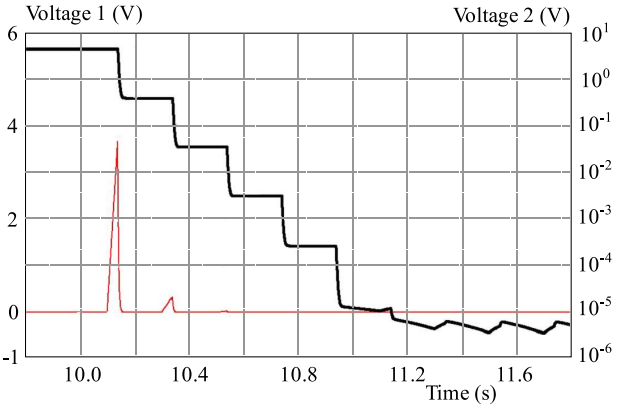

Fig. 4. The diagram of stationary state establishment simulation

3 VALIDATION OF PROPOSED METHOD

Having above in mind, one simulation was done (Fig. 4), because it was not being possible to scope the real process by available ordinary instruments. The voltage transition from 4 to 0 Volts was simulated and the result, as a diagram is presented in Fig. 4. The instrument is build of next values of components: $R_1 = 20\,\mathrm{k\Omega}$? $C_1 = 2\,\mu\mathrm{F}$ $R_2 = 3.3\,\mathrm{k\Omega}$, $C_2 = 1\,\mu\mathrm{F}$, but for better presentation of stationary state achievement in simulation, for resistance R_1 10% greater value is taken ($R_1 = 22\,\mathrm{k\Omega}$?and $R_1C_1 = 0.044$ instead of 0.040 s). The simulation includes a parasitic AC voltage of 5 mV and 50 Hz, as well. Figure 4 shows the tenth second of measuring cycle, when the input voltage drops from 4 V to zero.

The red thin line (Voltage 1) is IC1 output, and the black bold line (Voltage 2) is the end output voltage. Voltage 2 is presented in logarithmic scale to be easily noticeable. But, to show it as a positive logarithmic function it was necessary to add an offset of $5\,\mu\mathrm{V}$, as it could be seen.

The controller clock is synchronized with power network frequency and the integration takes integer number of periods (two of them) and means values of voltage and its harmonics, as a consequence of network current, equals zero. In real case those signals are so small and could not be seen and recorded by ordinary scope. The simulation results confirm assumption, as it was expected.

But, instrument function in practice shows the different results. It takes 3 s to reach 30 ppm difference of final voltage. After that time, it needs about 15 s for 15 ppm difference, more than 30 s for 3 ppm and 60 seconds for difference of 1 ppm (experimentally results). The establishment of stationary state on digital display is now in question. The output hold circuit, annulations circuit and A/D converter must be consider as well [7].

The slow stationary state achievement (inside area of 10 ppm) probably is caused by imperfection of dielectric in memory capacitors as a consequence of absorption. Paper, polyester and similar capacitors have significant absorption coefficient and it slows the establishing process. The polypropylene capacitors are the best [8], but not available at the moment. The next experiment will be done with some of them.

4 CONCLUSIONS

There are several instruments that use similar measurement method to one presented in the paper (HP 3458 System Multimeter, Keithley 81/2-digit Model 2002 High Performance Digital Multimeters [3]), [9]. However, the measurement scale of those instruments is significantly less than above proposed. Mentioned instrumentation method is usually used in the Laboratories where high precision of metal resistances is required and is necessary for determining its elementary characteristics [10]. Very high accuracy in resistance comparison and measurement is achieved (0.08 ppm for 1 000 independent measurement attempts and 0.26 ppm for 100 attempts) [4]. The realized instrument is working as a prototype in a laboratory at Copper Instuitute in Bor at this moment. There is an intention of integrating it into standard operative laboratory equipment for a new materials resistance and conductivity measerment. All experiments were performed at the Department of Electrical Measuring of the Faculty of Technical Sciences in Novi Sad and the official institution in Belgrade confirms the results.

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