JOURNAL OF APPLIED ENGINEERING SCIENCES
ISSN: 2247-3769 / e-ISSN: 2284-7197
sciendo
VOL. 9(22), ISSUE 2/2019
ART.NO. 269 pp. 169-176

DESIGN AN IMPROVED STRUCTURE FOR 10-BIT PIPELINE ANALOG TO DIGITAL CONVERTER BASED ON 0.18µM CMOS TECHNOLOGY

REZAPOUR Arash [a], SETOUDEH Farbod [b, *], TAVAKOLI Mohammad Bagher [a]

[a] Islamic Azad University, Arak Branch, Faculty of Electrical Engineering, Arak, Iran, e-mails: arash.rezapour@gmail.com, m-tavakoli@iau-arak.ac.ir
[b*] Arak University of Technology, Faculty of Electrical Engineering, Arak, Iran, e-mail: f.setoudeh@arakut.ac.ir

Received: 21.06.2019 / Accepted: 06.09.2019/ Revised: 10.10.2019 / Available online: 10.12.2019

DOI: 10.2478/jaes-2019-0023

KEY WORDS: Analog to Digital Pipeline, Comparator, Amplifiers, Buffer.

ABSTRACT:

This paper proposed a novel structure of a 10-bit, 400MS/s pipelined analog to digital convertor using 0.18 µm TSMC technology. In this paper, two stages are used to converter design and a new method is proposed to increase the speed of the pipeline analog to digital convertor. For this purpose, the amplifier is not used at the first stage and the buffer is used for data transfer to the second stage, in the second stage an amplifier circuit with accurate gain of 8 that is open loop with a new structure was used to speed up, also the design is such that the first 4 bits are extracted simultaneously with sampling. On the other hand, in this structure, since in the first stage the information is not amplified and transferred to the second stage, the accuracy of the comparator circuit should be high, therefore a new structure is proposed to design a comparator circuit that can detect unwanted offsets and eliminate them without delay, and thus can detect the smallest differences in input voltage. The proposed analog to digital convertor was designed with a resolution of 10 bits and a speed of 400MS/s, with the total power consumption 74.3mW using power supply of 1.8v.

1. INTRODUCTION

Today Analog signals have been replaced by digital signals. Analog-to-digital convertor (ADC) plays a key role in today's modern telecommunications (Fatemi-Behbahani, et al., 2016, Lv, et al., 2018, Murshed, et al., 2018, Rezapour, et al., 2019). The ADC operation is such that the continuous range of the analogue input signal is divided into several sub-ranges and each one of them has a digital code assigned. After the sample is obtained from the input analog signal, this sample is compared with the steps previously defined. Based on this comparison, it has been determined that the value of the input signal of the sample corresponds to the steps. The digital code for that step determines the output of the convertor. The comparator is the basic block of ADC. The comparator has the task of detecting a large or small sampled signal relative to the value of each step (Cárdenas-Olaya, et al., 2017, Correia, et al., 2015, de Aguilar, et al., 2016, Khorami and Sharifkhani, 2016, Kiran, et al., 2016, Prakash, et al., 2017, Steensgaard-Madsen, 2016). Many studies have been done to design and manufacture ADC. This structures has weaknesses and strengths that make them specific to a particular application. The fastest structure between analog-to-digital structures is the flash convertor. The structure of the flash convertor is conceptually very simple, this convertor works in a completely parallel way. Generally an n-bit flash convertor has 2^{n-1}comparator and same reference voltage for comparison. In the flash convertor structure a reference voltage in this structure is divided into n parallel part and for comparison placed beside n comparators (Khalapure, et al., 2017, Liu, et al., 2017, Sarkar, et al., 2017). As a result, the output of all comparators whose reference voltage is smaller than the sampled signal is one, and vice versa the output of all comparators whose reference voltage is larger than the sampled signal is zero. Hence, these structures are not actually used to build 10-bit convertor s because they cost more and require high power consumption and more space. Another structure used is the Two Step flash convertor. The basic block of this convertor is the same type of flash convertor. This structure is made up of two successive flash memory modules (Adimulam, et al., 2017, Liu, et al., 2010, Ozeki, et al., 2017). On the one hand, each stage has a number of sub-stages, which reduces the number of comparators and reduces power consumption, but it should be noted that they require more time to reach the end. As a result, we can create a swap between time and power. The Successive Approximation (SAR) convertor is one of the Subranging subgraphs that uses a digital to analog convertor to approximate, since it generates an analog signal using this convertor (DAC) (Ali, et al., 2014, Boo, et al., 2015, Wang, et al., 2017). By setting the digital-to-analog convertor, a digital code that represents the input analog value is created as long as its output is same with the input sample. An SAR convertor only includes a Sample and Hold circuit, an analog-to-digital convertor and a digital processor that controls it (Roy and Banerjee, 2018, Wang, et al., 2018). The speed of this structure is much less than the Pipeline because all the output bits must be generated before the new signal is sampled in the input. A serial convertor is one of the simplest existing structures that use a counter and comparator to generate digital code. In this structure, the counters begin counting from zero, and continue until the

* Corresponding Author: Setoudeh Farbod, e-mail: f.setoudeh@arakut.ac.ir

Ramp signal generated from the sampled input signal is larger. At this moment, the counter is equal to the digitized input value. Due to the expressed structures, it is necessary to have a structure that has very high speed and acceptable power consumption. This study is divided into 4 sections. In Section 1, the block diagram of the proposed pipeline convertor is presented, and in the second section, the design of various ADC convertor circuits is examined. In Section 3, the simulation results of different blocks are presented and finally in Section 4, a general comparison is made between the proposed design and several references published in recent years.

2. SPATIAL RANGE

Since the pipeline ADC is suitable for applications that require high precision and high bandwidth (Fan, et al., 2017, Li and Du, 2017, Tao, 2015, Vyas, 2013). Given that the present study tends to determine an ADC design with sampling speed of 400MS/s and due to the high speed of information conversion and the use of a channel to reach the target (parallelization is not working), the pipeline structure is used. According to the studies conducted, it is necessary to have an extremely low power and very fast processing speed ADC. Also, the proposed design must occupy the lowest area and can provide a trade-off between speed and power consumption, to open the designer's hand for various applications. The general proposed block diagram is shown in Figure 1.

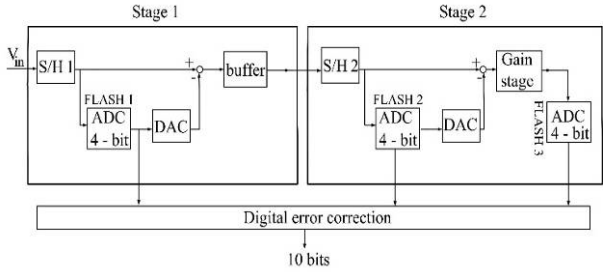

Figure 1. Block diagram of the proposed 10-bit pipeline A/D convertor

Since in pipeline analog to digital convertor is disappears about half of conversion time in the amplifier, So As shown in Figure1, on the stage1 is not used the amplifier, Instead, it used buffer, That's an advantage and makes the power consumption decreases and the convertor speed increases, but the circuit of the buffer must have a high precision and high speed, So that it can transfer data quickly to the next stage. Therefore on the stage2, the comparator's performance will be very difficult because the signal reached to this stage is not amplified, comparator must be able to eliminate unwanted offsets and detect the smallest amount of input In other words, the comparator should be very precise and it have to can recognize difference between very small voltages. Also an open loop amplifier is designed to further increase the convertor speed at stage 2. A new error correction circuit was designed for the Ring Counter. Since it is necessary for a 10-bit pipeline analog to digital convertor to have the S/H circuit having a minimum accuracy of 11 bits. Therefore, the S/H circuit designed has a precision above 11 bits. In the proposed structure, most of the circuits have been innovated, and as much as possible, extra bits of the input data are extracted. The total time available for each conversion is 2.5 ns, with duration of 1 ns divided into S/H. This is shown in Figure 2.

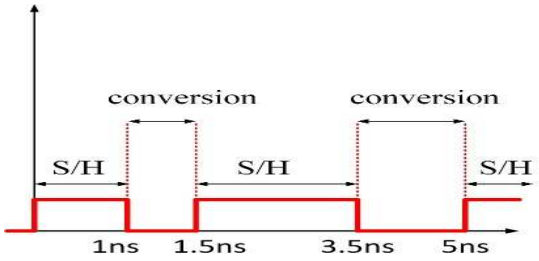

Figure 2. Allocations of scheduling to the proposed convertor

3. BLOCK CIRCUIT DESIGN

3.1. Comparator

After sampling the input information in the Flash convertor, comparators are needed to compare the input information with different voltage levels and make the corresponding binary output corresponds to it. As soon as the differential circuit name comes up, this circuit amplifies the difference between two signals; therefore, it seems logical that a comparator can be made using a differential amplifier. One of the important design problems is the lack of full compliance with the elements used in these circuits so that the input information can be detected incorrectly. Another issue faced in the design of comparator is the limited gain of the circuit. This problem reveals its impact when there is little difference between input information and reference information. When this difference is low, the output signal is also small and cannot be detected. To compensate for this problem, we use a latch class in the comparator circuit output so that we can make even the small signal in the output of the circuit to convey identified information to the next digital block. This structure is shown in Figure 3.

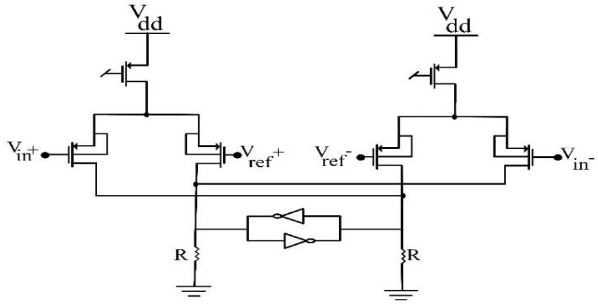

Figure 3. The first Proposed Comparator Structure

Also, we put a switch on the two ends of the Latch output. So, by the time we want to identify the information, first, by closing this switch, the previous information must have been cleared in a word and the Latch circuit can work properly. After putting Latch on the output, we are faced with the problem of Kick back noise. In cases where the input range is small, it can be destroyed. To solve this problem, the common practice is to use a Pre-amplifier stage to convert a low-input signal to a better-suited signal and then deliver it to the Latch circuit on the next stage. In this study, the structure of Figure 4 for the comparator circuit is used.

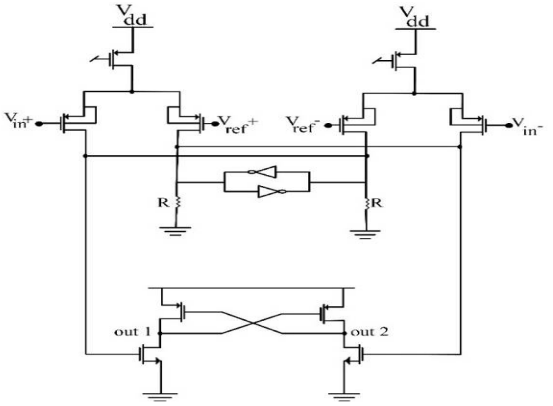

Figure 4. Proposed comparator structure

Also, in the first stage, due to lack of area at the IC level, instead of the passive resistance, active elements are used. That is, the transistors of Figure 4 actually play the role of resistance. For the comparator circuit in a convertor to improve its performance and not to limit the overall design, it must be able to eliminate unwanted offsets and detect the smallest amount of input. There are various ways to eliminate offsets that usually exhibit this defect, but they require separate time to do so. Absolutely, comparison should be stopped regularly in each cycle or after several cycles and start the elimination of offsets. If it can be done directly without additional time to eliminate offsets, it will be a way to achieve a higher speed in the comparator design. Innovation in this field has made it possible. To eliminate offsets, a method should be determined to identify the offsets. If an ideal amplifier circuit is to be considered in a situation which its average input is zero, its average output is expected to be zero. If the amplifier has offsets, the average value of the signal in the output is not zero and has a non-zero value. Therefore, if a signal at the input of a circuit that has a mean of zero can be created, it is expected to be zero if the offset of average output signal is lost. To reach the input with a mean of zero, we will switch the input and output in each cycle as demonstrated in Figure 5.

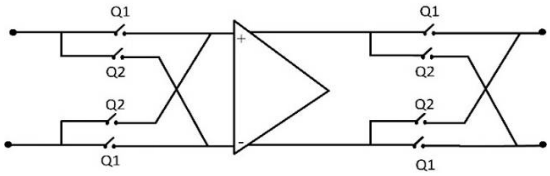

Figure 5. Switching amplifier for offset removing

As shown in Figure 5, when this operation is performed on a regular basis, the mean input is therefore zero and, by examining the average output voltage, we can detect the offset in the circuit output. Finally, to determine the average output voltage of the pre amplifier, two simple RC circuits are used on each side of the output according to the Figure 6. In each cycle of the comparison operation, when the switch of the comparator output is not connected, we allow the RC circuits to be connected to the circuit output. Thus, after a large number of cycles, the average output signal of each side in the corresponding capacitor is specified. In using the voltages of these capacitors to eliminate the offset as shown in Figure 7, we can put a controlled current source with the voltages of these capacitors in each side.

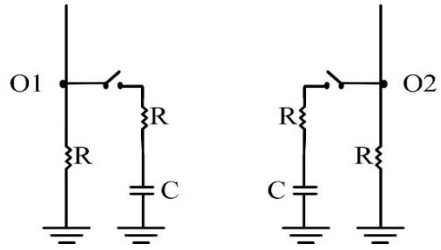

Figure 6. Using the RC circuit on each side of the output

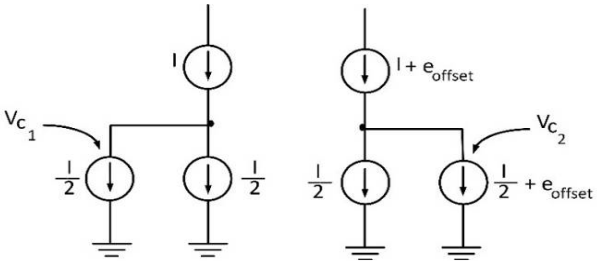

Figure 7. Voltage controlled current sources

Each side that has more current tends to have higher voltages and as such, more current from the active loads should be pulled out. As a result, we can use two simple transistors, each gate of which is connected to the capacitor of its own side, as shown in Figure 8, for implementation of voltage dependent current sources. The complete circuit diagram, regardless of switches, is shown in Figure 8.

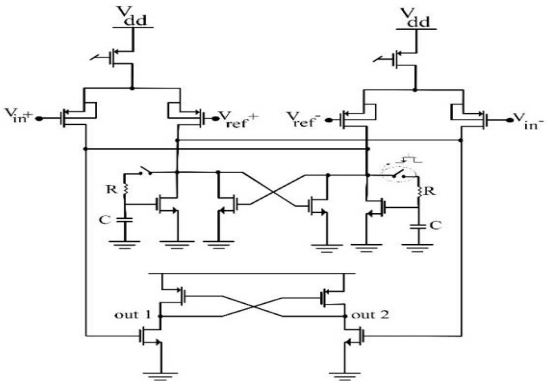

Figure 8. The proposed comparator circuit

3.2 Buffer

One of the vital blocks is the Buffer block which amplifiers the differential signal (the difference of the main signal from the first stage signal). The transfer of signal by the buffer to the next level at a low and high precision time is one of the problems that, if solved, can take an effective step in ADC speed increase and it can have many applications. As shown in Figure 9, if the common source buffer is considered as an open loop buffer, we can have:

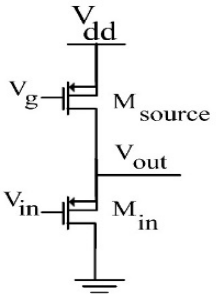

Figure 9. Conventional Buffer Structure

The gain of this circuit in small signal mode will be equal to:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{r_{ds_{source}} \cdot r_{ds_{in}} \cdot g_{m_{in}}}{(r_{ds_{source}} \cdot r_{ds_{in}} \cdot g_{m_{in}}) + r_{ds_{source}} + r_{ds_{in}}} \quad (1)$$

As can be seen, the term $\frac{1}{g_{m_{in}}}$ in the above relation causes the gain not to be exactly equal to one.

In the case of circuits built with BJT technology, this gain could be very accurate and meet many needs in the field of integrated circuits. But with the MOS technology, the gains are not so much accurate due to the fact that the transistors have small r_{ds} and g_m. In addition, the mentioned buffer does not have desirable frequency response.

As you can see, the buffer gain limit is said to be due to the resistor limitation in the source of the transistor. In this design, negative resistance has been used to compensate for this problem. The concept of this is very simple, so if two resistors of the same size, but one positive and the other negative, are parallel, the resistance in the source will be very large and the buffer gain becomes more accurate.

To build the negative resistance, the famous Latch structure is used. It shown in Figure 10.

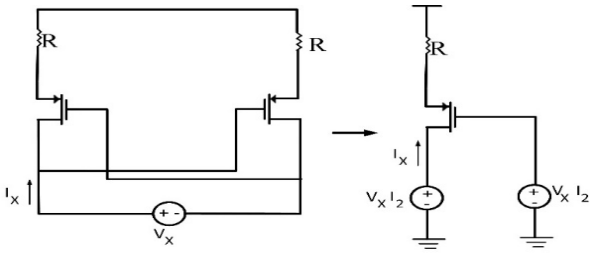

Figure 10. The famous structure of LATCH to create a negative resistance

$$\frac{V_x}{2} = Ri_x + r_{ds}\left(i_x + g_m\left(Ri_x + \frac{V_x}{2}\right)\right) \rightarrow \frac{V_x}{2}(1 - g_m r_{ds}) = i_x(R + r_{ds} + g_m r_{ds} R)$$

$$R_{in} = \frac{V_x}{i_x} = 2\left(\frac{r_{ds} + (1 + g_m r_{ds})R}{1 - g_m r_{ds}}\right) \quad (2)$$

Assuming $g_m r_{ds} >> 1$, we have:

$$R_{in} = 2\left(\frac{r_{ds} + (1 + g_m r_{ds})R}{-g_m r_{ds}}\right) = -2\left(R + \frac{1}{g_m} + \frac{R}{g_m r_{ds}}\right) \quad (3)$$

If $R \approx r_{ds}$, so we have:

$$R_{in} = -2\left(R + \frac{2}{g_m}\right) = -2(r_{ds} + \frac{2}{g_m}) \quad (4)$$

Consequently, if we have a circuit similar to that shown in Figure 11, then we will have:

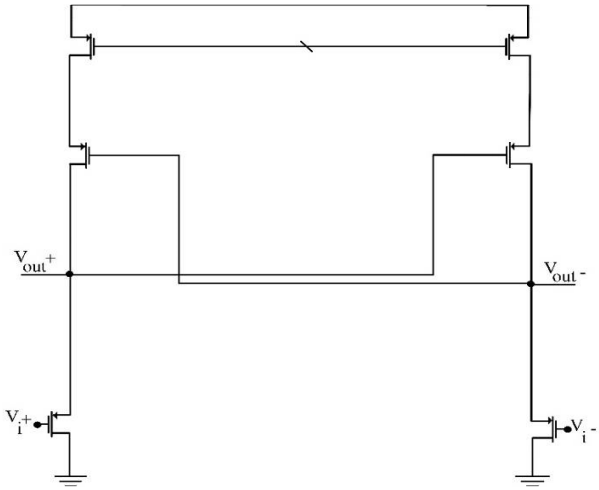

Figure 11. The proposed circuit for the buffer structure

The gain of the circuit will be equal to:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{-2(r_{ds} + \frac{2}{g_m}) \cdot r_{ds_{in}} \cdot g_{m_{in}}}{(-2(r_{ds} + \frac{2}{g_m}) \cdot r_{ds_{in}} \cdot g_{m_{in}}) + (-2(r_{ds} + \frac{2}{g_m})) + r_{ds_{in}}} \quad (5)$$

This shows a dramatic improvement in buffer gain.

3.3 Amplifier circuit

After extracting the second-stage bits, an amplifier is required to amplify the rest of the signal. 1 ns time is needed to amplify the signal. Looking at the conventional structures of amplifiers with precision, it can be seen that most of these structures use a negative feedback loop. Such amplifiers cannot operate at short time of about 1 ns due to operational amplifier constraints. The only solution to achieve an amplified voltage in the short time of 1 ns, is to use an open loop amplifier. The most important issue associated with the use of loop amplifiers is their low accuracy. To solve this problem in the proposed circuit, a method is used to improve this accuracy. For this purpose, the Folded Cascade circuit whose input transistors are scaled is used. This circuit is shown in Figure 12.

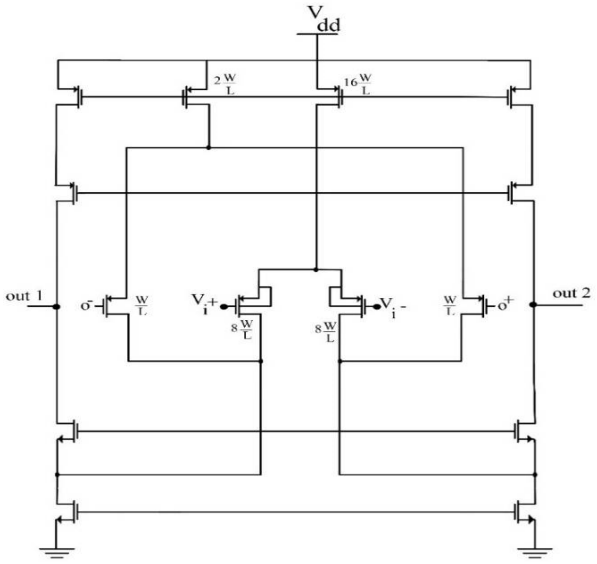

Figure 12. Structure of the proposed amplifier

3.4 Clock generation circuits

The clock required in ADC is the method of reference (Rezapour, et al., 2019). The difference is that, this Ring Counter is made up of two flip-flops to be reset and one flip-flop to be set. On the other hand Ring counter Error Correction Circuit design for two flip-flops. The Ring Counter Error Correction circuit is shown in Figure 13. As in reference (Rezapour, et al., 2019), In Ring Counter circuit for every clock, one of the outputs (phi0, phi1 and phi2) must be '1' and the rest must be '0'. If this happens otherwise, the error correction circuit will fix it (Holdsworth and Woods, 2002).

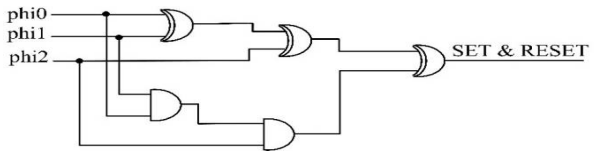

Figure 13. Ring counter Error Correction Circuit (Holdsworth and Woods, 2002)

4. SIMULATION AND RESULTS

After presenting the final block of the ADC convertor and related circuits which are completely new, this section first presents the simulation results of all circuits separately. Thereafter, the simulation results of the analogue to digital convertor are presented.

4.1 S/H circuit

For S/H circuits design, we used method of reference (Rezapour, et al., 2019). Also, because analog voltage goes straight to the S/H in the first stage and requires a precision of 7 bits, the capacitor is 0.05 PF, and the second stage requires a precision of 8 bits, in which we used a capacitor of 0.2 PF (Abo, 1999). To evaluate the proposed S/H performance, the SNDR measurement method is used in the buffer output. The differential load of the buffer output is also 1pF. The method involves the use of a variable-frequency signal in the input and in the buffer output. Signal-to-noise-and-distortion ratio (SNDR) is the ratio of the input signal amplitude to the rms sum of all other spectral components. SNDR measurements are performed with the help of the HSPICE software; the sampling frequency is considered as 400 MHz. The simulated SNDR versus the input signal frequency is shown in Table 1 and Figure 14. As shown in the table, the SNDR is a very high and good value, indicating the proper function of the designed convertor.

Table 1. Measurement SNDR

$s_{ampling}$	f_{in}	SNDR
400MHz	10MHz	-84dB
400MHz	20MHz	-81dB
400MHz	60MHz	-77dB
400MHz	190MHz	-76dB

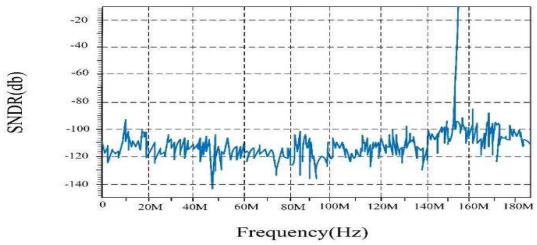

Figure 14. The simulated ADC SNDR versus the input signal frequency.

To bring the simulation results closer to the results of construction, two signals with close frequencies are used. Also if, with this operation, the SNDR output again has values below -80dB, as shown in Figure 14, the proposed circuit for S/H is well suited for the design of an ADC with a sampling rate of 400 MS/s.

4.2 Comparator circuit

As previously mentioned the comparator circuit can remove offset, it shown in Figure 15, the circuit offset disappears after several cycles and the circuit operates correctly. Also, based on the simulations carried out, the proposed circuit can detect a voltage difference of 8 mV correctly at a clock frequency of 1 GHz (1 ns period, as shown in Figure 15). If at 1 GHz the comparator circuit can remove offset, then it is certain that it will not develop problem at 400 MHz.

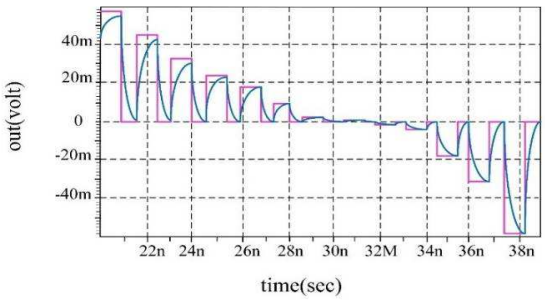

Figure 15. Comparison circuit offset after several cycles

The comparator circuits are tested in the worst conditions, such that a very large positive value is first applied to the comparator, followed by the application of a negative value (up to the LSB/2 level). The comparator should be able to identify this change correctly. In the opposite case, the circuit must correctly detect the change of operation. In Figure 16(a), curves V_{in} are the inputs of Figure 10, and in Figure 16(b), curves output and inverse output are the outputs of Figure 3.

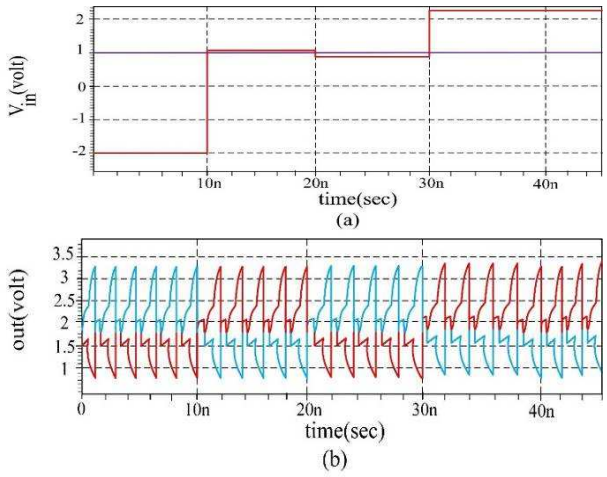

Figure 16. Simulation results of comparator circuit, (a) inputs of Figure 8 and (b) outputs of Figure 8

4.3 The buffer circuit

As shown in Figure 11, in order to simulate the buffer circuit, a load must be placed on its output. In this study, we considered the load capacitance equal to 1pF.As shown in the Figure17, the conventional buffer (Figure9) with a DC gain is close to 0.9, while the proposed buffer (Figure11) has a precision unit rate of 1 GHz (it shown in Figure 18). It is also apparent from the figure that the -3 dB bandwidth is acceptable and can be seen to be above 1 GHz.

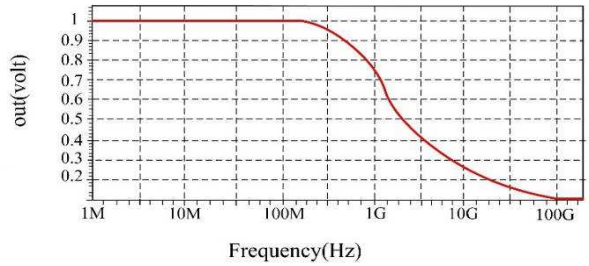

Figure 17. Result of Conventional Buffer Structure (Figure 6)

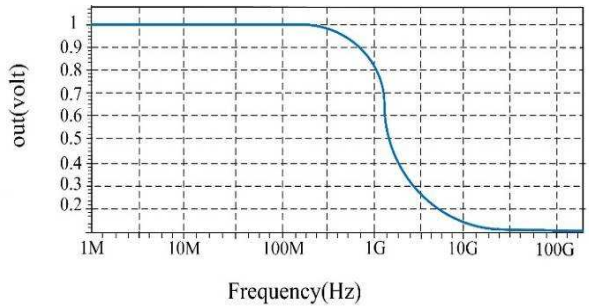

Figure 18. Proposed buffer output (Figure 9)

4.4 Amplifier circuit

Figures 19(a) and 19(b) shows the frequency responses of the gain stage (Figure 12) in the second stage. The circuit has a gain of 8V and the bandwidth or -3 dB frequency is 1.49 GHz. The circuit also has better stability because Phase Margin is at a frequency of -3dB equal to 70 degree, which has the best stability The important thing in Figure 19(a) is that the UGB of both stages of the amplifier, where the gain is equal to 1 or 0, is above 10 GHz and this shows the correct performance of the amplifiers.

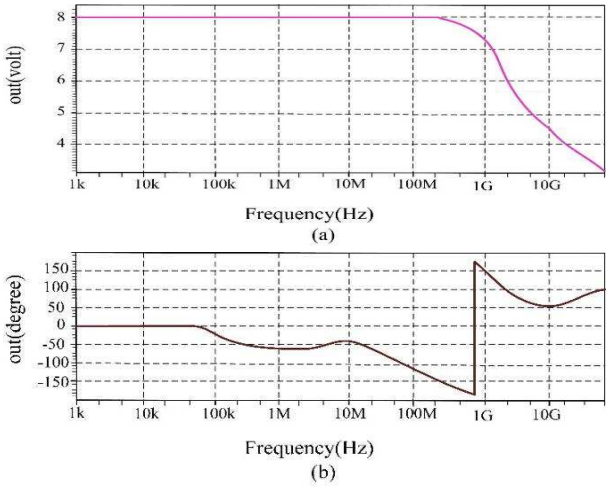

Figure 19. (a) Gain (out(dB)) for Figure 12 of the second stage and (b) phase response(out(degree)) for Figure 12 of the second stage

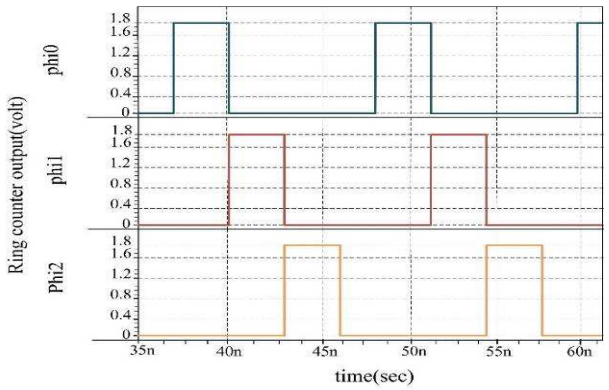

Figure 20. Output of ring counter circuit in figure 13

5. CONCLUSIONS

Since in pipeline analog to digital convertor is disappears about half of conversion time in the amplifier, so in this paper to increase the speed of convertor didn't use the amplifier for the first stage, and to transfer the data from the first stage to the second stage designed a buffer with gain very accurate unit that can transfer the data to the next stage at a low time with high speed and high accuracy. Given the lack of data amplification in first stage, the second stage requires a precision comparator circuit that can detect offset without delay and eliminates it. So a new structure comparator and low power was designed. There is also another idea for further increase of the convertor speed, we designed the analog circuits with open loop structures, and so for the second stage an amplifier with a precision of 8, the open loop

was designed. A new error correction circuit was designed for the Ring Counter. Since it is necessary for a 10-bit Pipeline ADC to have the S/H circuit having a minimum accuracy of 11 bits. Therefore, the S/H circuit designed has a precision above 11 bits. A 10-bit pipeline convertor with sampling speed of 400 MS/s with 0.18 µm TSMC technology was designed and simulated in this study. All internal circuits of this convertor were designed and their simulation results were presented separately. Finally, the overall simulation of the ADC convertor was carried out and the results of the proposed simulation were: 10-bit resolution, sampling rate of 400 MS/s and power consumption of 74.3 mW. All analyses were also performed using the Hspice software in the 0.18 µm process. In Table 2, the simulation results are compared with previous study. Since all designs are voltage based, we therefore recommend that the designs be current based and compare the results of this paper. Also use calibration to reduce the error and use the sub threshold method to reduce the power consumption.

Table 2. Comparison of the proposed ADC with previous work

Speed (MHz)	Power (mW)	SNDR (dB)	SFDR (dB)	Bit	Process (um)	Ref
100	19.7	54.4	-	10	0.18	(Rezapour, et al., 2019)
350	75	60.52	69.27	10	0.18	(Rezapour, et al., 2019)
30	136	43.1	75.51	14	0.5	(Lv, et al., 2018)
200	46.8	54.7	-	10	0.13	(Murshed, et al., 2018)
200	115	55.58	62.97	10	0.18	(Wang, et al., 2017)
250	120	74.4	87.1	14	0.018	(Wang, et al., 2018)
166	38.9	45.9	50	8	0.018	(Li and Du, 2017)
250	28	61.84	78.2	10	0.018	(Fan, et al., 2017)
400	74.3	59.2	65.7	10	0.18	This Work

References:

Abo, A.M., 1999. Design for reliability of low-voltage switched-capacitor circuits, *Doctor of Philosophy in Electrical Engineering, University of California Berkeley*.

Adimulam, M.K., Movva, K.K., Srinivas, M., 2017. A low power, programmable 12-bit two step SAR-flash ADC for signal processing applications, 2017 30th IEEE International System-on-Chip Conference (SOCC), IEEE, pp. 45-50. doi: 10.1109/SOCC.2017.8226004.

Ali, A.M., Dinc, H., Bhoraskar, P., Dillon, C., Puckett, S., Gray, B., Speir, C., Lanford, J., Brunsilius, J., Derounian, P.R., 2014. A 14 Bit 1 GS/s RF sampling pipelined ADC with background calibration, *IEEE Journal of Solid-State Circuits* 49, pp. 2857-2867. doi: 10.1109/JSSC.2014.2361339.

Boo, H.H., Boning, D.S., Lee, H.-S., 2015. A 12b 250 MS/s pipelined ADC with virtual ground reference buffers, *IEEE Journal of Solid-State Circuits* 50, pp. 2912-2921, DOI: 10.1109/JSSC.2015.2467183.

Cárdenas-Olaya, A., Rubiola, E., Friedt, J.-M., Bourgeois, P.-Y., Ortolano, M., Micalizio, S., Calosso, C., 2017. Noise characterization of analog to digital converters for amplitude and phase noise measurements, *Review of Scientific Instruments* 88, p. 065108, DOI: 10.1063/1.4984948.

Correia, A.P.P., Barquinha, P.C., da Palma Goes, J.C., 2015. A Second-Order ΣΔ ADC Using Sputtered IGZO TFTs, Springer.

de Aguilar, J.D., Salinas, J., Lapuh, R., Méndez, A., Lagos, F.G., Sanmamed, Y., 2016. Characterization of the amplitude frequency response of analog-to-digital converters, 2016 Conference on Precision Electromagnetic Measurements (CPEM 2016), IEEE, pp. 1-2, DOI: 10.1109/CPEM.2016.7540455.

Fan, Q., Chen, J., Wen, X., Feng, Y., Tang, Y., Zuo, Z., Gong, D., Liu, T., Ye, J., 2017. A low-power 10-bit 250 MS/s dual-channel pipeline ADC in 0.18 µm CMOS, *Journal of Instrumentation* 12, p. C02018, DOI: 10.1088/1748-0221/12/02/C02018.

Fatemi-Behbahani, E., Farshidi, E., Ansari-Asl, K., 2016. Analysis of chaotic behavior in pipelined analog to digital converters, *AEU-International Journal of Electronics and Communications* 70, pp. 301-310, DOI: 10.1016/j.aeue.2015.12.008.

Holdsworth, B., Woods, C., 2002. Digital logic design, Elsevier.

Khalapure, S., Siddharth, R., Vasantha, M., 2017. Design of 5-Bit Flash ADC Using Multiple Input Standard Cell Gates for Large Input Swing, 2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), IEEE, pp. 585-588, DOI: 10.1109/ISVLSI.2017.108.

Khorami, A., Sharifkhani, M., 2016. High-speed low-power comparator for analog to digital converters, *AEU-International Journal of Electronics and Communications* 70, pp. 886-894, DOI: 10.1142/S0218126617501183.

Kiran, K.R., Kumar, A., Reddy, A.S., Sarojini, M., 2016. A 5-bit, 0.08 mm 2 area flash analog to digital converter implemented on cadence virtuoso 180nm, 2016 International Conference on Emerging Trends in Engineering, Technology and Science (ICETETS), IEEE, pp. 1-6, DOI: 10.1109/ICETETS.2016.7603035.

Li, Y.F., Du, L., 2017. 1.5 bit-per-stage 8-bit Pipelined CMOS A/D Converter for Neuromophic Vision Processor, *arXiv preprint arXiv:1701.08877*.

Liu, C.-C., Chang, S.-J., Huang, G.-Y., Lin, Y.-Z., 2010. A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure, *IEEE Journal of Solid-State Circuits* 45, pp. 731-740, DOI: 10.1109/JSSC.2010.2042254.

Liu, D., He, L., Lin, F., Li, T., Chou, Y.-K., 2017. A Time-Interleaved Statistically-Driven Two-Step Flash ADC for High-Speed Wireline Applications, *Journal of Circuits, Systems and Computers* 26, p. 1750118, DOI: 10.1142/S0218126617501183.

Lv, J., Que, L., Wei, L., Meng, Z., Zhou, Y., 2018. A low power and small area digital self-calibration technique for pipeline ADC, *AEU-International Journal of Electronics and Communications* 83, pp. 52-57, DOI: 10.1016/j.aeue.2017.08.025.

Murshed, A.M., Krishna, K.L., Saif, M.A., Anuradha, K., 2018. A 10-bit high speed pipelined ADC, 2018 2nd International Conference on Inventive Systems and Control (ICISC), IEEE, pp. 1253-1258, DOI: 10.1109/ICISC.2018.8399006.

Ozeki, T., Naka, J., Takuji, M., 2017. A/D converter including multiple sub-A/D converters, Google Patents.

Prakash, A.J., Jose, B.R., Mathew, J., Jose, B.A., 2017. A Differential Quantizer-Based Error Feedback Modulator for Analog-to-Digital Converters, *IEEE Transactions on Circuits and Systems II: Express Briefs* 65, pp. 21-25, DOI: 10.1109/TCSII.2017.2666822.

Rezapour, A., Tavakoli, M.B., Setoudeh, F., 2019. A new approach for 10-bit pipeline analog-to-digital converter design based on 0.18 µm CMOS technology, *AEU-International Journal of Electronics and Communications* 99, pp. 299-314, DOI: 10.1016/j.aeue.2018.10.030.

Rezapour, A., Tavakoli, M.B., Setoudeh, F., 2019. Analysis and design of a new structure for 10-bit 350MS/s pipeline analog-to-digital converter. *Genero & Direito* 8 - N. 03 – Ano, pp. 301-328, DOI: 10.22478/ufpb.2179-7137.2019v8n3.47576.

Roy, S., Banerjee, S., 2018. A 9-Bit 50 MSPS Quadrature Parallel Pipeline ADC for Communication Receiver Application, *Journal of The Institution of Engineers (India): Series B* 99, pp. 221-234, DOI: 10.1007/s40031-018-0315-y.

Sarkar, S., Cai, Y., Adak, A., 2017. Two-step residue transfer technique for high-speed pipeline A/Ds, 2017 30th International Conference on VLSI Design and 2017 16th International Conference on Embedded Systems (VLSID), IEEE, pp. 3-8, DOI: 10.1109/VLSID.2017.51.

Steensgaard-Madsen, J., 2016. Analog-to-digital converter, Google Patents.

Tao, S., 2015. Power-Efficient Continuous-Time Incremental Sigma-Delta Analog-to-Digital Converters, KTH Royal Institute of Technology, DOI: 10.1109/TCSI.2015.2418892.

Vyas, J.L., 2013. Simulation of 3 bit flash ADC in 0.18 µm technology using NG SPICE tool for high speed application, *IJSRD. Int J Sci Res, Dev* 1.

Wang, C., Wang, X., Ding, Y., Li, F., Wang, Z., 2018. A 14-bit 250MS/s Low-Power Pipeline ADC with Aperture Error Eliminating Technique, 2018 IEEE International Symposium on Circuits and Systems (ISCAS), IEEE, pp. 1-5, DOI: 10.1109/ISCAS.2018.8351100.

Wang, L., Meng, Q., Zhi, H., Li, F., 2017. A 10 bit 200 MS/s pipeline ADC using loading-balanced architecture in 0.18 µm CMOS, *Journal of Semiconductors* 38, p. 075003, DOI: 10.1088/1674-4926/38/7/075003.