

# Design and Control of a STATCOM for Non-Linear Load Compensation: A Simple Approach

Saurabh Mani Tripathi\* (Assistant Professor, Kamla Nehru Institute of Technology, Sultanpur, India),  
Prakash Ji Barnawal (Assistant Professor, Noida Institute of Engineering and Technology, Greater Noida, India)

**Abstract** – This paper presents a systematic procedure to design a simple control for a three-phase VSC-based static synchronous compensator (STATCOM) in order to overcome the problems caused by the presence of the non-linear load at the point of common coupling (PCC). The proposed control method regulates the STATCOM in such a way that the source quadrature current component is forced to be zero so that only the active current component is drawn from the source and the harmonic and reactive current demands of the non-linear load are met by the STATCOM. The tuning of the inner and outer loop PI controllers is carried out with the help of the modulus optimum and symmetric optimum criteria, respectively. At last, a few case studies are presented using MATLAB simulation to exemplify the success of the proposed control method.

**Keywords** – Modulus optimum; Non-linear load compensation; Power quality; Static synchronous compensator (STATCOM); Symmetric optimum.

## NOMENCLATURE

|            |  |
|------------|--|
| MO         | Modulation optimum                                       |
| PCC        | Point of common coupling                                 |
| SO         | Symmetric optimum  |
| VSC        | Voltage source converter                                 |
| $v_{abc}$  | Three-phase source voltages                              |
| $f$        | Supply frequency   |
| $i_{abc}$  | Three-phase source currents                              |
| $e_{abc}$  | Three-phase converter voltages                           |
| $R, L$     | Resistance and inductance of coupling reactor            |
| $V_{LL}$   | Line-to-line rms PCC voltage                             |
| $MI$       | Modulation index   |
| $V_{DC}$   | DC capacitor voltage                                     |
| $C$        | Capacitance  |
| $a$        | Overload factor  |
| $f_s$      | Switching frequency                                      |
| $I_{crp}$  | Ripple current   |
| $K_{pi}$   | Proportional gain of current PI controller               |
| $K_{ii}$   | Integral gain of current PI controller                   |
| $K_{po}$   | Proportional gain of DC voltage PI controller            |
| $K_{io}$   | Integral gain of DC voltage PI controller                |
| $G_{c,OL}$ | Open-loop transfer function of current control loop      |
| $G_{c,CL}$ | Closed-loop transfer function of current control loop    |
| $G_{v,OL}$ | Open-loop transfer function of DC voltage control loop   |
| $G_{v,CL}$ | Closed-loop transfer function of DC voltage control loop |

## I. INTRODUCTION

An improved power quality has always been a primary requirement and also a major challenge in any electric distribution system [1]. Due to the growing use of power electronics, power quality problems have become an important concern nowadays since these problems not only result in degradation of the power factor but also lead to failures of sensitive devices, equipment overheating etc. [2]–[5]. The increased penetrations of the distributed energy resources to the power grid have also given rise to many challenges related to power quality. The work reported in [6] presents a comprehensive discussion of power quality issues, basic standards, power quality monitoring techniques as well as techniques to mitigate power quality problems etc., especially in distributed generation systems. The non-linear loads connected at the point of common coupling (PCC) draw the harmonic and reactive currents in addition to the active current from the source, thereby degrading electric power quality [3], [7]. Earlier, only passive filters were used to mitigate power quality problems [3]. Nevertheless, fixed compensation capability and time-dependent adjustment of the filter parameters were present as some of the limitations of the passive filters [8], [9]. Nowadays, the inverter-based power quality conditioners have received much attention from researchers in mitigating power quality problems because of their small size and fast dynamic response with lower losses [10]. The shunt active power filters are used today not only to enhance reliability but also to mitigate the power quality problems due to the non-linear loads connected at the PCC [3], [8]. The performance of active power filters at different conditions along with involved control algorithms have been investigated in literature [11]–[15]. Further, different sorts of control algorithms employed for the shunt active power filters have been reviewed thoroughly in [2].

In this paper, a STATCOM (a shunt-connected second-generation FACTS device) is utilised for non-linear load compensation. A STATCOM is basically a solid-state switching converter that works as a static VAR compensator, having the ability to either absorb or supply reactive power at its terminals independently of the AC system voltage and provides better transient stability, dynamic response and enhanced capability to exchange power than any other shunt-connected FACTS devices [16]–[18]. Moreover, the STATCOM is becoming a potential choice to mitigate the power quality issues in distributed generation systems as well

\* Corresponding author.  
E-mail: mani\_excel@yahoo.co.in

[19], [20]. A review of various converter topologies and output filter configurations meant for STATCOM applications has been presented in [16].

The promising performance of the STATCOM depends not only on the converters but also on a well-designed control system [2], [21]. Numerous methods/theories have already been reported for STATCOM control such as the hysteresis-controller-based method, the deadbeat or predictive-control-based method, the instantaneous symmetrical component theory, the self-tuning-filter-based instantaneous reactive power theory, the cross-correlation-coefficients-based control and the enhanced phase-locked-loop based method [22]–[27] etc. Furthermore, the  $I \cos \phi$  algorithm has also been reported in literature [3], [20], [28] so as to accomplish the improvement in the power factor as well as compensation in reactive power with STATCOM. Ref. [29] presents a robust design for a current-controlled STATCOM. A robust voltage controller for a STATCOM was designed in [30] using a simple loop-shaping method. Li et al. [21] evaluated a direct-current vector control scheme for reactive power and voltage supports to the grid by means of a VSC-based STATCOM and compared the performances of the same with those of a conventional scheme.

Besides, proportional-integral (PI) controllers, offering stabilised controls, have always represented a vital part of the control system [30]–[32]. PI controllers are usually employed to implement the control of STATCOM [10]. A wealth of literature is available which deals with the design of the proportional and integral gains of the PI controller [33]–[38].

However, a linear mathematical model of the controlled system is a prerequisite for designing the PI controller [10]. The tuning of the PI controller parameters can be performed with the help of different tuning methods. Several PI tuning methods are discussed in [35] along with their key features and limitations as well.

The ‘modulus optimum’ and ‘symmetric optimum’ criteria are the simplest and most convenient PI tuning criteria [35]–[38]. The modulus optimum generally deals with the tuning of the PI controller for a second-order control system and results in fast and non-oscillatory time response whereas the symmetric optimum, which provides the advantage of a maximised phase margin along with better rejection to the disturbance, is generally applied when a pole of the open-loop transfer function of the control system is at the origin or near it [35], [38].

In this paper, a systematic procedure to design a simple control for a three-phase VSC-based STATCOM including component sizing as well as tuning of the inner and outer loop PI controllers by means of the ‘modulus optimum’ and ‘symmetric optimum’ criteria, respectively, is presented. The paper is organized as follows. The complete schematic of the STATCOM control method is described in Section II. The sizing of various system components is carried out in Section III. Tuning of the inner current PI controllers and the outer DC voltage PI controller is performed in Sections IV and V, respectively. Section VI presents the simulation verification of the proposed STATCOM control method. Finally, some conclusions are drawn in Section VII.

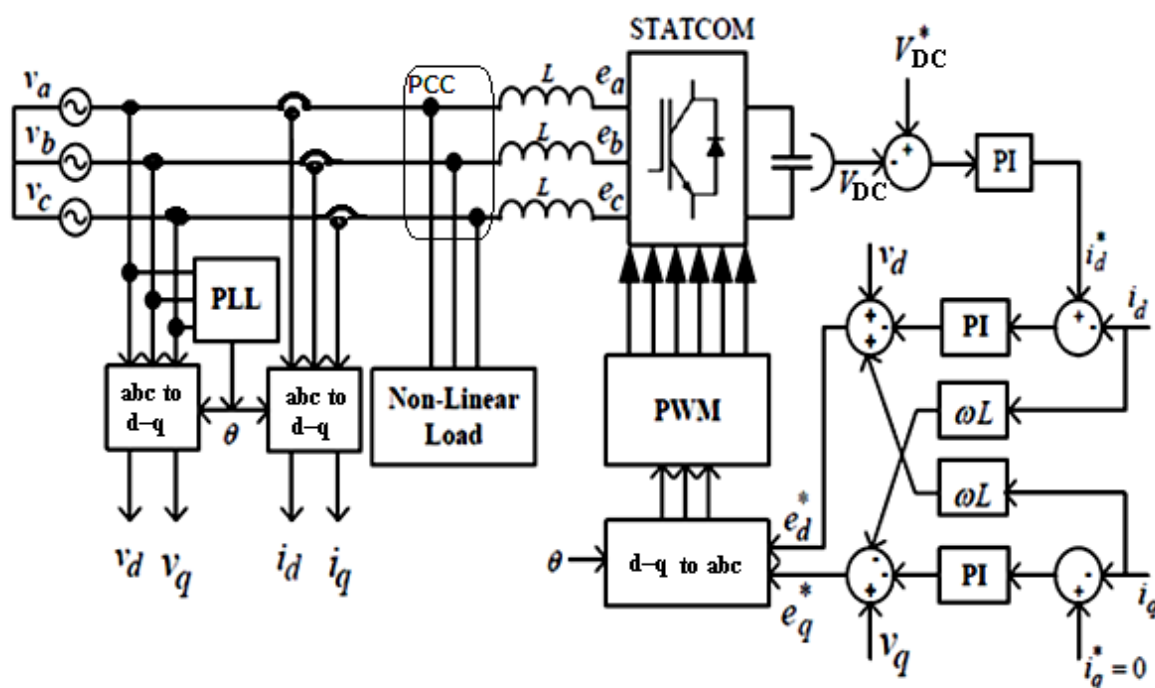


Fig. 1. Schematic of the proposed STATCOM control method.

## II. SYSTEM DESCRIPTION AND STATCOM CONTROL

The schematic of the proposed STATCOM control method is illustrated in Fig. 1. A three-phase AC source, a three-phase VSC-based STATCOM and the non-linear loads are connected at the PCC. Two PI controllers are involved in the inner current control loop and one PI controller is involved in the outer DC voltage control loop. The outer DC voltage PI controller generates the reference value of the direct-axis source current as follows:

$$i_d^* = K_{po} \left( \frac{1+T_o s}{T_o s} \right) (V_{DC}^* - V_{DC}). \quad (1)$$

The objective of compensating non-linear load connected at PCC is achieved by implementing the STATCOM control indirectly. Unlike the direct current control method, which is based on the extraction of the reactive and harmonic components from the load current [39], the proposed control is an indirect current control strategy, wherein the STATCOM operation does not require load current sensing; the control is rather based on the source current regulation such that the source quadrature current component is forced to be zero; accordingly, only the active current component is drawn from the source and the harmonic and reactive current demands of the non-linear load are met by the STATCOM itself. This indirect current control method has the advantage that it requires a reduced number of current sensors as compared to the direct current control method [39]. Let the three-phase AC voltages at PCC be

$$v_a = V \cos(\omega t); \quad (2)$$

$$v_b = V \cos\left(\omega t - \frac{2\pi}{3}\right); \quad (3)$$

$$v_c = V \cos\left(\omega t + \frac{2\pi}{3}\right), \quad (4)$$

where  $V$  is the peak value of the PCC voltage per phase.

The voltage relationship between the PCC and the inverter (STATCOM) is expressed as follows:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = R \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}. \quad (5)$$

Transforming (5) into a d-q reference frame, it can be written that

$$L \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -R & \omega L \\ -\omega L & -R \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} v_d - e_d \\ v_q - e_q \end{bmatrix}. \quad (6)$$

From Eq. (6) it can be seen that the voltage equations of each axis are cross-coupled. In order to facilitate the decoupled control of d-q axes source current components, the equivalent control signals are derived from the inner current control loop and the decoupled d-q axes reference inverter (STATCOM) voltage can then be expressed as follows:

$$e_d^* = v_d - \omega L i_q - \Delta v_d; \quad (7)$$

$$e_q^* = v_q - \omega L i_d - \Delta v_q, \quad (8)$$

where  $e_d^*$  and  $e_q^*$  are the reference values of the STATCOM voltages and

$$\Delta v_d = K_{pi} \left( \frac{1+T_i s}{T_i s} \right) (i_d^* - i_d); \quad (9)$$

$$\Delta v_q = K_{pi} \left( \frac{1+T_i s}{T_i s} \right) (i_q^* - i_q). \quad (10)$$

In order to generate the PWM control signals for the STATCOM, the reference STATCOM voltages obtained in (7)–(8) are transformed back into an a-b-c reference frame with the help of the grid-synchronising phase angle, which is estimated by using a phase-locked loop (PLL) [40]. A PLL system can be used to quickly and accurately detect the phase angle and frequency of source (grid) voltages. In our simulation, the discrete PLL block available in the Simulink library has been used (see Fig. 2).

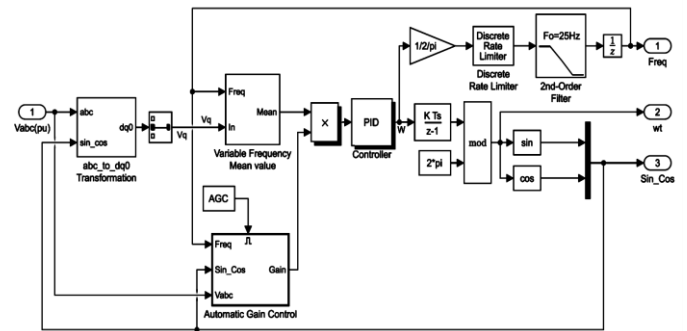


Fig. 2. Discrete PLL system for the detection of the phase angle and the frequency of the source (grid) voltages.

## III. COMPONENT SIZING

The component sizing for the system shown in Fig. 1 is performed as follows:

## A. DC Capacitor Voltage

The DC capacitor voltage basically depends upon the PCC voltage [41]. The relationship between the PCC voltage and the DC capacitor voltage [35], [41] can be shown as follows:

$$V_{DC} = \frac{2\sqrt{2}V_{LL}}{\sqrt{3MI}}, \quad (11)$$

where  $MI$  and  $V_{LL}$  represent the modulation index (set as unity) and the line-to-line rms PCC voltage, respectively.

Here, the value of the reference DC voltage is selected to be 800 V.

## B. DC Capacitor

The VSC of the STATCOM is rated for 25 kVA, hence the rms value of the system current would be

$$I_{rms} = \frac{25 \cdot 10^3}{\sqrt{3}V_{LL}}. \quad (12)$$

The capacitance value of the DC capacitor [35] may be formulated as

$$C = \frac{0.9I_{rms}}{0.02 \cdot 4\pi f V_{DC}}, \quad (13)$$

where  $f$  is the nominal supply frequency.

Here, the capacitance of the capacitor is selected to be 3200  $\mu$ F.

### C. Coupling Reactor

The inductance of the coupling reactor depends on the value of the converter switching frequency  $f_s$  and the line ripple current  $I_{crp}$  [35], [41] as follows:

$$L = \frac{\sqrt{3MI} \cdot V_{DC}}{12\alpha f_s I_{crp}}, \quad (14)$$

where the line ripple current is calculated as

$$I_{crp} = 0.05\sqrt{2}I_{rms}. \quad (15)$$

Here, the inductance value of the coupling reactor is selected to be 3.91 mH.

### IV. TUNING OF INNER CURRENT PI CONTROLLERS

The structure of the inner current control loop is depicted in Fig. 3. The current control loop is modelled in the synchronously rotating d–q reference frame. This frame allows treating the control variables as DC quantities [42]. By taking the difference of the reference and measured values of the d–q axes source currents, the error signals are generated and are processed by the inner PI current controllers. The PI controllers force the d–q axes source currents to follow their reference values exactly. Feed-forwarding is employed for reducing the problems caused by the cross-coupling of the axes currents [43].

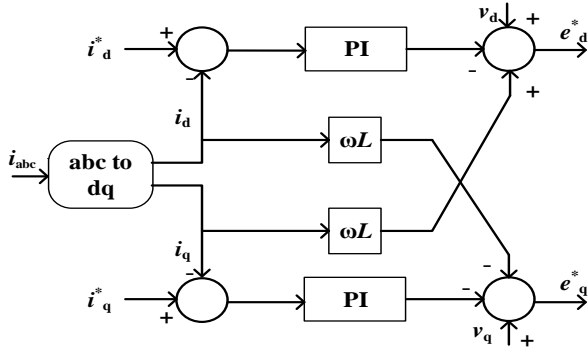


Fig. 3. Structure of the inner current control loop.

The anti-wind-up gain for the PI current controllers is set as the inverse of the proportional gain [44]. The anti-wind-up PI controller modelled in MATLAB/Simulink is illustrated in Fig. 4.

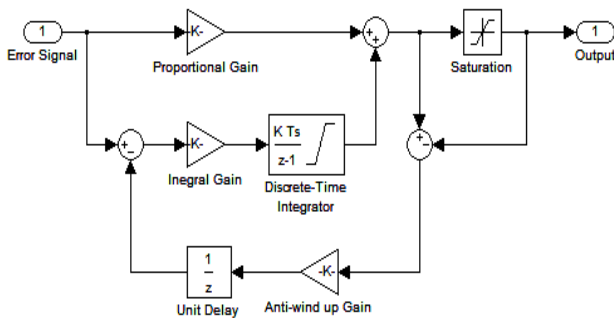


Fig. 4. Anti-wind-up PI controller modelled in MATLAB/Simulink.

The block-diagram representation of the inner current control loop is depicted in Fig. 5. Using the block diagram of the inner current control loop, the open-loop transfer function can be expressed as follows:

$$G_{C,OL}(s) = \frac{i_d}{i_d^*} = \frac{i_q}{i_q^*} = K_{pi} \left( \frac{1+T_i s}{T_i s} \right) \left( \frac{1}{1+T_w s} \right) \frac{1}{R} \left( \frac{1}{1+\tau s} \right), \quad (16)$$

where

$$T_i = K_{pi}/K_{ii}, \quad (17)$$

$$\tau = L/R, \quad (18)$$

and  $T_w$  is the average time-lag associated with the control delay and the PWM converter i.e. 1.5 times the sampling time ( $T_{sample}$ ) of the inner current control loop [35].

$$T_w = 1.5T_{sample}. \quad (19)$$

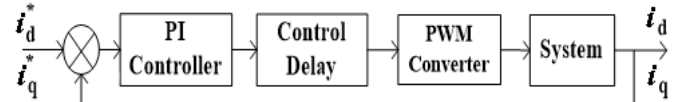


Fig. 5. Block-diagram representation of the inner current control loop.

The fast response is a mandatory requirement for the inner current control loop. In view of this, the inner current PI controllers are tuned by using the ‘modulus optimum’ criterion, which is a very simple technique of PI tuning, providing a faster and non-oscillatory response [35]. According to the modulus optimum criterion, the dominant pole of the plant is cancelled with the controller zero resulting in

$$T_i = \tau, \quad (20)$$

where  $T_i$  is the integral time constant of the inner current PI controllers.

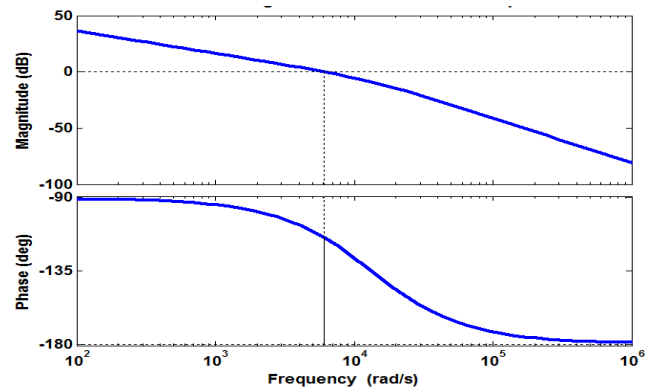


Fig. 6. Bode plot of the open-loop transfer function of the inner current control loop.

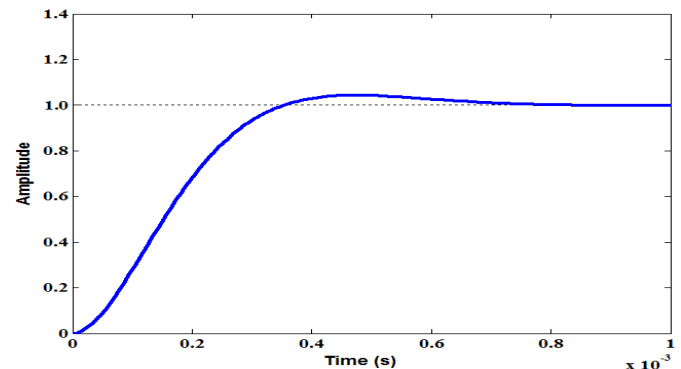


Fig. 7. Step response of the inner current control loop.

Further, the proportional gain of the inner current PI controllers is formulated [35], [36], [38] as

$$K_{pi} = \frac{\tau R}{2T_w}. \quad (21)$$

Using (16), (20)–(21), the open-loop transfer function of the inner current control loop is modified as follows:

$$G_{C,OL}(s) = \frac{1}{2T_w s} \left( \frac{1}{1 + 2T_w s} \right). \quad (22)$$

Hence, the closed-loop transfer function of the inner current control loop can be derived as follows:

$$G_{C,CL}(s) = \frac{1}{2T_w^2 s^2 + 2T_w s + 1}. \quad (23)$$

It can be deduced from (23) that the complex poles of the closed-loop transfer function of the inner current control loop have the damping ratio  $\xi = 0.7071$  and the natural frequency  $\omega_n = 1/T_w \sqrt{2}$ . The open-loop Bode plots and the step response of the inner current control loop are shown in Figs. 6–7, respectively. The modulus optimum PI tuning criterion results in a phase margin equal to  $65.5^\circ$  as well as an infinite gain margin meaning that the closed-loop system would be stable. From the step response depicted in Fig. 6 the settling-time is observed to be 0.63 ms with an overshoot of 4.32 %.

#### V. TUNING OF OUTER DC VOLTAGE PI CONTROLLER

By taking the difference of the reference and measured values of the DC voltage across the capacitor, the error signal is generated, which is processed by the outer DC voltage PI controller so as to produce the reference direct-axis source current command for the inner current control loop. The anti-wind-up gain for the DC voltage PI controller is set as the inverse of the proportional gain [44].

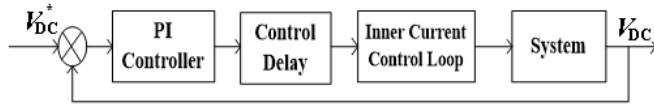


Fig. 8. Block diagram representation of the DC voltage control loop.

The block-diagram representation of the outer DC voltage control loop is depicted in Fig. 8. Using the block diagram of the outer DC voltage control loop, the open-loop transfer function can be expressed as follows:

$$G_{V,OL}(s) = \frac{K_{po} K}{sT} \left( \frac{1 + T_o s}{T_o s} \right) \left( \frac{1}{1 + T_e s} \right), \quad (24)$$

where

$$T_v = K_{po}/K_{io}; \quad (25)$$

$$T = 2C/3; \quad (26)$$

$$K = v_d/V_{DC}, \quad (27)$$

and  $T_e$  is the sum of the time lag associated with the control delay in the outer DC voltage control loop ( $= 10T_{\text{sample}}$ ) and the time constant of the approximated first-order closed-loop transfer function of the inner current control loop ( $= 2T_w$ ), i.e.

$$T_e = 2T_w + 10T_{\text{sample}}. \quad (28)$$

The desired goal of the outer DC voltage control loop is system stability and optimum regulation. It can be observed from (24) that the outer DC voltage control loop has a pole at

the origin and therefore, the symmetric optimum criterion is used for the tuning of the outer DC voltage PI controller, which helps maximising the phase margin and thereby tolerating system delays. The cross-over frequency corresponding to the maximum phase margin would be the geometrical mean of the two corner frequencies formulated as

$$\omega_c = 1/\sqrt{T_o T_e}. \quad (29)$$

According to the symmetric optimum criterion of PI tuning, a symmetric response about the frequency  $\omega_c$  can be obtained when

$$T_o = a^2 T_e, \quad (30)$$

where  $T_o$  is the integral-time constant of the outer DC voltage PI controller and parameter ‘ $a$ ’ may vary from 2 to 4 [35].

Further, the proportional gain of the outer DC voltage PI controller is formulated [35], [36], [38] as

$$K_{po} = \frac{T_c}{K\sqrt{T_o T_e}} = \frac{T_c}{aKT_e}. \quad (31)$$

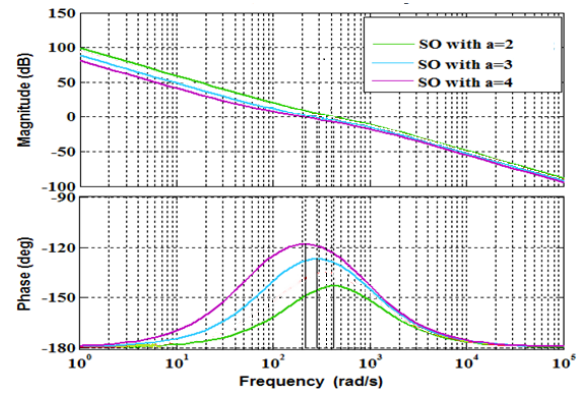


Fig. 9. Bode plot of the open-loop transfer function of the outer DC voltage control loop.

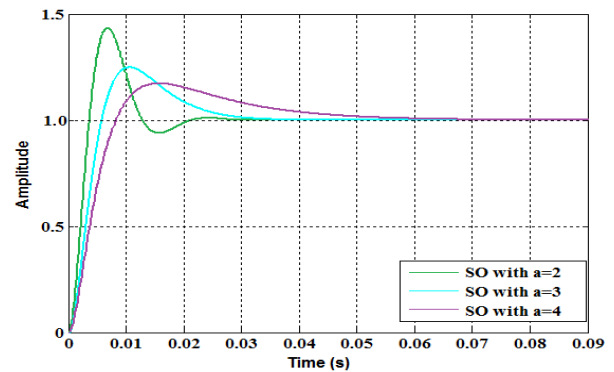


Fig. 10. Step responses of the DC voltage control loop.

Using (24), (30)–(31), it is possible to obtain the closed-loop transfer function of the outer DC voltage control loop as

$$G_{V,CL}(s) = \frac{1 + a^2 T_e s}{(aT_e s + 1)(a^2 T_e^2 s^2 + a(a-1)T_e s + 1)}. \quad (32)$$

The open-loop Bode plots and step responses of the outer DC voltage control loop for different values of parameter ‘ $a$ ’ are shown in Figs. 9–10, respectively.

TABLE I  
RESULTS CORRESPONDING TO THE DESIGN OF THE PI CONTROLLER OF THE DC VOLTAGE CONTROL LOOP

| Tuning criterion | $K_{pi}$ | $T_i$   | GM, dB    | PM, ° | Crossover frequency, rad/s | Closed loop stable? | Damping ratio | Step response |                   |
|------------------|----------|---------|-----------|-------|----------------------------|---------------------|---------------|---------------|-------------------|
|                  |          |         |           |       |                            |                     |               | Overshoot, %  | Settling time, ms |
| SO with $a = 2$  | 3.8744   | 0.00260 | $-\infty$ | 36.9  | 769                        | Yes                 | 0.5           | 43.4          | 10.8              |
| SO with $a = 3$  | 2.5829   | 0.00585 | $-\infty$ | 53.1  | 513                        | Yes                 | 1.0           | 24.9          | 15.4              |
| SO with $a = 4$  | 1.9372   | 0.01040 | $-\infty$ | 61.9  | 385                        | Yes                 | 1.0           | 17.3          | 26.6              |

The PI controller parameters, the gain and phase margins as well as the settling time and the percentage peak overshoot in the step responses are listed in Table I. It can be observed that, with an increase in parameter 'a', the phase margin and the settling time both increase whereas the overshoot decreases. With increased phase margin, also the robustness of the system increases [35]. It is found that the DC voltage control loop offers reasonable performance when  $a = 3$ . Hence, the value of parameter 'a' is chosen equal to 3 for the tuning of the outer DC voltage PI controller. The symmetric optimum PI tuning criterion corresponding to  $a = 3$  results in a phase margin equal to  $53.1^\circ$  while the settling time is observed to be 15.4 ms with an overshoot of 24.9 %.

TABLE II  
SIMULATION PARAMETERS

| Parameter | Value        |
|-----------|--------------|
| $V_{LL}$  | 415 V        |
| $F$       | 50 Hz        |
| $R$       | 1.8 $\Omega$ |
| $L$       | 3.91 mH      |
| $C$       | 3200 $\mu$ F |
| $V_{DC}$  | 800 V        |
| $K_{pi}$  | 26.06        |
| $K_{ii}$  | 12 000       |
| $K_{po}$  | 2.5829       |
| $K_{io}$  | 445.327      |

## VI. SIMULATION VERIFICATION

Having tuned the inner and outer PI controllers with the help of the modulus optimum and symmetric optimum criteria, respectively, a few case studies are presented using MATLAB simulation to exemplify the success of the proposed STATCOM control method as follows:

- Case 1: Performance under balanced non-linear load;
- Case 2: Performance under unbalanced non-linear load;
- Case 3: Performance under unbalanced non-linear load with a switched unbalanced linear resistive load.

A stiff AC supply system with a negligible grid impedance has been considered in this paper. The uncontrolled diode-bridge rectifier is usually employed as non-linear load in simulations as well as experimental setups due to the fact that it results in the worst harmonic current distortions [4], [45], [46]. Also in this study, the uncontrolled diode-bridge rectifier has been used in constituting the non-linear load. Further, the system parameters used in the simulation are listed in Table II.

### Case 1: Performance Under Balanced Non-Linear Load

In this case, the performance of the proposed STATCOM control method is analysed under balanced non-linear load which is constituted by three single-phase diode-rectifiers that separately feed impedances of similar values, i.e.  $(20 + j18.85) \Omega$ . One can observe from Fig. 11(a) that the capacitor voltage is maintained at its reference value, i.e. 800 volts. The observed three-phase PCC voltage is sinusoidal (see Fig. 11(b)). The non-linear load current profiles for all three phases are shown separately in Fig. 11(c). These non-linear load currents are compensated by the inverter (STATCOM). The compensating STATCOM current profiles for all three phases are shown separately in Fig. 11(d). Fig. 11(e) shows the compensated source current profiles which are nearly sinusoidal. Moreover, it is noticeable that similar currents are carried by each phase since the non-linear loads connected at the PCC are balanced. The harmonic spectra and the THDs of the load and source currents are also shown in Figs. 11(f)–(h) for all three phases. Further, the magnitudes and THDs of the load and source currents for Case 1 are listed in Table III.

### Case 2: Performance Under Unbalanced Non-Linear Load

In this case, the performance of the proposed STATCOM control method is analysed under unbalanced non-linear load which is constituted by three single-phase diode-rectifiers connected between the phases a–b, b–c and c–a, respectively; which separately feed impedances of different values, i.e.  $(12 + j18.85) \Omega$ ,  $(20 + j1.885) \Omega$  and  $(28 + j0.1885) \Omega$  at the DC sides, respectively. Although a small ripple in DC voltage is apparent in Fig. 12(a), caused by the unbalanced non-linear load currents, still the capacitor voltage is maintained at its reference value, i.e. 800 volts, in this case as well. The observed three-phase PCC voltage is sinusoidal (see Fig. 12(b)). The non-linear load current profiles for all three phases are shown separately in Fig. 12(c). Even under unbalanced non-linear load connected at the PCC, the STATCOM effectively compensates the non-linear load currents, and the compensating STATCOM current profiles for all three phases are shown separately in Fig. 12(d). Fig. 12(e) shows the compensated source current profiles, which are nearly sinusoidal. Moreover, it is noticeable that different load currents are drawn from each phase since the non-linear loads connected at the PCC are unbalanced. However, the currents supplied by the source are almost balanced. The harmonic spectra and the THDs of the load and source currents are also shown in Fig. 12(f)–(h) for all three phases. Further, the magnitudes and THDs of the load and source currents for Case 2 are listed in Table III.

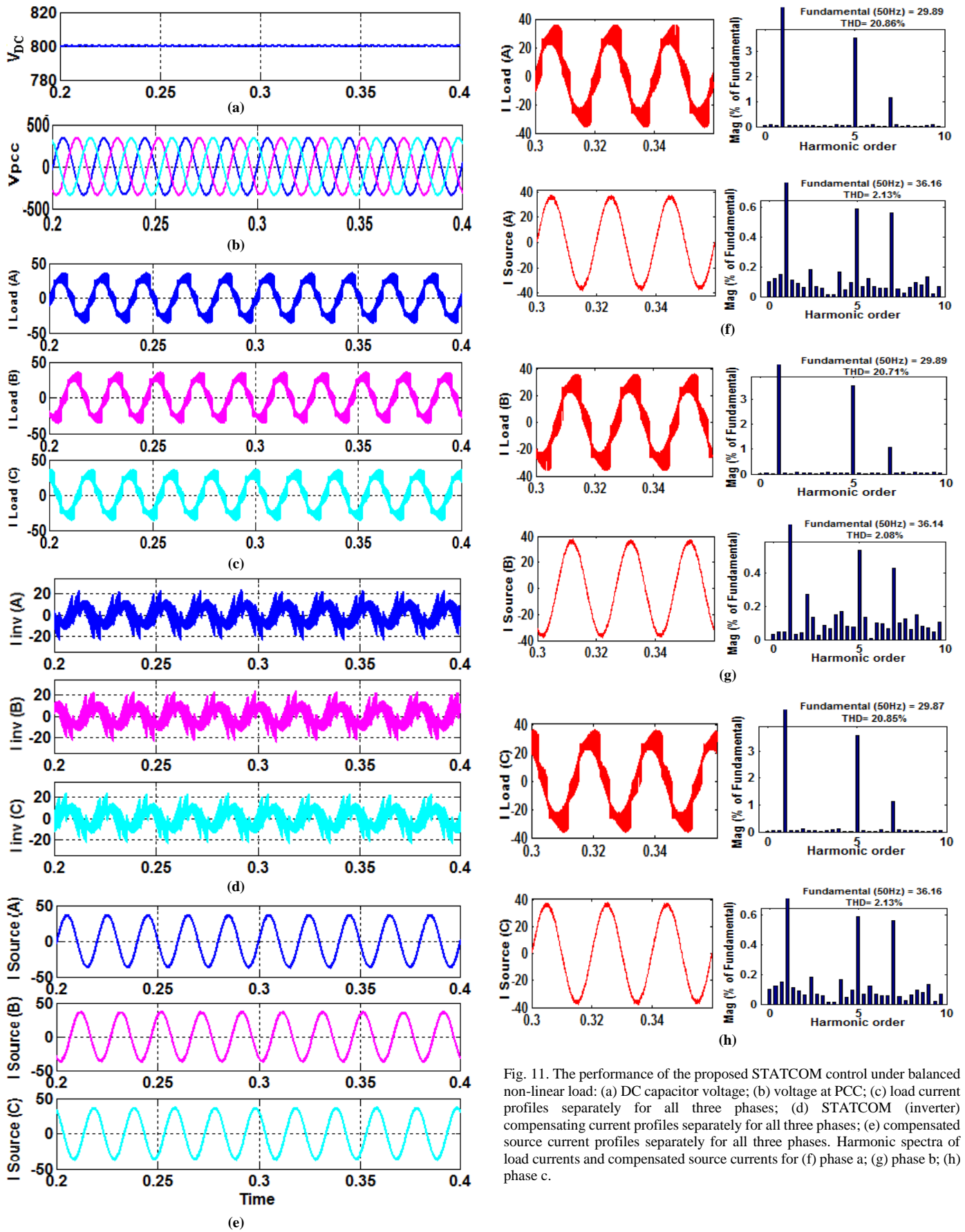


Fig. 11. The performance of the proposed STATCOM control under balanced non-linear load: (a) DC capacitor voltage; (b) voltage at PCC; (c) load current profiles separately for all three phases; (d) STATCOM (inverter) compensating current profiles separately for all three phases; (e) compensated source current profiles separately for all three phases. Harmonic spectra of load currents and compensated source currents for (f) phase a; (g) phase b; (h) phase c.

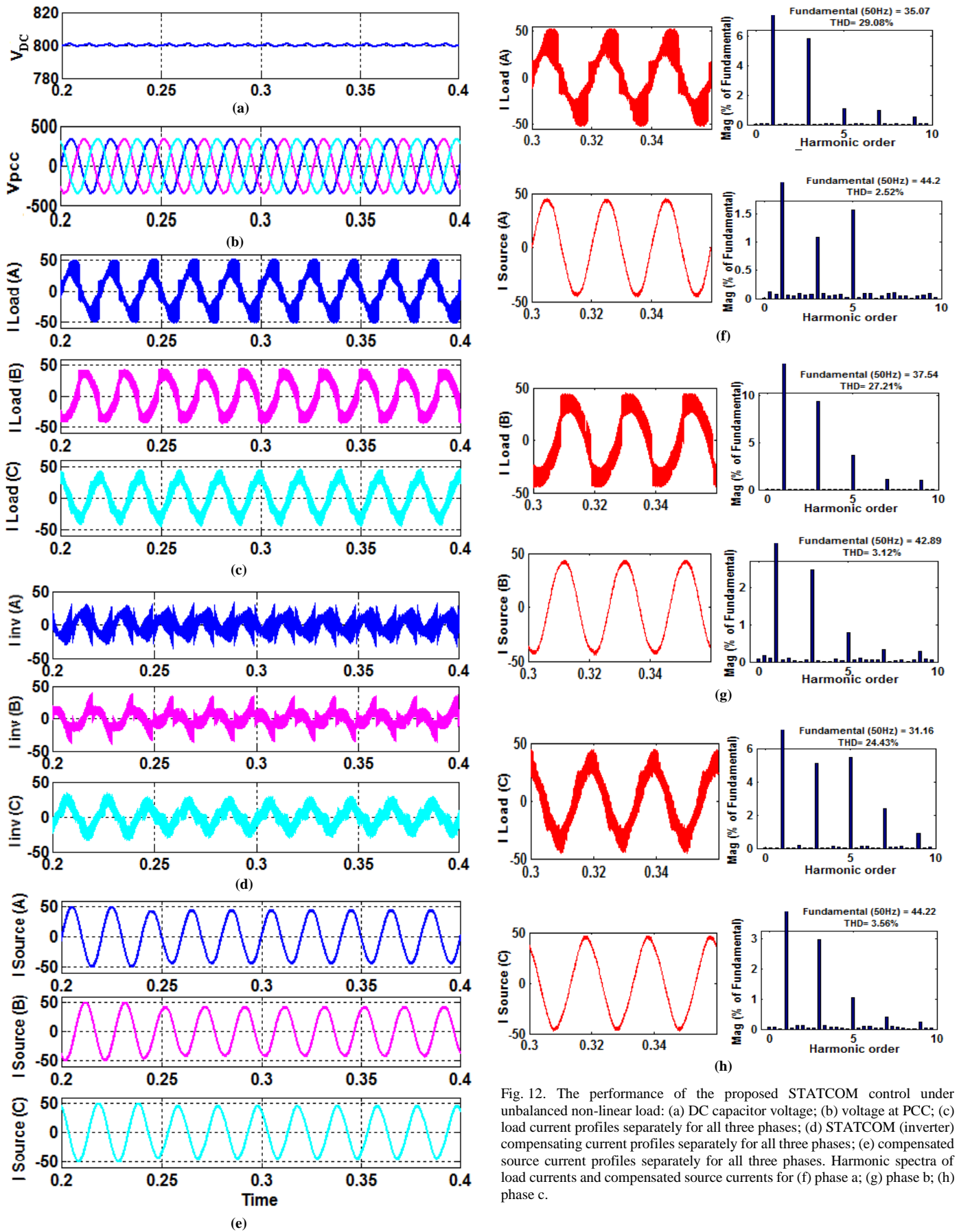


Fig. 12. The performance of the proposed STATCOM control under unbalanced non-linear load: (a) DC capacitor voltage; (b) voltage at PCC; (c) load current profiles separately for all three phases; (d) STATCOM (inverter) compensating current profiles separately for all three phases; (e) compensated source current profiles separately for all three phases. Harmonic spectra of load currents and compensated source currents for (f) phase a; (g) phase b; (h) phase c.



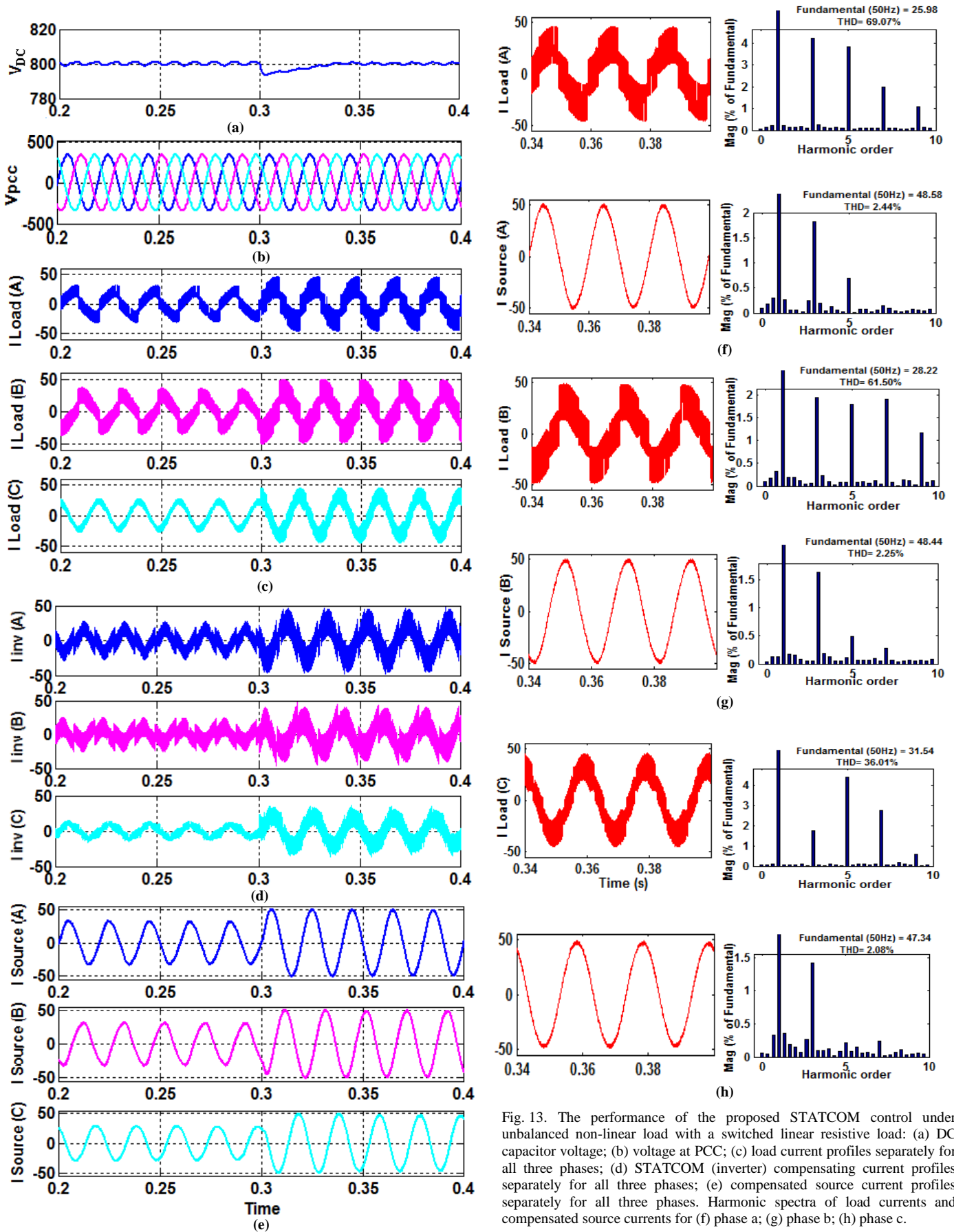


Fig. 13. The performance of the proposed STATCOM control under unbalanced non-linear load with a switched linear resistive load: (a) DC capacitor voltage; (b) voltage at PCC; (c) load current profiles separately for all three phases; (d) STATCOM (inverter) compensating current profiles separately for all three phases; (e) compensated source current profiles separately for all three phases. Harmonic spectra of load currents and compensated source currents for (f) phase a; (g) phase b; (h) phase c.

### Case 3: Performance Under Unbalanced Non-Linear Load With a Switched Unbalanced Linear Resistive Load

In this case, the performance of the proposed STATCOM control method is analysed under unbalanced non-linear load with a switched unbalanced linear resistive load. The non-linear load is constituted by three single-phase diode-rectifiers connected between the phases a–b, b–c and c–a, respectively; which separately feed impedances of different values, i.e.  $(40 + j3.141) \Omega$ ,  $(35 - j0.318) \Omega$  and  $(30 + j1.57) \Omega$  at the DC sides, respectively. Further, a three-phase unbalanced linear resistive load constituted by three resistances of different values, i.e.  $25 \Omega$ ,  $30 \Omega$  and  $35 \Omega$ , is additionally connected between the phases a–b, b–c and c–a, respectively, by closing the circuit breaker at time  $t = 0.3$  s. It is worth noting that even after connecting balanced linear resistive loads additionally in this case, the nature of the entire loads connected at the PCC remains non-linear and unbalanced.

TABLE III

MAGNITUDE AND THDS OF LOAD AND SOURCE CURRENTS IN DIFFERENT CASES

| Case   | Phase | Load current           |        | Source current         |        |
|--------|-------|------------------------|--------|------------------------|--------|
|        |       | Mag. of fundamental, A | THD, % | Mag. of fundamental, A | THD, % |
| Case 1 | a     | 29.89                  | 20.86  | 36.16                  | 2.13   |
|        | b     | 29.89                  | 20.71  | 36.14                  | 2.08   |
|        | c     | 29.87                  | 20.85  | 36.16                  | 2.13   |
| Case 2 | a     | 35.07                  | 29.08  | 44.20                  | 2.52   |
|        | b     | 37.54                  | 27.21  | 42.89                  | 3.12   |
|        | c     | 31.16                  | 24.43  | 44.22                  | 3.56   |
| Case 3 | a     | 25.98                  | 69.07  | 48.58                  | 2.44   |
|        | b     | 28.22                  | 61.05  | 48.44                  | 2.25   |
|        | c     | 31.54                  | 36.01  | 47.34                  | 2.08   |

It can be observed from Fig. 13(a) that the capacitor voltage is almost maintained at its reference value, i.e. 800 V, except at time  $t = 0.3$  s when a dip in the DC capacitor voltage is apparent for a very small period of time due to the addition of the three-phase unbalanced resistive load at the PCC. The three-phase

PCC voltage remains sinusoidal (see Fig. 13(b)). The non-linear load current profiles for all three phases are shown separately in Fig. 13(c). Even at unbalanced non-linear load with a switched unbalanced linear resistive load condition, it can be observed that the non-linear load currents are effectively compensated by the STATCOM before and after switching. The compensating STATCOM current profiles for all three phases are shown separately in Fig. 13(d). Fig. 13(e) shows the compensated source current profiles, which are nearly sinusoidal in this case as well, however, the current magnitudes increase after time  $t = 0.3$  s due to the addition of the three-phase unbalanced resistive load at the PCC.

Besides, it is noticeable that different load currents are drawn from each phase since the total loads connected at the PCC remain unbalanced. However, the currents supplied by the source are almost balanced. The harmonic spectra and the THDs of the load and source currents are also shown in Figs. 13(f)–(h) for all three phases. Further, the magnitudes and THDs of the load and source currents for Case 3 are listed in Table III. A close observation of Figs. 11–13 and keeping in mind the facts tabulated in Table III confirms that the proposed control method regulates the STATCOM in such a way that only the active current component is drawn from the source and the non-linearity in the load current profile due to the presence of the harmonic and reactive current components is compensated by the STATCOM.

Furthermore, the capability of the proposed STATCOM control in order to support reactive power during a voltage sag has been shown in Fig. 14. The grid codes are primarily intended to meet the technical requirements regarding the interconnection of distributed resources to the utility grid, a critical review of which is performed in [47], [48], specifically considering the several standard grid codes from different countries such as the E.ON Netz (German) grid code [49], the Nordic Grid Code [50], the grid codes of Denmark [51] as well as several other grid codes from Italy, Sweden, Spain and New Zealand etc.

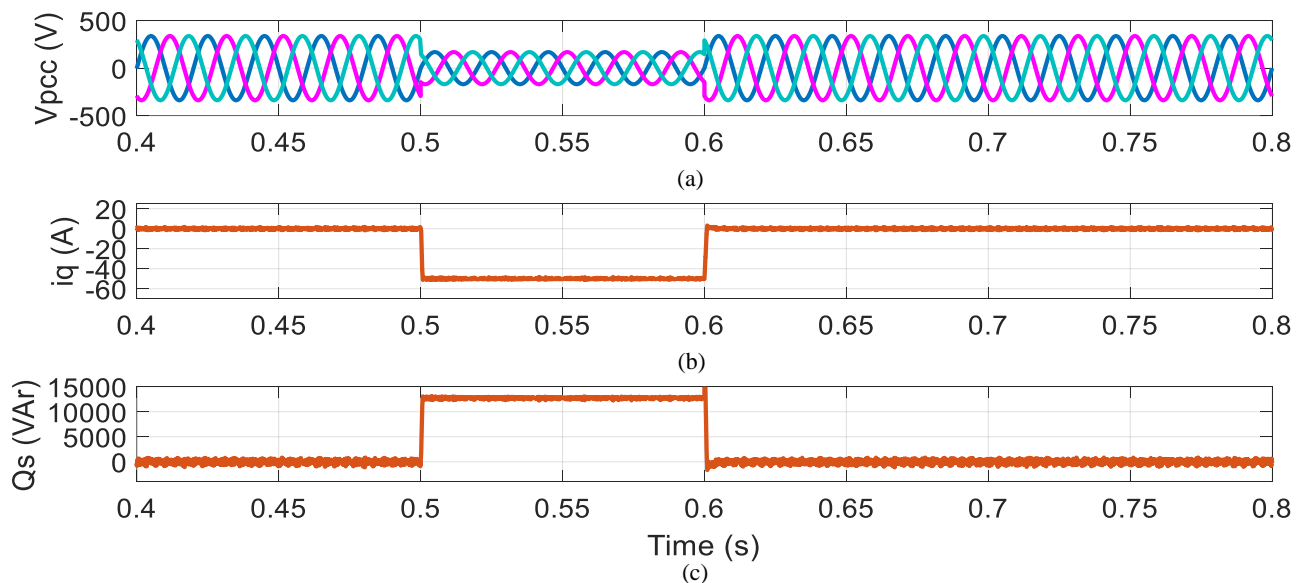


Fig. 14. Capability of the proposed STATCOM control for supporting reactive power during a voltage sag condition: (a) voltage at PCC; (b)  $q$ -axis source current component (reactive current); (c) reactive power support to the source (grid).

The reactive power support to the source (grid) can simply be achieved by varying the reference value of the source quadrature current component as demanded by the utility operator strictly following standard grid codes. For example, as per the E.ON Netz (German) grid code [49], it is required to support reactive current in the amount of 100 % of the rated system value when there occurs a voltage sag of 50 % at the PCC. As depicted in Fig. 14(a), there occurs a voltage sag of 50 % at the PCC at time 0.5 s for a duration of 100 ms. At this moment, as stated above, the reference value of the source quadrature current component in the STATCOM control is set at about  $-50$  A. It can easily be seen that initially, no reactive power was exchanged between the source and the STATCOM; however, a support of about 12.5 kVAr reactive power to the source is noticed during the voltage sag (see Fig. 14(c)).

## VII. CONCLUSION

A simple structure of the indirect current control strategy for a VSC-based STATCOM was discussed for harmonic and non-linear load compensation. Sizing of various system components was carried out. The PI controllers used in the inner and outer control loops were tuned using the ‘modulus optimum’ and ‘symmetric optimum’ criteria, respectively. In order to demonstrate a better harmonics tracking capability of the proposed STATCOM control method, three cases were presented and analysed, using MATLAB simulation. Even during load perturbation (Case 3), a very small variation in the DC capacitor voltage of the STATCOM was observed, which points to better system performance. The THDs of the compensated source currents in all three cases considered were also found to be under the limits as per the IEEE-519 standard. The capability of the proposed STATCOM control to support reactive power during a voltage sag condition was also highlighted. In this way, as validated by the simulation, the performance of the proposed STATCOM control method with tuned PI controllers was found to be responding satisfactorily.

## ACKNOWLEDGMENT

The work presented in this paper was supported by WBTEQIP-II at KNIT, Sultanpur, by providing the seed money grant for the P.G. Project under the “Research Promotion Scheme” (No. 369/WBTEQIP/2015).

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**Saurabh Mani Tripathi** was born in Amethi (U.P.), India, and is currently working as Assistant Professor of Electrical Engineering at Kamla Nehru Institute of Technology, Sultanpur (U.P.), India. He obtained his B. Tech. degree in electrical & electronics engineering and did his M.Tech. in electrical engineering with specialisation in power electronics & drives from Uttar Pradesh Technical University, Lucknow, India, in the years 2006 and 2009, respectively. He obtained his Ph. D. degree in electrical engineering from Dr. A. P. J. Abdul Kalam Technical University, Lucknow, India, in the year 2016. He has authored three engineering books and has published over 40 research papers in reputed international/national journals as well as at conferences. He has also successfully concluded two research projects. He was honoured as "Author of the Month" in the January 2009 issue of "The Librarian Journal" published by Laxmi Publications, New Delhi, India. He has also gained recognition in Marquis Who's Who in the World (A Who's Who in America Publication). He has supervised over 18 dissertations of M. Tech. students. He is the recipient of IET Young Engineers Award 2018-19 presented by the Institution of Engineers, India. He is Member of the IE(I), IAENG, ISEE, WASET as well as Life Member of the ISTE. His areas of current interest include electrical drives, renewable energy systems and power quality. Address: Department of Electrical Engineering, Kamla Nehru Institute of Technology, Sultanpur – 228118, (U.P.), India E-mail: mani\_excel@yahoo.co.in



**Prakash Ji Barnawal** was born in Bhadohi, India, in 1991. He completed his B. Tech. degree from Galgotias College of Engineering & Technology (U.P.), India, in the year 2014, and M.Tech. degree in power electronics & drives from Kamla Nehru Institute of Technology (U.P.), India, in the year 2016. He is currently working as Assistant Professor of Electrical and Electronics Engineering at Noida Institute of Engineering and Technology, Greater Noida (U.P.), India. His fields of current interest include power quality, power electronics and

electric drives.

Address: Department of Electrical and Electronics Engineering,  
Noida Institute of Engineering and Technology, Greater Noida – 201306,  
(U.P.), India

E-mail: prakashbarnawal6@gmail.com