ARTIFICIAL SATELLITES, Vol. 47, No. 1 – 2012

DOI: 10.2478/v10018-012-0009-7

SOME CONSIDERATIONS IN DESIGNING A GPS PSEUDOLITE

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ABSTRACT. Pseudolites are transmitters of GPS-like signals placed on the ground. Though pseudolites are well known devices and have already been used in the project where visibility to the GNSS satellites is limited, there are still many issues that need enhancement. A prototype of a low-cost pseudolite is being designed and assembled at the University of Warmia and Mazury. This will allow for conducting tests with various codes, signals and software. The goal of the project is to apply the pseudolite as an augmentation to GNSS positioning tasks in geodetic engineering projects. Some practical considerations crucial for the design are discussed in this paper.

Keywords: pseudolite, GPS signal transmitter

1. INTRODUCTION

Pseudo-satellites or, pseudolites are transmitters of GPS-like signals placed on the ground. They are useful either as stand alone systems, for example, in indoor navigation [Progri et al.(2001)], or navigation on other planets [Lemaster and Lemaster(2005)] or as augmentation to GNSS positioning in navigation of vehicles [Brekke and Company(2008)] and in monitoring structural deformation [Dai et al.(2000)] and ground deformation [Chrzanowski(2007)] in areas of limited visibility to the satellites. Though pseudolites are well known devices, there are still many issues that need investigation and enhancement. For example, enhancement of signal structure, navigation message structure, linearization problem, near-far problem, GNSS integration and many others. To investigate these problems, one has to have a full access to all pseudolite parameters (in particular: PRN code generated, transmitt power, navigation message, pulsing scheme). Therefore, the authors have decided to design and build a pseudolite within a research program on the development of new techniques for geodetic engineering projects at the University of Warmia and Mazury (UWM). This will allow for conducting tests with various configurations of hardware modules and software parameters: PRN codes, methods of near/far mittigation, receivers and types of navigation message.

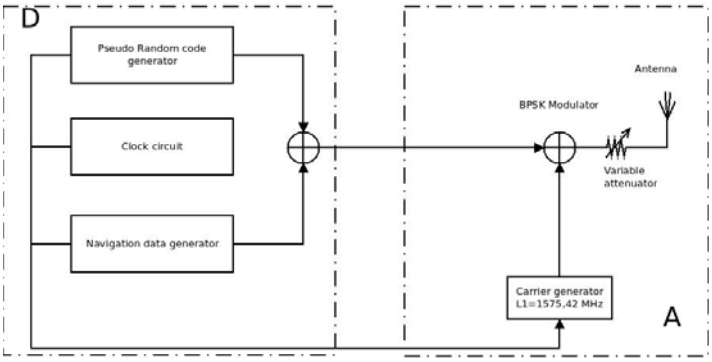


Figure 1: Overall design of a pseudolite

2. THE DESIGN

After analyzing all possibilities, the authors decided to build a pseudolite on the basis of the *Field Programmable Gate Array (FPGA)*. It will allow for modifying the software during the tests. The analog part of the proposed device is designed and built at UWM. The overall design of the pseudolite is depicted in Figure 1. It will consist of two main parts — digital and analog. The analog part will generate carrier wave and will provide Binary Phase Shift Keying (BPSK) modulation and transmission of the signal. The digital part will be responsible for code and navigation data. In Figure 1, D stands for digital and A for analog. Figure 2 depicts a functional block diagram of pseudolite.

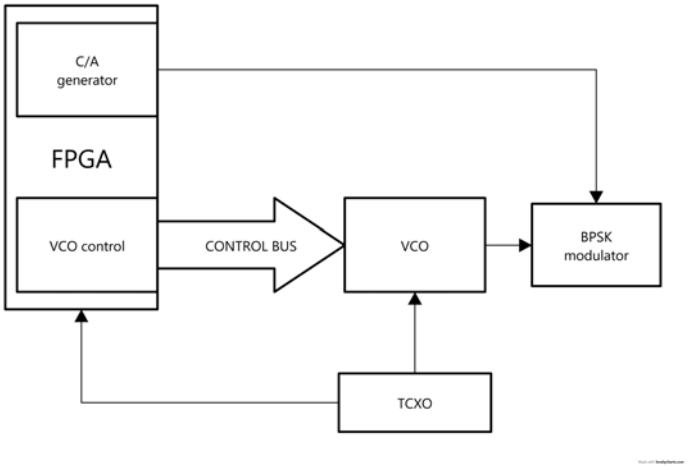


Figure 2: Functional block diagram of pseudolite

3. DIGITAL PART

3.1. HARDWARE

Instead of designing a new circuit board, a DE0 evaluation kit from TerasIC (TerasIC, 2010) will be used. It is a development board of a compact size designed with all the essential tools for FPGAs. The parameters of this kit are listed in Table 1.

Table 1: DE0 parameters [TerasIC(2010)]

Parameter	Description
FPGA device	Altera Cyclone III
Speed grade	C6
FPGA logic element (LEs)	15.408
SDRAM	8 MB
FLASH	4 MB
SD card socket	Yes
VGA	4-bit Resistor Network
USB Blaster	Built-in
RS-232	Optional
PS/2	Yes
LEDs	10
Toggle Switches	10
Push Buttons	3
Expansion ports	2 x 40-pin

Logic element resources on DE0 are sufficient to implement the digital part of the pseudolite. Occupancy of FPGA resources for each functional block are presented in Table 2. It shows that about 93% of logic elements can be used for navigation data generator. Estimations done earlier show that it is enough to implement such functionality. Additionally, dynamic phase shift in the PLL (*Phase Lock Loop*) circuits can be implemented.

Table 2: Occupancy of FPGA resources

Functional block	Total logic elements	Memory	PLL
PRN generator	5%	0	1
Interface to ADF4350	$< 1\%$	0	1
User interface	$< 1\%$	0	0

3.2. NAVIGATION DATA AND PRN GENERATOR

Both C/A code and navigation data generator belong to digital part of pseudolite. So, it can be realized using a microprocessor, CPLD (*Complex Programmable Logic Device*) or FPGA. The procedure of the code and navigation message generation is described in [Bao-Yen(2005), Borre et al.(2007)].
The C/A code is a relatively short pseudo–random (PRN) binary code (it consists of 1023 bits) used in civil applications. Pseudo–random means that it has random characteristics

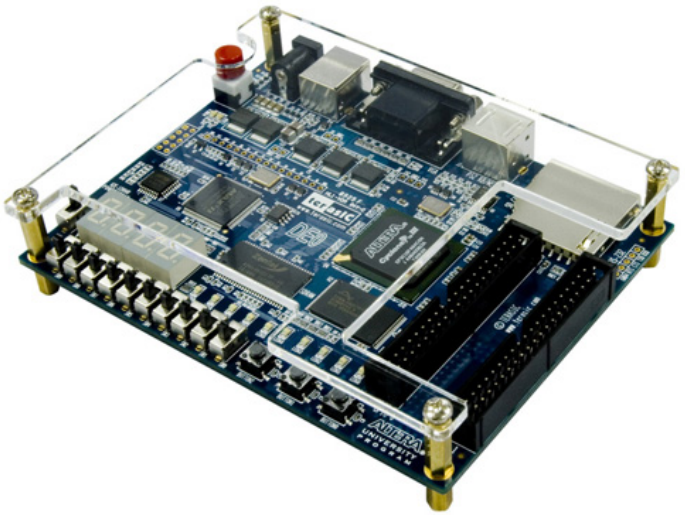


Figure 3: TerasIC DE0 board [TerasIC(2010)]

but it is generated according to the GPS signal specifications [U.S. Department of Defense (1995)]. These codes are a product of two 1023 bits PRN codes:

$$XG(t) = G1(t)G2[t + N_i(10T_C)] \tag{1}$$

Every $G1$ and $G2$ code is generated by the 10 stage, maximal–length linear shift register. These codes are used because they provide uniformly low cross correlations [Parkinson and Spilker(1996)]. Thanks to this properties the PRN codes provide the possibility to measure pseudoranges.

The C/A code is unique for each satellite. For the pseudolite each of the codes used by satellites may be generated, or additional code may be admitted. Since additional PRN code would require modification of the receiver, the PRN code for such a satellite that is not in view will be used.
C/A code generator can be built using D flip-flops and XOR gates. The data (D) flip-flop tracks the input, making transitions with match those of the input data. XOR is a well known digital logic gate that implements an exclusive or operator.It returns a true output results if one, and only one, of the inputs to the gate is true. In the oposite case it returns a false output. In the presented design the above C/A code generator is implemented on the FPGA. The major advantage of such an approach is that it has a built in PLL blocks which are able to generate 1.023 MHz clock signal from external TCXO. Additionally we can implement software responsible for control of ADF4350 through control bus. Logic gate resources available in FPGA are sufficient for generation of all C/A codes and navigation message simultaniously. One disadvantage of using FPGA devices is that their packages requires a multilayer PCB (*Printed Circuit Board*). It has an impact on a cost of pseudolite. Therefore on the prototyping stage the DE0 development boards from TerasIC was used.

The navigation data is transmitted as five, 6 seconds long, sub–frames for a total of 30 s frame period (1 bit of data is transmitted every 20 ms). This data stream is modulo–2 added to the C/A code on L1 frequency. The sub–frames 1, 2 and 3 are required as a minimum for a navigation solution [Parkinson and Spilker(1996)].

4. ANALOG PART

4.1 L1 CARRIER GENERATOR

The L1 carrier generator is a RF part of the GPS transmitter. It can use a wideband synthesizer with integrated Voltage Controlled Oscillator. Currently, there are several circuits available commercially. In this project, an ADF4350 from Analog Devices was used because of easy implementation and satisfactory parameters like phase noise and output power of +5dBm which is sufficient for BPSK modulator based on Double Balanced Mixer. Additionally RF outputs of ADF4350 can be muted. It makes implementation of pulsed pseudolite very easy (pseudolite signal pulsing is a technique of near/far problem mitigation). Spectrum of signals generated by such integrated circuit is shown in Figure 4.

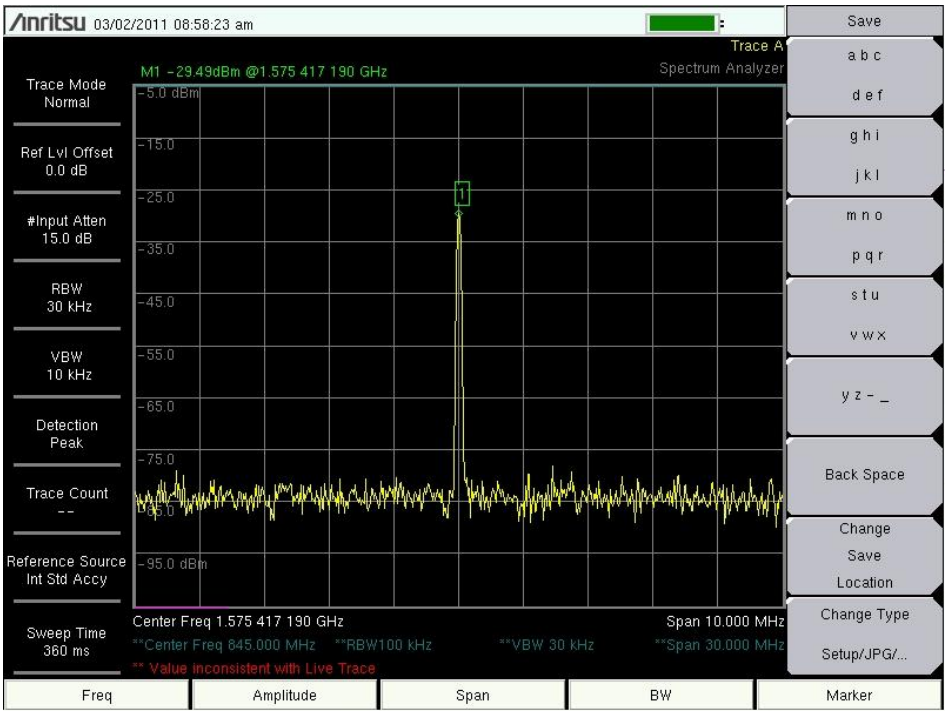


Figure 4: Spectrum of L1 carrier generated by ADF4350

Frequency measured is $f_z = 1575.417190MHz$. The difference between GPS L1 frequency $1575,42MHz$ is:

$$|\Delta f_{L1}| = |f_{L1} - f_z| = 0.00281[MHz] = 2.81[kHz] \tag{2}$$

which is:

$$\frac{\Delta f_{L1}}{f_{L1}} \times 100\% = \frac{0.00281}{1575.42} = 1.783 \times 10^{-4}\% \tag{3}$$

After restarting the ADF4350 the frequency was $f_z = 1575,421818MHz$:

$$|\Delta f_{L1}| = |f_{L1} - f_z| = 0.00182[MHz] = 1.82[kHz] \tag{4}$$

which is:

$$\frac{\Delta f_{L1}}{f_{L1}} \times 100\% = \frac{0.00182}{1575.42} = 1.154 \times 10^{-4}\% \tag{5}$$

This value of deviations from the L1 frequency should be irrelevant for the receiver. According to [Cobb(1997)], the maximum expected Doppler shift is 6 kHz. The values generated with our circuit is much below this, so the commercially available GPS receivers should be able to track the pseudolite's signal. Figure 5 shows the spectrum of the signal with the max–hold function. It shows the fluctuation of the signal within a few hundreds Hertz. Also two, about 63dB smaller, spur frequencies are visible. The power of spur frequencies is 2×10^6 times weaker then the center frequency. Hence entire bandwidth will be attenuated to match the GPS satellites signal level, spur frequencies are considered neglible.

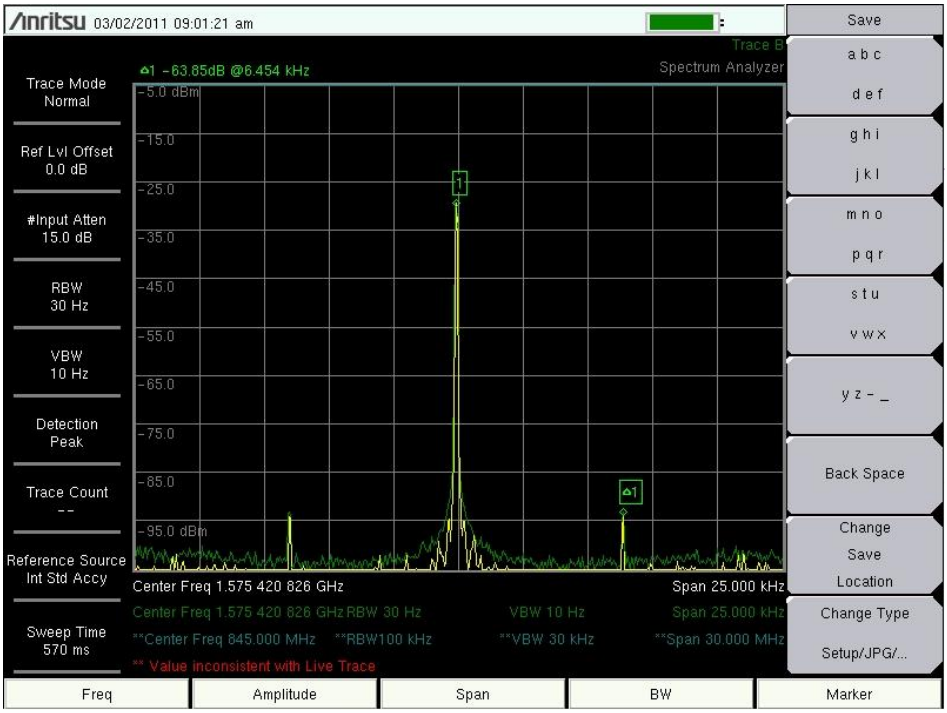


Figure 5: Spectrum of L1 carrier generated by ADF4350 with max—hold.

4.2 BPSK MODULATOR

To transmit the data, the carrier of the GPS signal is modulated using BPSK (a.k.a. PRK — Phase Reversal Keying, or 2PSK). It is the simplest form of phase shift keying (*PSK*) modulation. It uses two phases separated by 180 degrees. So, whenever a rising edge in the digital signal occurs, the phase of the carrier is shifted by 180 degrees. The principle of BPSK modulation is depicted in Figure 6.

The modulator can be realized as a pin diode BPSK modulator or as a dedicated integrated circuit. RF2638 from RF Micro Devices or ADE-2M are the examples of the

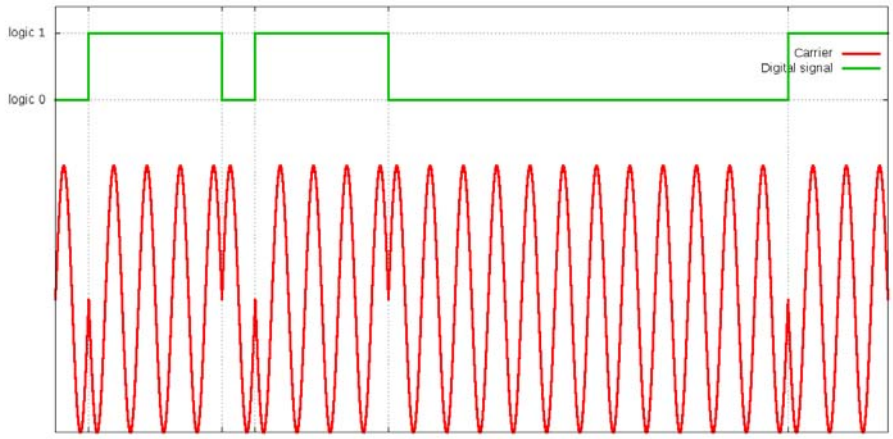


Figure 6: BPSK modulation.

integrated modulators. Each of them has an input for a local oscillator (LO) (in our case it is an L1 carrier) and two inputs IF+ and IF- for data (where IF- is a negation of IF+). Following parameters have to be considered when choosing a modulator:

- frequency range of LO input ,
- frequency range of RF output,
- IF input frequency,
- return loss at LO input.

For the L1 signal, the range of L0 input and RF output frequencies must enclose 1.575420 GHz and the IF input frequency must be grater then 1.023MHz. The last parameter describes the internal attenuation of a modulator. It is of a minor importance, since output RF signal from the modulator must be attenuated further to match the GPS satellites signal level. The attenuator must be used between the digital part and modulator because maximum acceptable input level for mixer data input is smaller than the combined signal including navigation message and C/A code.

4.3 SIGNAL ATTENUATION

The BPSK modulator accepts signals up to 2dBm. On the output there is about 0dBm. Since the signal from the satellites is about -120dBm at receiver, there is a necessity to attenuate the pseudolite signal. Therefore, the variable attenuator is placed between the BPSK modulator and the antenna. The necessity to attenuate the signal is caused by the near/far effect. If 0dBm signal would occur in receiver, then it is obvious that the receiver would not be able to track much weaker satellite signals [Cobb(1997)].

5. PRACTICAL CONSIDERATIONS

5.1 CLOCK

The main role of the clock circuit is to provide appropriate clock signals to pseudo random code generator, carrier generator and Navigation Data generator. The main relation between different clock frequencies used in GPS signals is shown in Table 3.

Clock signal name	Relation to main frequency	Frequency [MHz]
Main frequency fMAIN	f	10.23
C/A code frequency fC/A	$\frac{f}{10}$	1.023
P code frequency fP	$1 \times f$	10.23
P(Y) code frequency fP(Y)	$\frac{f}{20}$	0.5115
Carrier frequency L1 fL1	$154 \times f$	1575.42
Carrier frequency L2 fL2	$120 \times f$	1227.60
Navigation message frequency fNM	$\frac{f}{204600}$	$50x10^{-6}$

Table 3: Clock frequencies used in GPS signal

The accuracy of the position designation in GPS strongly depends on the accuracy of this frequency. Therefore, atomic clocks are used in GPS satellites. This kind of frequency source is not practical in pseudolite applications due to the high cost. The other possibility is to use a quartz oscillator source. There are many possible frequency sources: starting from rubidium oscillators up to crystal clock sources like TCXO or OCXO. Rubidium clock is the most stable, but it is expensive, relatively large and difficult in implementation into a packed device. In [Cobb(1997)] it have been proven that TCXO oscillators are stable enough for such an application. Another important parameter of clock source is it's nominal frequency. To achieve a required frequency of PLL (*Phase Lock Loop*) in FPGA two parameters must be specified (m,n). The range of these parameters is limited by FPGA manufacturer [Altera(2009)]. In general the output frequency can be described by the following equation:

$$f_{out} = \frac{m}{n} f_{in} \tag{6}$$

In the case of a C/A code pseudolite, the 1.023MHz frequency is required. In proposed design the frequency of TCXO $f_{in} = 16.368MHz$. Hence setting $m = 1$ and $n = 16$ results in the frequency of C/A code. Similar situation is in the case of carrier frequency generated by VCO. For the INT, FRAC, and MOD values, make it possible to generate output frequencies that are spaced by fractions of the f_{PFD} frequency. The RF VCO frequency (RF_{OUT}) equation is:

$$RF_{OUT} = f_{PFD} INT + \frac{FRAC}{MOD} \tag{7}$$

where RFOUT is the output frequency of external voltage controlled oscillator (VCO). INT is the preset divide ratio of the binary 16-bit counter (23 to 65535 for 4/5 prescaler, 75 to 65,535 for 8/9 prescaler). MOD is the preset fractional modulus (2 to 4095). FRAC is the numerator of the fractional division (0 to MOD - 1).

$$f_{PFD} = REF_{IN}\frac{1+D}{R(1+T)} \tag{8}$$

where REFIN is the reference input frequency, D is the REFIN doubler bit, T is the REFIN divide-by-2 bit (0 or 1), R is the preset divide ratio of the binary 10-bit programmable reference counter (1 to 1023) [ADF4350(2011)] The chosen oscillator will be a source of signal which synchronizes the work of all the circuits in the pseudolite. There is a wide range of oscillators that can be used. Some of them are capable to generate exactly 10.23 MHz, but some of them generate different frequencies. So, to provide a required frequencies Phased Locked Loop or frequency synthesizers can be used. These circuits are able to convert input signal from oscillator with fIN frequency to signal with different frequency fOUT. Depending on the oscillator chosen our main frequency fMAIN can be the input fIN or output fOUT signal. Using the PLL or the synthesizers has the following advantage — they can have a few independent outputs that can generate different frequencies. It is depicted in figure 7.

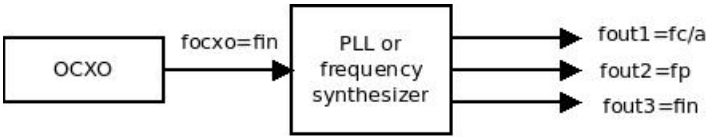


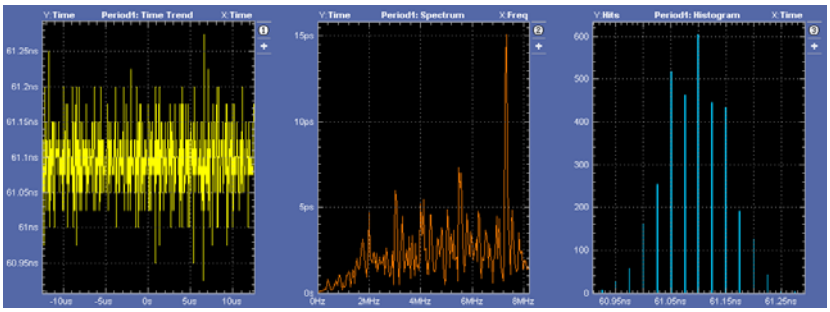
Figure 7: Block diagram of sample clock circuit

The input to the frequency synthesizer comes from the OCXO (*Oven Controlled Crystal Oscillators*).

5.2 JITTER

Besides the frequency stability, the jitter of each clock is an important parameter of clock circuit. Generally jitter is a deviation of rising and falling edge of the signal from their ideal location in time. More details about jitter can be found in [Ong et al.(2004)]. The graphical representation of the jitter is depicted on figure 8(a). Solid line shows the ideal signal location in time. Dashed lines are deviation of both edges of the signal.The histogram below shows jitter distribution. As it can be seen a small deviation occurs more often than higher deviation. The example histogram from a measurement of TCXO is shown on figure 8(b). The presence of jitter has impact on the modulated signal because period for L1 carrier is 634.75 ps and for L2 carrier 814.59 ps. In case of jitter comparable to carrier period, errors in signal may occur – high jitter values may cause lost of C/A code tracking in the receiver. This might be caused by a loss of synchronization between nominal C/A code chip frequency and actual code frequency generated by FPGA.

(a) Rising edge jitter



(b) Histogram of jitter

Figure 8: Signal jitter example

6. CONCLUSION

The presented above aspects of a pseudolite design should allow for building a flexible and cost effective device. When the pseudolite prototype is ready, a number of tests will be performed. First tests will include a careful inspection of the generated signal, which will be carried out with a precise spectrum analyzer. It will include a test of carrier frequency stability, correctness of C/A code and navigation message, test of transmitted signal level, antenna patterns etc. After the signal meets all the requirements, the next step will include actual positioning experiments. Several models of GNSS receivers will be used in the field tests in order to select the best matching GPS/pseudolite pair. After a successful set up of the equipment, various experiments will be conducted in actual geodetic engineering projects in which GNSS survey will be augmented by pseudolites to increase positioning accuracy, speed up an ambiguity resolution and increment GNSS signal availability in harsh survey environment.
Currently the pseudolite prototype development is at the stage of signal testing. We have successfully tracked it's signal with a software receiver. Both carrier phase and code ranges were observed. Test of the quality of recorded signals will be performed in the next step.

ACKNOWLEDGEMENT

The authors would like to acknowledge that the described research has been sponsored by Ministry of Science and Higher Education grant number N N526 229139.

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Received: 2011-09-13,

Reviewed: 2012-01-19,

Accepted: 2012-04-02.