FAST RESPONSE, MEDIUM RESOLUTION DIGITAL EVENT TIMER AND RANGE GATE GENERATOR FOR SATELLITE LASER RANGING

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ABSTRACT. For our kHz Satellite Laser Ranging (SLR) system in Graz, we developed a fast response, medium resolution Event Timer to determine laser firing times; and a digital Range Gate Generator to activate the Single Photon Avalanche Detector (C-SPAD). The Event Timer has a resolution of about 500 ps, and determines the Event Times within 20 ns; the Range Gate Generator produces a range gate pulse with about 500 ps resolution, and with an accuracy of better than 1 ns. Both devices are fully digital, and are implemented within an FPGA circuit. These devices can be used in the present 2 kHz SLR system, as well as in future higher repetition rate SLR systems.

Keywords: Event Timer, FPGA, SLR, Range Gate Generator

INTRODUCTION

SLR systems use short laser pulses to measure distances between ground stations and retro-reflector equipped satellites to the millimeter level. These activities are coordinated within the International Laser Ranging Service (ILRS), supporting geodetic and geophysical research (Pearlman et al, 2002).

An SLR system consists of a laser, a telescope, a – single or multiple - photon detector (in Graz: C-SPAD) and a time of flight (TOF) measurement device. The TOF can be measured with 2 different methods: With a simple time interval counter, or with event timers.

Time interval counters are not applicable for kHz SLR, because due to the high repetition rate (some kHz) there are always more than 1 pulse – up to 300 pulses for high orbit satellites for a 2 kHz SLR system – simultaneously traveling between SLR station and satellite.

The high precision event timers determine laser firing epochs, and epochs of the returns independently; these epochs are then used to calculate the TOF. Because the ultra high precision Graz E.T. (< 2.5 ps) needs about 400 μ s to fix the event time (Kirchner et al, 2000), we developed a much faster (20 ns response time: The completed event time measurement is available within 20 ns after the event), but medium resolution (500 ps) event timer within the FPGA (Iqbal, 2008), dedicated – and accurate enough - for range gating purposes.

After detecting a laser start pulse event time, the expected return event time is calculated, and loaded into the Range Gate Generator; which then activates the detector short before arrival of the return photon(s). While this is done at present with a combination of a digital 100-ns-resolution FPGA counter PLUS a programmable analog delay chip, we implemented now a fully digital Range Gate Generator into the FPGA - using a 5-ns course counter, and a 500 ps vernier – to improve linearity and stability.

Both devices were implemented within the Altera FPGA Apex 20K chip on the Graz FPGA card.

2. EVENT TIMER IMPLEMENTATION

The fast response digital event timer is implemented using a well known vernier method. This method uses a 200 MHz counter and a vernier for the 5 ns intervals. The vernier uses standard AND gates with 500 ps transit time per gate (fig. 2). To implement a series of identical, cascaded delay gates we had to disable the automatic optimization of the Quartus Compiler for the Altera FPGA device.

The event pulse (e.g. Laser Start Pulse) starts traveling through several parallel chains of AND Gates; each chain consists of an increasing number of AND gates; the next following 5 ns clock pulse is used as a STOP pulse for this simple vernier (fig. 1).

Fig. 1. A digital vernier interpolates between 5 ns clock pulses.

Fig. 2. Event timer unit, using chains of AND delay gates of increasing length.

If the start pulse reaches the end of a chain BEFORE the STOP pulse, a “1” is latched into an output register; if not: a “0”... (Fig. 2). The bits in this output register represent a measure for the 0-5 ns interpolation; together with the latched actual reading of the 200 MHz coarse clock this forms a 500 ps resolution event time.

Simulation of such a circuitry gave promising results for the required speed and resolution of this Event Timer (fig. 3); therefore we implemented this event timer into the Graz ISA card FPGA; optimizing its floor plan layout to achieve optimal linearity and uniform resolution..

Fig. 3. (A) Vernier measurement, interpolating 5 ns intervals.

3. EVENT TIMER TEST RESULTS

We tested the temperature drift of a 100-AND-gate delay chain; it drifted with about 10 ps/C° (Fig. 5), which is quite acceptable considering the required resolution, and the location of the PC / ISA Card / FPGA in the air conditioned laser room.

Fig. 5. Delay of a 100-AND-Gates Delay Chain vs. Temperature.

To evaluate the FPGA event timer linearity, (fig 6: Test setup) we compared its results with those of our ultra high precision (1.2 ps resolution, < 2.5 ps non-linearity) Graz E.T. (Kirchner et al, 2004). The differences between both showed an RMS of 260 - 290 ps.

Fig. 6. Test setup to compare Graz E.T. and FPGA ET.

Although an event timing accuracy of < 300 ps is fully sufficient for the purpose of Range Gate Epoch determination, we tested possible improvements by implementing 4 such Event Timer Units in parallel (fig. 7) into the FPGA. All 4 event times are read by PC and averaged there; this average reduces the FPGA event timer jitter only to 217 ps RMS (instead of the theoretically expected values of about 140 ps), mainly due to the remaining non-linearities within the 5 ns interpolation interval.

Fig. 7. 4 Parallel Event Timers.

4. RANGE GATE GENERATOR

We used a 200MHz clock and a chain of AND gates to implement a Range Gate Generator (programmed via PC) - which generates a range gate pulse short before the actual return of the laser photons - with a resolution of about 500 ps and an accuracy of < 1ns.

The start pulse (fig.8) travels through the chain of AND gates. The output of each gate switches its associated D-Flip-Flop as soon as the start pulse has passed; only ONE out of these D-Flip-Flops is activated by the pre-programmable selection logic, and generates the Range Gate pulse (fig. 8).

Fig. 8. Block Diagram of Digital Range Gate Generator.

5. RANGE GATE GENERATOR TEST RESULTS

Our test setup (fig.9) used a DG535 Pulse Generator, a Stanford SR620 Time Interval Counter, and a GPS system (1 pps, 10 MHz) to test the linearity of the Range Gate Generator.

Fig. 9. Experimental set up for Range Gate Generator Evaluation.

We tried 3 different placements (floor plan layouts; both manual placements and/or automatical placements (Altera), of the AND gates and D-Flip-Flops within the logical cells) of the Range Gate circuitry inside the FPGA to find the optimum linearity (Fig.10); the selected final placement has the best R-squared value ("R2" in fig. 10) and linearity.

Fig. 10. Delay Time (ps) vs. Delay Chain Length – different placements of AND gates and D-Flip-Flops to optimize linearity.

CONCLUSIONS

The resolution and non-linearity of this FPGA Event Timer unit is more than adequate for our purpose of fast Range Gate setting; if higher resolution is required, a multi-channel Event Timer can be implemented. Due to its high speed – the result is available within 20 ns -, it is well suited for the existing 2 kHz SLR system, and also for systems with significantly higher repetition rates, (Sadovnikov, 2000).

This Digital Range Gate Generator is fully adequate for the present Graz 2 kHz SLR system, and we envisage it's use also for higher repetition rate SLR systems.

kHz SLR has gained vital interest within the SLR community, and these newly designed devices - FPGA event timer and range gate generator - can help to reduce implementation problems of of present and future high repetition rate SLR systems.

Acknowledgment

Special thanks to Higher Education Commission of Pakistan (HEC) for providing a PHD fellowship for Farhat Iqbal at SLR Graz for this study and research.

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Received: 2009-02-27,

Reviewed: 2009-07-22, by I. Procházka,

Accepted: 2009-08-03.