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# ON THE DESIGN OF CLASS-J MICROWAVE POWER AMPLIFIER

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**Abstract.** ***Due to the ISM band being unlicensed for communication applications, a lot of applications have been developed in this band and a good example is WiFi IEEE 802.11a, b, g, n of Bluetooth. This numeracy of applications motivated this paper. The paper is concerned with the design of a low distortion 20dBm 2.4GHz class-J power amplifier (PA) since PAs are indispensable in radio communications. The design is based on the AVAGO ATF-52189 transistor with a transition frequency of 6GHz. The design is done as a hybrid circuit network realized using microstrip elements and surface mount device (SMD) capacitors. The schematic design, and simulation are carried out using Keysight's Advanced Design System version 2016.01. The simulated PA exhibited a drain efficiency of 69% and a power output of 21dBm.***

Keywords: power amplifier, design, ADS

## 1. INTRODUCTION

Modern communication systems have evolved over the recent past and are still evolving largely in favor of wireless links especially at the last hop i.e. the access network. This is majorly because of the demand for mobility.

Wireless communication operates in the radio frequency (RF) range. The RF actually implies frequencies at which electromagnetic (EM) radiation is practical for communication purposes. These frequencies range from about 3 kHz to about 300 GHz.

A very recent concept is the internet of things that arguably increases the demand for wireless communication by orders of magnitude. It is justifiably estimated that the number of smart devices connected to communication networks will far outnumber the human population in a few years' time.

This demand means that the PA designer at RF frequencies has to keep PAs performing exceptionally well especially in terms of bandwidth and efficiency. Wide bandwidth is required to support the various applications, services and capabilities from new mobile equipment. Obviously mobile equipment is battery powered and this makes power efficiency a very crucial consideration in RFPA design.

The power amplifier has a power output that necessarily far outweighs the input power driving the amplifier. Strictly speaking however, there is no such thing as power amplification and a more accurate description would be that a 'PA' is really an AC controlled DC to AC power converter.

PAs differ from small signal amplifiers by way of quality and quantity of signal emphasized by the designer. Small signal amplifier designers are concerned with low noise and low distortion amplification i.e. linear amplification. In short, small signal amplifier designers are obsessed with linearity. PA designers on the other hand seek to maximize power output as efficiently as possible even at the expense of linearity. The load line matching concept at the output is therefore preferred to conjugate matching. Aptly then, PA designers are obsessed with power efficiency. Recent works on PA design can be found in [1-8].

## 2. DESIGN METHODOLOGY

### 2.1 Active device

The ATF-52189 GaAs transistor was selected as the active device in the amplifier design. From the manufacturer AVAGO technologies, the datasheet was obtained from which some of the important absolute maximum ratings were extracted and are illustrated in Figure 1. All parameters in Figure 1 were adopted from AVAGO technologies [9] (the new name of AVAGO technologies is Broadcom Corporation).

| Symbol | Parameter | Units | Absolute Maximum |
|---|---|---|---|
| $V_{ds}$ | Drain–Source Voltage[2] | V | 7 |
| $V_{gs}$ | Gate–Source Voltage[2] | V | -5 to 1.0 |
| $V_{gd}$ | Gate Drain Voltage[2] | V | -5 to 1.0 |
| $I_{ds}$ | Drain Current[2] | mA | 500 |
| $I_{gs}$ | Gate Current | mA | 46 |
| $P_{diss}$ | Total Power Dissipation[3] | W | 1.5 |
| $P_{in\ max.}$ | RF Input Power | dBm | +27 |
| $T_{ch}$ | Channel Temperature | °C | 150 |
| $T_{stg}$ | Storage Temperature | °C | -65 to 150 |

**Thermal Resistance**[2,4]
$\theta_{ch\text{-}b} = 52°C/W$

**Notes:**
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Assuming DC quiescent conditions.
3. Board (package belly) temperature $T_B$ is 25°C. Derate 19.25 mW/°C for $T_B > 72°C$.
4. Channel-to-board thermal resistance measured using 150°C Liquid Crystal Measurement method.

**Figure 1. ATF-52189 absolute maximum rating**

### 2.2 Active device nonlinear model

An open parasitic model of the packaged ATF52189 was obtained from the manufacturer as an ADS schematic hierarchy illustrated in Figure 2, Figure 3, and Figure 4. All parameters in these figures were adopted from AVAGO technologies [9].

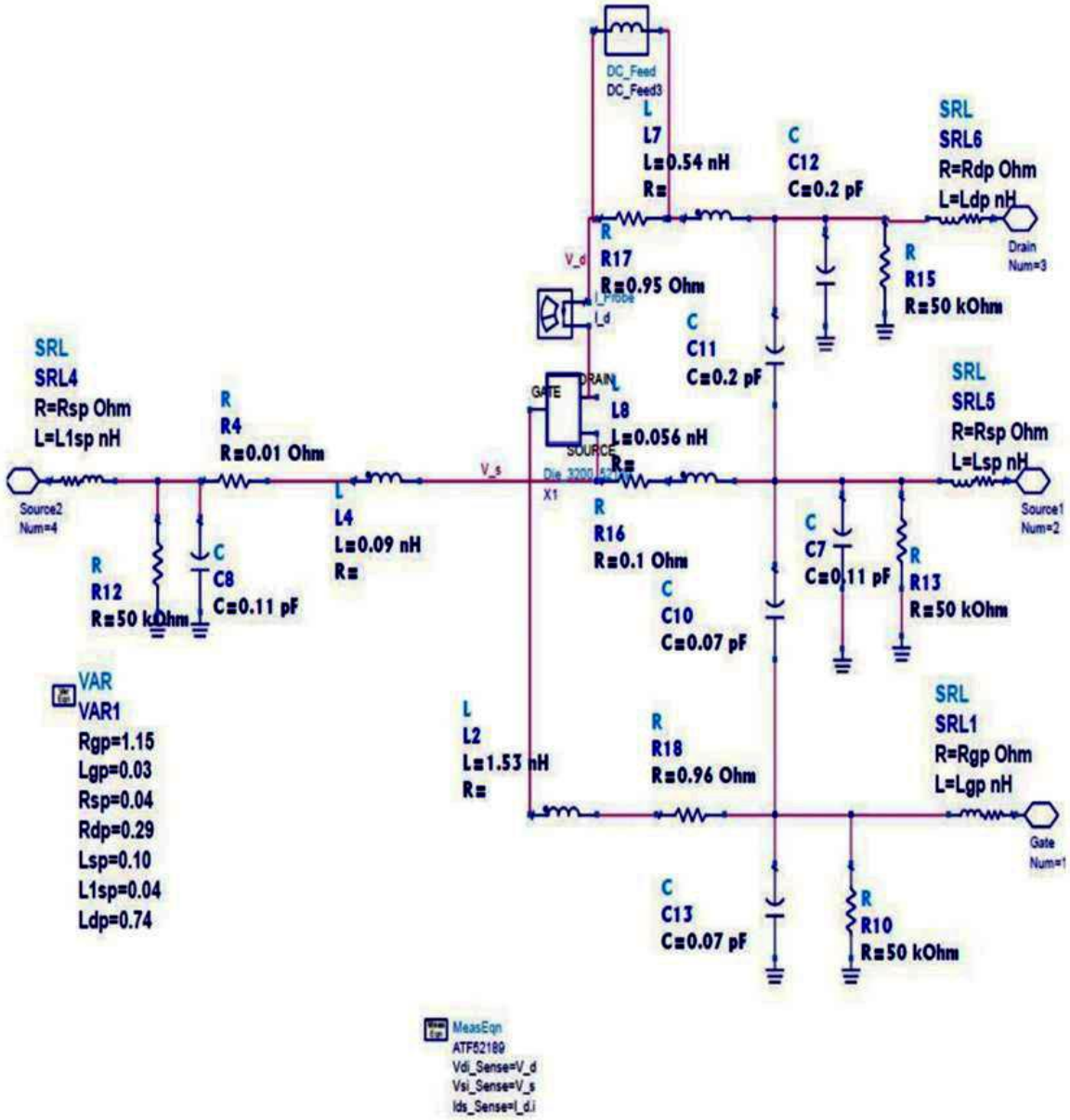



**Figure 2. Extrinsic model of the ATF-52189 obtained from AVAGO Technology**

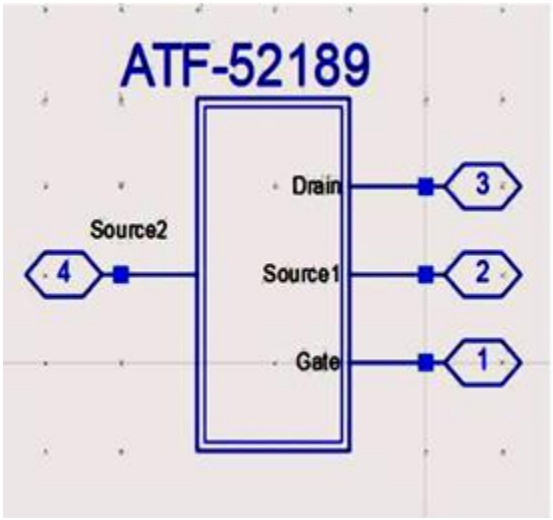



**Figure 3. Schematic symbol of the ATF-52189**

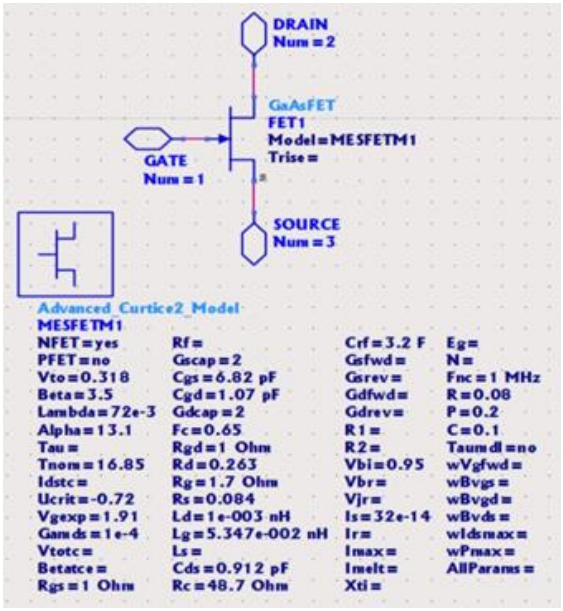



**Figure 4. Intrinsic model of the ATF-52189 obtained from AVAGO technologies**

## 2.3 DCIV characteristics and waveform prediction from a class B load-line

The schematic for obtaining the DCIV characteristics is illustrated in Figure 5. From the DCIV characteristics, a class B load-line was constructed from which the voltage swing and current swing were obtained. Based on these swings, class-J waveforms were predicted and plotted. The requisite fundamental and second harmonic impedances were obtained by Fourier techniques. These were the target impedances to be presented to the intrinsic drain of the device. Figure 3-5 illustrates the data display.

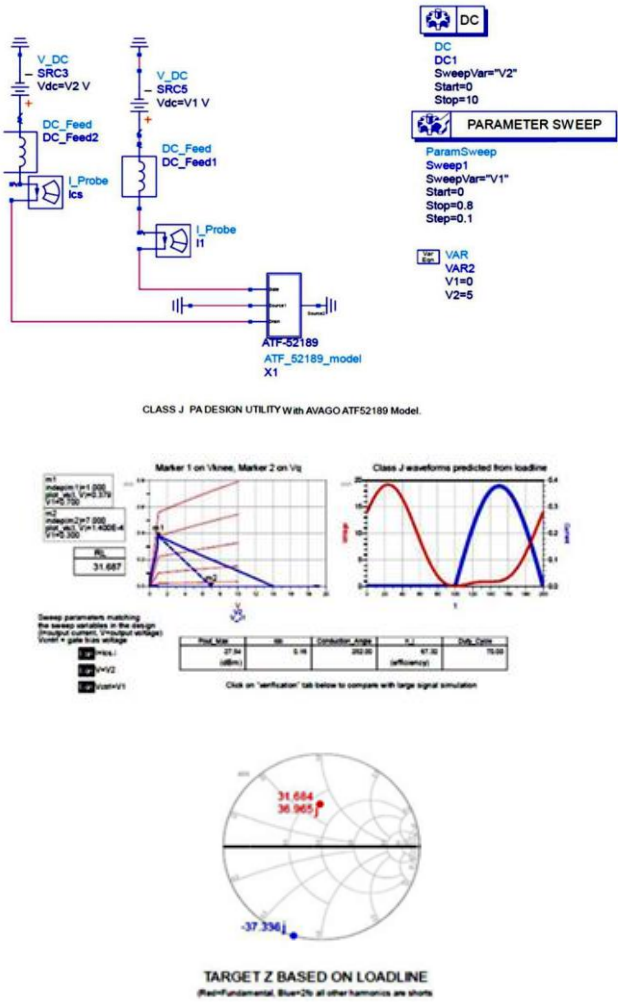



**Figure 5. DCIV characteristics schematic capture and class J prediction**

## 2.4 Parasitic tune

The impedances obtained from the load line are required at the device intrinsic node, therefore, we expect different load terminations at the extrinsic (package) node. For this reason, a parasitic tune was carried out as shown in Figure 6. Here, an equation based ideal load was presented at the output and a low power source was connected to the input of the biased device. Using harmonic balance simulation, we swept the ideal load over reasonable impedance values. The resultant intrinsic impedance was calculated from voltage and current measured at the intrinsic node.

By data display methods, the appropriate external loads for the target internal fundamental, second and third harmonic impedances were found.

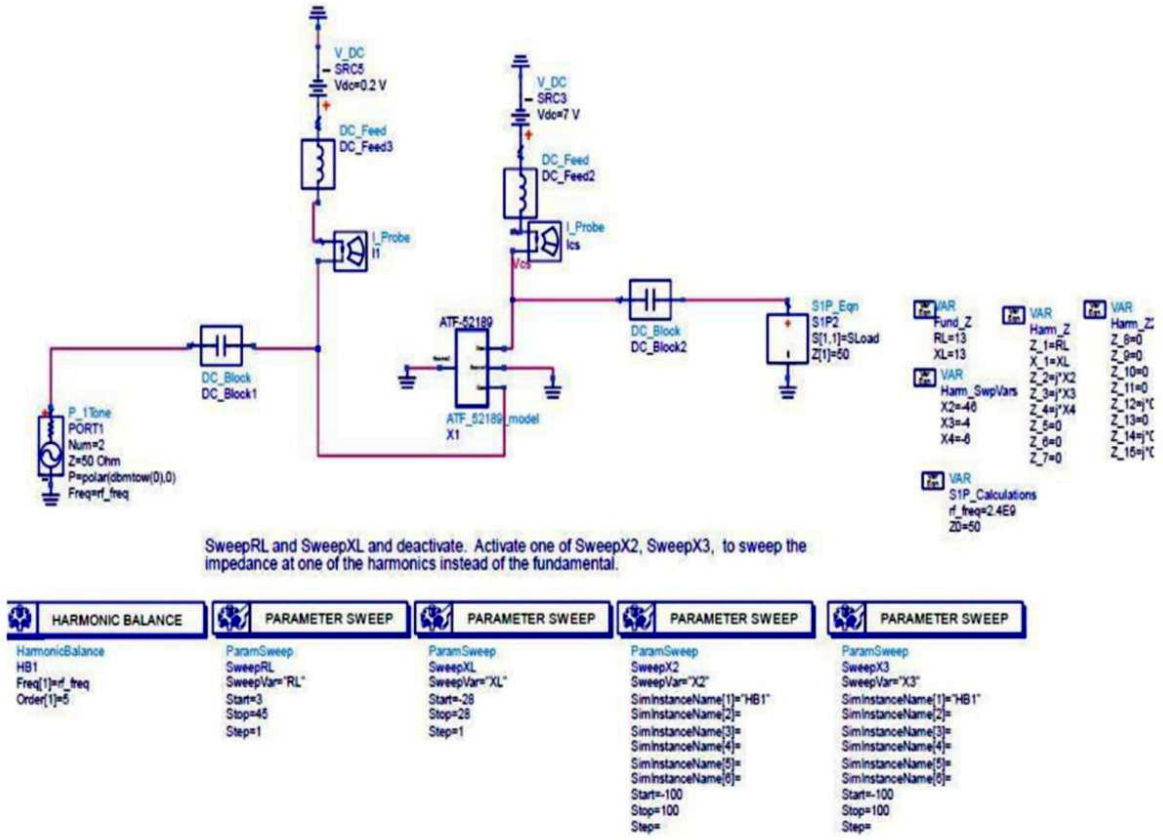



**Figure 6. Parasitic tune schematic and the swept parameters**

To improve the tune, the input was conjugate matched to a 50 ohm source and the input power was adjusted so that the drain current swung over the whole dc load-line.

Figure 7, Figure 8 and Figure 9 illustrate the data display for the swept impedances at fundamental, 2nd and 3rd harmonics.

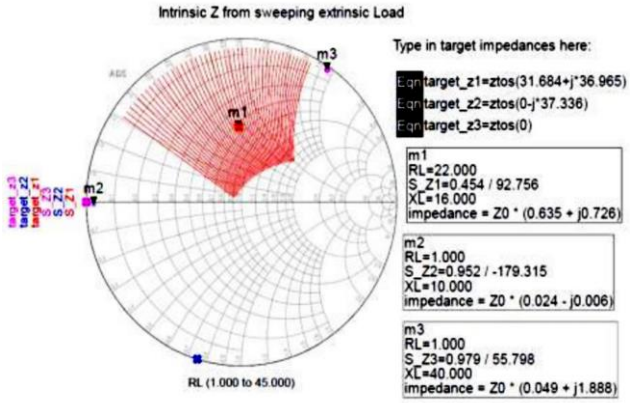



**Figure 7. Fundamental load tuning**

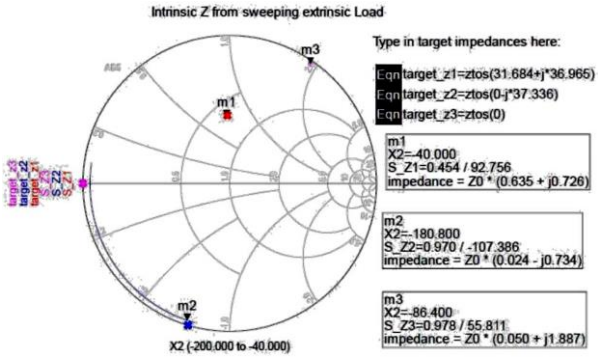



**Figure 8. 2nd harmonic tune**

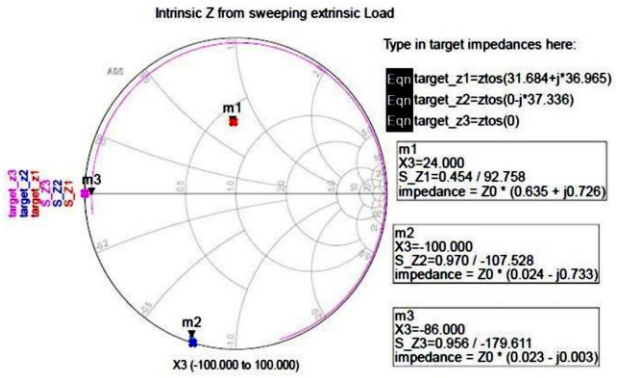



**Figure 9. 3rd harmonic tune**

The circuit schematic in Figure 10 was used to determine the input impedance so that a conjugate matching network can be designed between the device and the driver

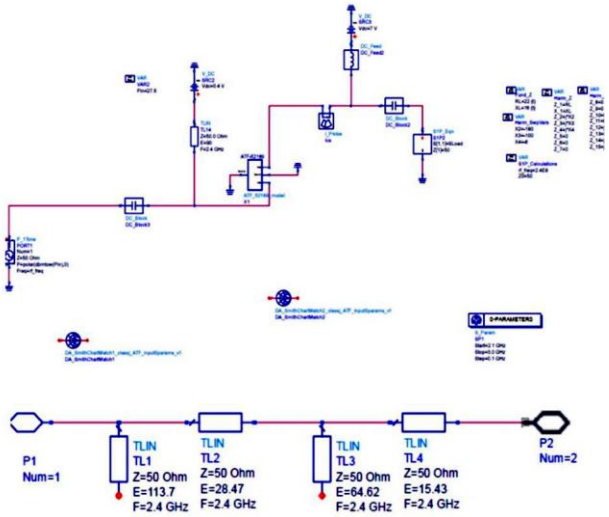



**Figure 10. Input impedance measurement and matching schematic**

## 2.5 Output network optimization

The external load obtained in the parasitic tune was approximated by the distributed element network illustrated in Figure 11.

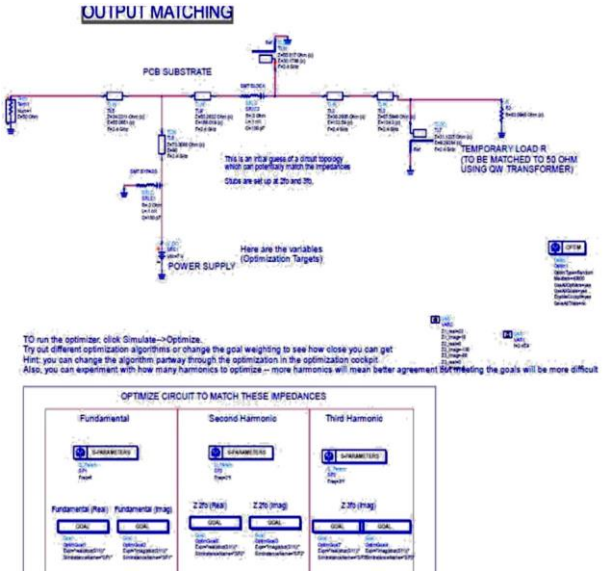



**Figure 11. Output impedance optimization schematic**

By defining the desired harmonic characteristics of the network as goals, the ADS optimization engine was used to fine tune each element within realizable ranges so as to closely match the desired impedances. Figure 12 captures the optimization cockpit as it runs through 40 000 iterations.

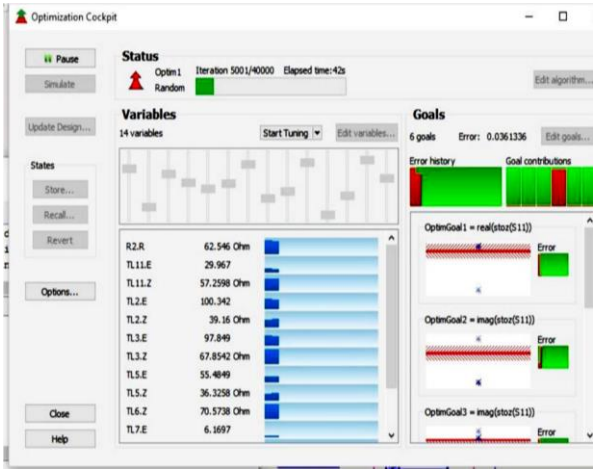



**Figure 12. Optimization in progress**

## 2.6 Complete design simulation

The complete schematic design shown in Figure 13 was simulated in order to compare its performance and waveforms with the load line prediction.

## 2.7 Layout design

The schematic design was converted into an FR4 substrate based layout design in readiness for fabrication. It was assumed that since the design was a simple single layer layout, EM simulation was not necessary. Figure 14 illustrates the layout design.

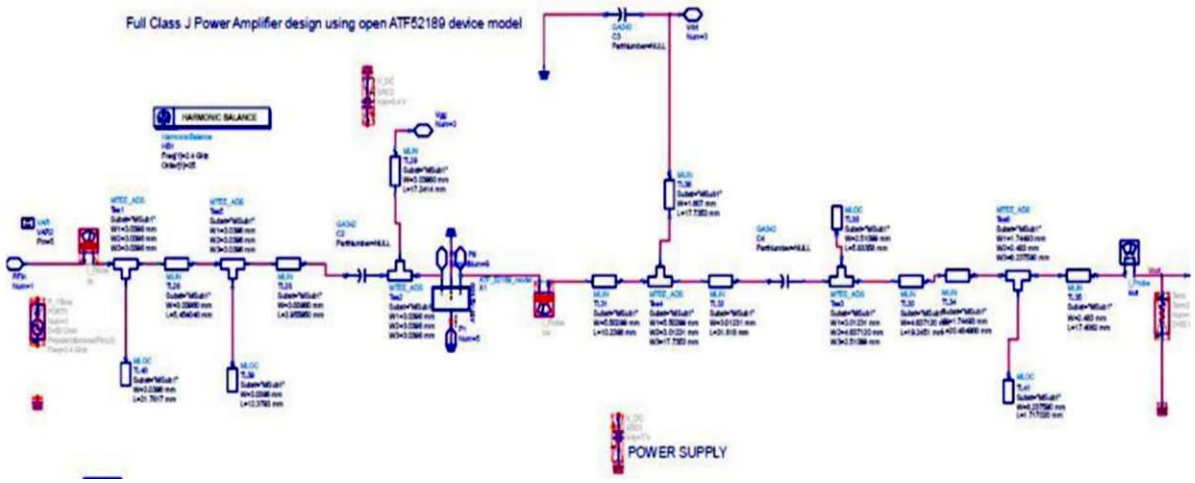



**Figure 13. Complete schematic design**

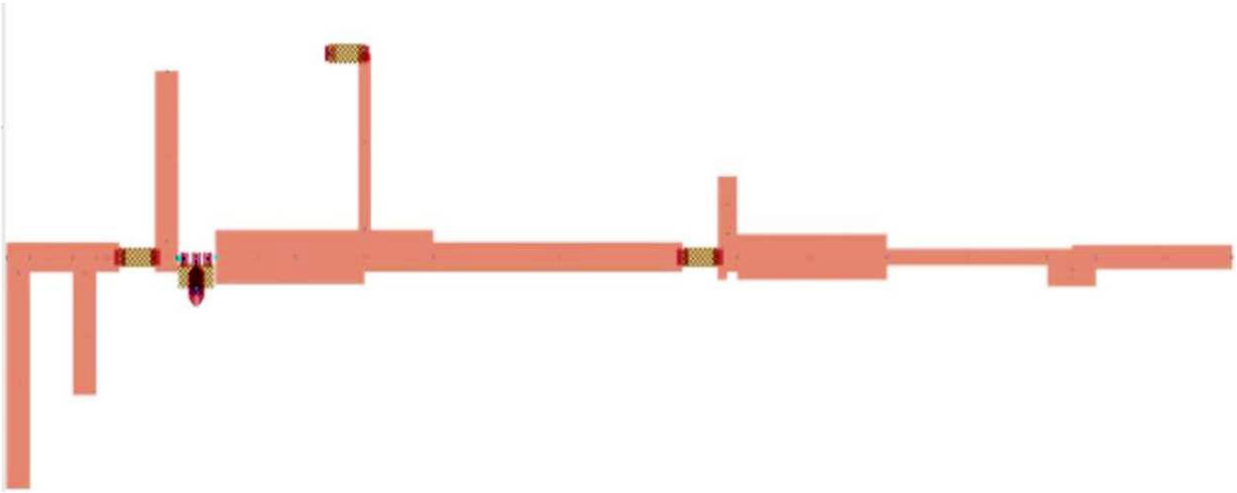


**Figure 14. 2.4 GHz layout design**

## 3. SIMULATION RESULTS

The simulation results are shown in Figure 15(a) and Figure 15(b). The power output and drain efficiency almost matching the predicted values from the dc load-line.

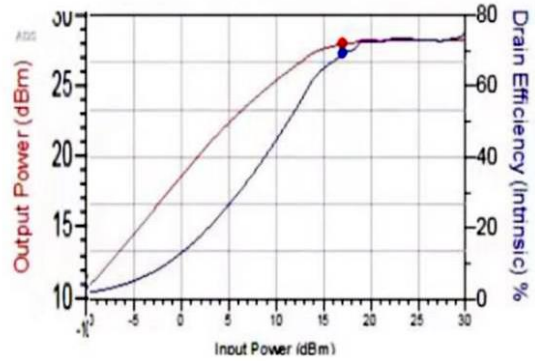
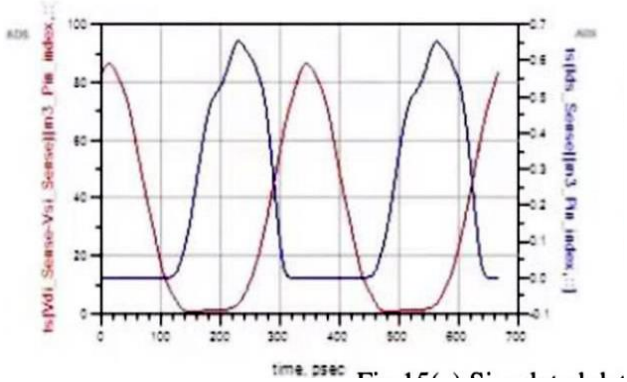



**Figure 15.a. Simulated data display**



## 4. CONCLUSION

The simulated 2.4 GHz PA closely achieved the predicted class-J waveforms, power output and efficiency performance. The slight discrepancy observed was attributed to the device parasitic other than the output capacitance which was absorbed in the design. The output power designed for, 20dBm, was slightly surpassed to yield a 21dBm output. The simulation results show that the PA exhibited a drain efficiency of 69% and a power output of 21dBm with low distortion.

## 5. REFERENCES

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