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A METHOD OF REDUCING SWITCHING LOSSES IN THREE-LEVEL NPC INVERTER*

RYSZARD BENIAK, KRZYSZTOF ROGOWSKI

Opole University of Technology, Faculty of Electrical Engineering,
Automatic Control and Informatics, ul. Prószkowska 76, 45-758 Opole, Poland,
e-mail: r.beniak@po.opole.pl, krzysztof.rogowski@doktorant.po.edu.pl

Abstract: The aim of the paper is to present a concept of implementation of a space vector modulation (SVM) algorithm, which is used to create alternating current waveforms of changing amplitude and frequency in power inverters. The main goal of the method is to decrease the number of state changes in power transistors. It is realized by utilizing a prediction algorithm and sequences of transistors, which are not common in use. The method requires measurement of inverter output current flow. The prediction algorithm analyzes possible sequences of transistors' states and choose those which offers smaller switch count. A decrease of about 20% was obtained for the cases tested. This paper presents simulation result for selected driving scenario. The described method decreases the number of state changes in power transistors and therefore it is a potentially good method to considerably decrease energy losses of multilevel inverter-powered drive.

Keywords: *reduction of switching losses, three level NPC inverter, space vector modulation*

1. INTRODUCTION

The Neutral-Point-Clamped PWM Inverter was originally developed by Nabae, Takahashi and Akagi in 1981 [1]. Main advantages of this configuration are better efficiency, less harmonic distortion due to more voltage levels and half of voltage rating of switching devices requirement (excluding second type 3L-NPC inverter presented in [1]) [1]–[3]. This is because switching losses in IGBT transistors are approximately proportional to the switching voltage and current. Lower voltage changes between levels put lower stress on the motor wiring. Additionally, lower voltage transistors may work faster [4]. Inverter of this type offers easy control of reactive power [5]. Test shows that a three-level inverter with switching frequency set at 2.5 kHz has higher efficiency compared with a two-level inverter set at 1 kHz. Higher switching frequency and increased voltage levels have positive impact on inverter output harmonic performance [4]. The main disadvantages of NPC configuration are more com-

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plex topology with higher number of power switches compared with two-level inverter, excessive number of clamping diodes (especially if the number of levels is high) and difficulty to do real power flow control for the individual inverter [5].

Space Vector Modulation (SVPWM) was originally developed by Van der Broeck et al. in 1988 [6] as a better alternative for sinusoidal pulse-width modulation (SPWM). The main advantages of this modulation are lower current harmonics and possible higher modulation index in comparison to SPWM [6]. The main disadvantages of SVPWM are complex calculations requiring more computing power. This issue is addressed in [7], [8] by simplification of sector identification and elimination of trigonometric operations in dwell time calculation.

There are many implementations of SVM, mainly differentiated by reference vector plane division utilized in generation of pulses. The most popular for three-level inverter are SVPWM-3H, SVPWM-4R and transposition of reference vector coordinates to equivalent two-level hexagon [7], [9], [10].

SVPWM-3H divides reference vector plane into three hexagons. The inner hexagon consists of small vectors, middle hexagon consists of medium vectors, and outer hexagon consists of large vectors. Each hexagon is divided into six sectors and each sector is limited by any two adjacent vectors. This gives 18 sectors [9].

SVPWM-4R divides reference vector plane into six sectors, each of 60 degrees, limited by two adjacent large vectors. Each sector is divided into four regions [9].

Transposition method divides reference vector plane into one inner and six outer two-level equivalent hexagons [10]. Pulse time is calculated in the analogous way as they are in two level inverter [11]. This method is used in this paper.

Finding ways to make switch count as low as possible is necessary to avoid switching losses. In the conventional approach there are methods to lessen the switch count (number of transistor state changes). This can be achieved by alteration to inverter topology, using smaller number of voltage vectors in sampling time, or simply by lessen sampling frequency. For example, one is to change the three-level inverter topology in such a way that it consists of about 25% smaller number of transistors, as presented in [12]. Downside of that method is the need for six independent power supplies. The other method achieves smaller switching losses by using smaller number of voltage vectors in sampling time, but gives slightly decreased quality of output current and requires use of additional measures to ensure proper neutral point balancing [13].

This paper presents a new approach in which additional transistor sequences are used in synthesizing 19 voltage vectors of the three-level NPC inverter (Fig. 1) [14], [15]. Those additional states make use of the inverter clamping diodes. A prediction algorithm is used to make full use of those additional sequences in order to lessen the switch count.

Space Vector Modulation method used in this paper is described in Section 2. The computational implementation and prediction algorithm is presented in Section 3. Section 4 is the conclusion.

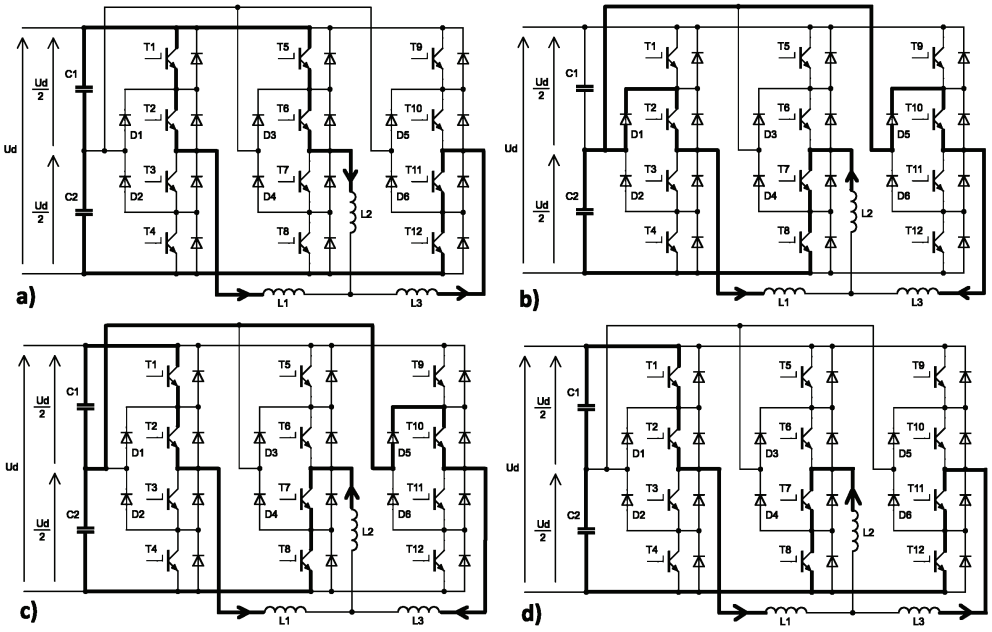

Fig. 1. Examples of three-level inverter active states:
(a) standard state – current flows only through transistors, (b) additional state – current flows through transistors and diodes D1 and D5, (c) additional state – current flows through transistors and diode D5, (d) standard state – current flows only through transistors

2. SPACE VECTOR MODULATION

To realize the SVM algorithm, changing voltages between phases are converted into a vector rotating in a complex plane which represents a rotating magnetic field. A three-level inverter has nineteen possible combinations of voltage values between phases (u_{AB}, $u_{BC,}$, u_{CA}). Those values are converted into phase voltages (u_A, $u_{B,}$, u_C). Then they are converted into Cartesian and polar coordinates in α-β plane – k_α, k_β; θ, ρ with (1), (2) respectively. This gives nineteen possible switching vectors forming a regular hexagon.

$$k_\alpha = u_A, \quad k_\beta = \frac{u_B - u_C}{\sqrt{3}}, \tag{1}$$

$$\theta = \sqrt{k_\alpha^2 + k_\beta^2}, \quad \rho = \operatorname{atan2}(k_\alpha, k_\beta). \tag{2}$$

Assuming that sampling time T_C is constant and sufficiently small, a rotating vector U_0 is considered constant in that time. In a two-level inverter, the U_0 vector can be

synthesized as a weighted average combination of the two adjacent switching vectors $U_{w1} \div U_{w6}$ and a null vector U_{w0} (Fig. 2).

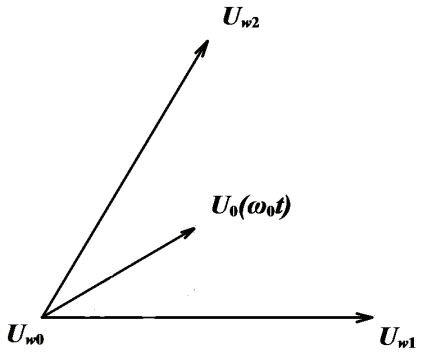

Fig. 2. Rotating vector U_0 synthesized as a switched combination of three adjacent vectors U_{w0}, U_{w1}, U_{w2}

The switching time (t_0, t_1, t_2) of each vector is calculated from $i = 1 \div 6$ according to formulas (3), (4). If $i + 1 = 7$ then we assume that $i = 1$.

$$\frac{T_C}{2} U_0(\omega_0 t) = t_1 U_{wi} + t_2 U_{wi+1}, \tag{3}$$

$$t_0 = T_C - t_1 - t_2. \tag{4}$$

A method of coordinate transposition was used for a three-level inverter (Fig. 3) [10]. This method allows for use of the same calculation of switching times as in two level inverter. For depth of modulation $m \leq 0.5$ the switching times are calculated from U_0 coordinates without change. For $m > 0.5$, depending on angle θ, coordinates U_0 are transposed to one of six smaller hexagons, which are treated locally in the analogous way as they are in two-level inverter.

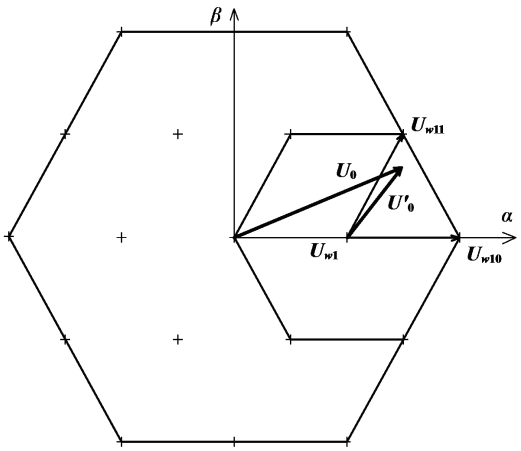

Fig. 3. Transposition of U_0 coordinates from the main hexagon to U'_0 coordinates in a local two-level hexagon

Calculated times (t_0, t_1, t_2) are used to modulate switching vectors in sequence: $t_0/4$; $t_1/2$; $t_2/2$; $t_0/2$; $t_2/2$; $t_1/2$; $t_0/4$ or $t_0/4$; $t_2/2$; $t_1/2$; $t_0/2$; $t_1/2$; $t_2/2$; $t_0/4$; t_0 for zero vectors, and t_1, t_2 for non zero vectors. Time calculation in (3), (4) does not include the time needed for transistors to change their state.

3. IMPLEMENTATION

The nineteen possible switching vectors, with one being zero, can be obtained by using from one to four different combinations of twelve transistor states per switching vector. For example, a zero vector U_{w0} has three possible sets of transistor states ($T_1 \div T_{12}$) 110011001100, 011001100110, 001100110011, where 0 denotes OFF, and 1 denotes ON state. In order to minimize switch count, a prediction algorithm is used in which two steps ahead are calculated.

The look-up tables are used in the algorithm. The first consists of nineteen rows of possible sets of transistor states, which correspond to all nineteen switching vectors. The prediction algorithm extracts its data from this table. Next, the set of transistor states considered is compared with previous one by XOR logical operation (Fig. 4). An example of one whole sequence is presented in Table 1. The second table consists of sequences of six switching vectors which correspond to six sectors of a two-level hexagon. There are six other tables, analogous to the second one, in which sequences of switching vectors are transposed in respect to local two-level hexagon (Fig. 5).

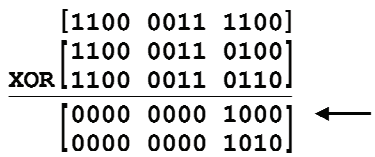

Fig. 4. Calculation of the most optimal set of transistors for the next step. In this example, the most optimal set after 110000111100 is 110000110100, because only one transistor changes its state

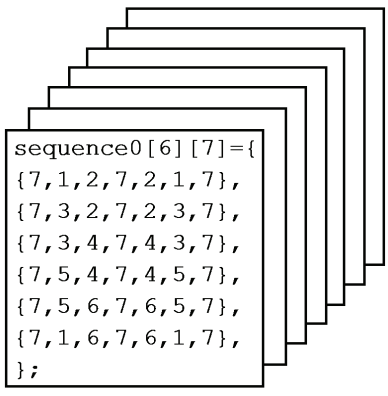

Fig. 5. Second look-up table – in front: vector switching sequences for six sectors of inner hexagon. The table has six rows for six sectors. Each row contains a sequence of switching vectors used in time T_C to synthesize vector U_0. There are six more analogous tables with transposed sequences. Number 7 denotes zero voltage vector, numbers 1–6 are active voltage vectors of inner hexagon

Table 1. Example of one sequence before and after optimization

after – 10 state changes	before – 12 state changes
001101000011	001101100011
001111000011	001111000011
011011000011	011011000011
011011000110	011011000110
011011000011	011011000011
001111000011	001111000011
001101000011	001101100011

The rotating vector control algorithm is used to calculate coordinates U_0 according to given parameters of power inverter in a sample of time. A simplified flowchart of the main algorithm is presented in Fig. 6.

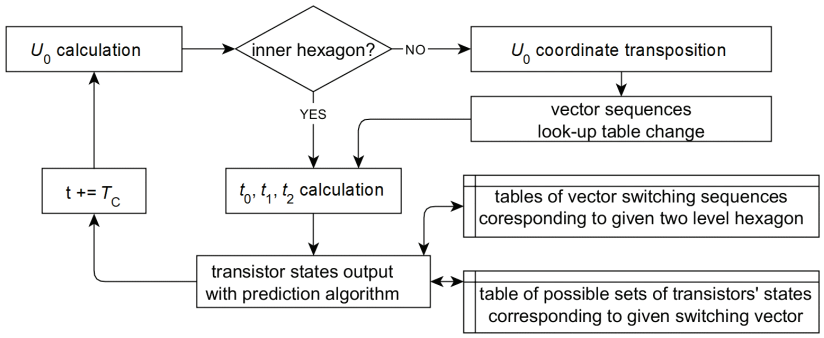

Fig. 6. Simplified flowchart of the main algorithm

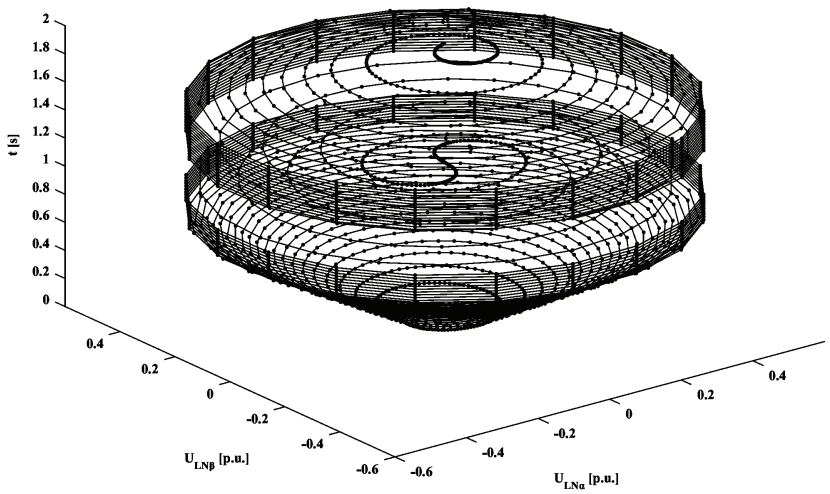

Fig. 7. Coordinates marked by rotating vector in complex space

An example chart of rotating vector coordinates is shown in Fig. 7. Coordinates are calculated for 0.8 s start up, 0.2 s steady state, 0.3 s to full reverse, 0.3 s steady state, 0.4 s to full stop (f_{start} = 5 Hz, f_{max} = 50 Hz, T_C = 1 ms, t = 2 s), as shown in Fig. 8. In this example, the number of individual transistor state changes drops from 43064 to 23777 for two-step prediction, without noticeable change in output waveform in analyzed drive (Fig. 9). Switching transistor dead time was taken into consideration in these calculations by ensuring that no transistor state will change for less than 5 µs. In Fig. 7, the maximum line-to-line voltage U_{Dcref} = 563 V [11].

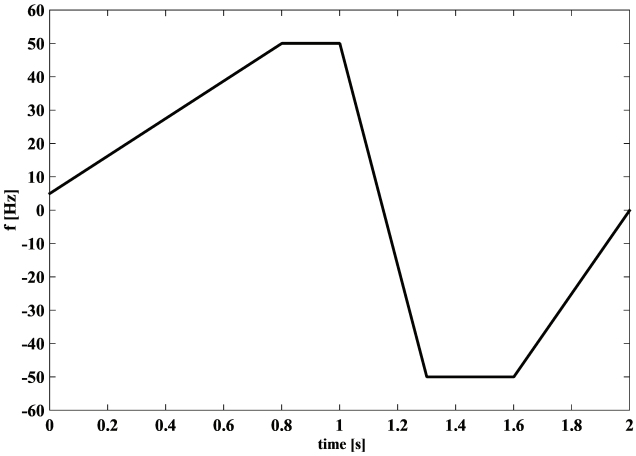

Fig. 8. Requested output frequency of the inverter

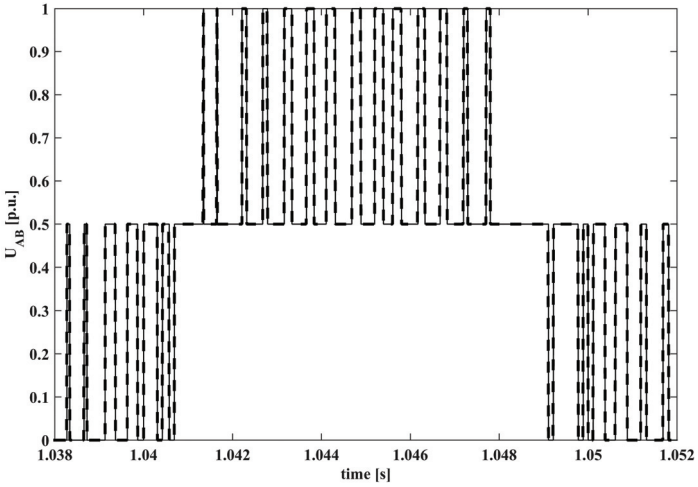

Fig. 9. Example of output waveform of the inverter (U_{AB}) before – solid line, and after use of prediction algorithm – dashed line

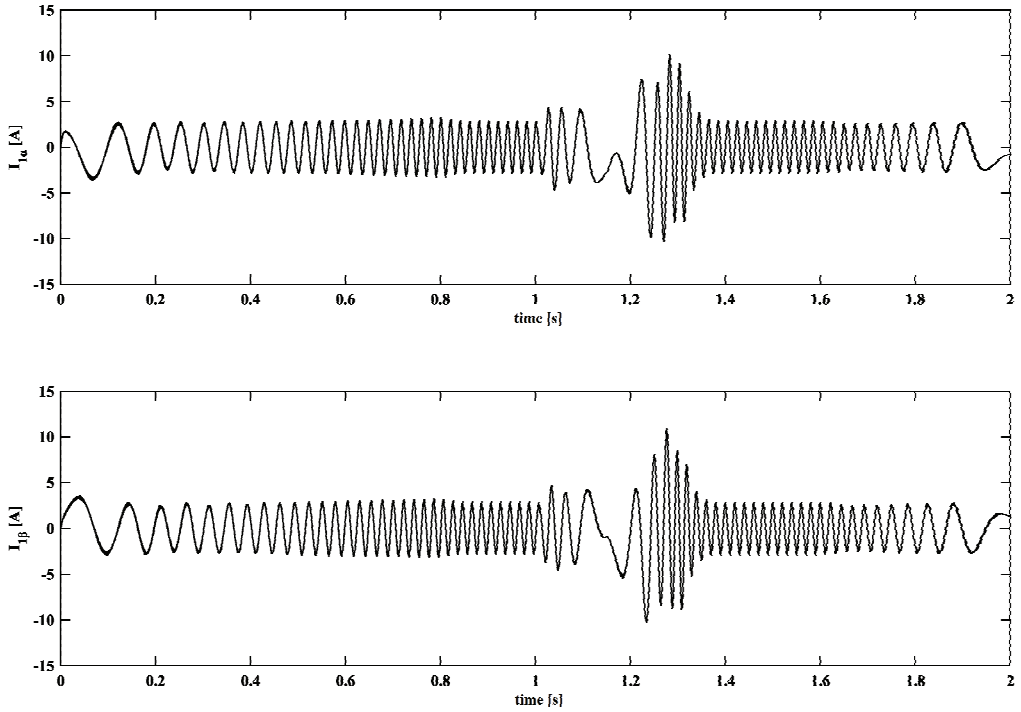

Fig. 10. The α and β components of the stator phase current

4. CONCLUSIONS

Thanks to additional sets of transistor states, corresponding to voltage vectors, and the use of prediction algorithm, it is possible to lessen the transistors switch count considerably. As shown in the simulation presented, the number of individual transistor state changes drops from about 43064 (without prediction) to 23777 for two-step prediction. Prediction of more than two steps ahead did not gave considerable improvement. A decrease of about 20% was obtained for most of the cases tested. In general, the rate of decrease changes from a few percent for about half of modulation depth value to about 20% for full modulation depth. It is important to mention that implementation of the method presented requires measuring of inverter output current flow.

It is necessary to find the ways to make switch count as low as possible in order to avoid switching losses and therefore improve energy efficiency of a power inverter.

REFERENCES

[1] NABAE A., TAKAHASHI I., HIROFUMI A., *A New Neutral-Point-Clamped PWM Inverter*, IEEE Transactions on Industry Applications, September/October 1981, IA-17, 5.

[2] RODRÍGUEZ J., LAI J.S., PENG F.Z.: *Multilevel Inverters: A Survey of Topologies, Controls, and Applications*, IEEE Transactions on Industry Electronics, August 2002, 49, 4.

[3] KOURO S., MALINOWSKI M., GOPAKUMAR K., POU J., FRANQUELO L.G., WU B., RODRÍGUEZ J., PÉREZ M.A., LEON J.I., *Recent Advances and Industrial Applications of Multilevel Converters*, IEEE Transactions on Industry Electronics, August 2010, 57, 8.

[4] ORFANOUDAKIS G.I., SHARKH S.M., YURATICH M.A., ABUSARA M.A., *Loss Comparison of Two and Three-level Inverter Topologies*, 5th IET International Conference on Systems Power Electronics, Machines and Drives (PEMD), 2010.

[5] LAI J.S., PENG F.Z., *Multilevel Converters – A New Breed of Power Converters*, IEEE Transactions on Industry Applications, May/Jun 1996, 32, 3.

[6] VAN DER BROECK H.W., SKUDELNY H.-C., STANKE G.V., *Analysis and Realization of a Pulsewidth Modulator Based on Voltage – Space Vectors*, IEEE Trans. on Industry Applications, January/February 1988, 24, 1, 142–150.

[7] GOUTHAM KUMAR REDDY G., SRIDHAR S., *Three Level Modified SVPWM Inverter Fed DTC Induction Motor Drive*, International Research Journal of Engineering and Technology (IRJET), Sep. 2015, 2, 6.

[8] DE PABLO S., REY A.B., HERRERO L.C., RUIZ J.M., *A simpler and faster method for SVM implementation*, European Conference on Power Electronics and Applications, 2007.

[9] URMILA B., SUBBA RAYUDU D., *Optimum Space Vector PWM Algorithm for Three-level Inverter*, ARPN Journal of Engineering and Applied Sciences, September 2011, 6, 9.

[10] ZYGMANOWSKI M., GRZESIK B., *Space Vector Modulation for 3-level neutral-point clamped inverter using DSP TMS 320F2812*, Zeszyty Naukowe. Elektryka, Politechnika Śląska, 2006, 198, 155–166, (in Polish).

[11] SOBAŃSKI P., ORŁOWSKA-KOWALSKA T., *Analysis of Space Vector Modulation Technique in Inverter-Fed Fault-Tolerant Induction Motor Drive*, 16th International Power Electronics and Motion Control Conference and Exposition, Antalya, Turkey, 21–24 Sept., 2014.

[12] SALEM A., AHMED E.M., AHMED M., ORABI M., ABDELGHANI A.B., *Reduced Switches Based Three-Phase Multi-Level Inverter for Grid Integration*, 6th International Renewable Energy Congress (IREC), 2015.

[13] KOŁOMYJSKI W., MALINOWSKI M., KAŹMIERKOWSKI M.P., *Adaptive Space Vector Modulator for Three-Level NPC PWM Inverter-Fed Induction Motor*, 9th IEEE International Workshop on Advanced Motion Control, 2006.

[14] PATRZEK P., *Control of Multilevel NPC Inverter with consideration of minimization of converter part losses*, Master thesis, Opole University of Technology, 2012, (in Polish).

[15] OBALEK K., *Control of Multilevel NPC Inverter with consideration of optimizing equations*, Master thesis, Opole University of Technology, 2012, (in Polish).