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THE DESCRIPTION OF TURN-OFF PROCESS AND EVALUATION OF SWITCHING POWER LOSSES IN THE ULTRA FAST POWER MOSFET*

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Abstract: The article presents an analytical description of the turn-off process of the power MOSFET suitable for use in high-frequency converters. The purpose of this description is to explain the dynamic phenomena occurring inside the transistor and contributing to the switching power losses. The detailed description uses the results of simulation studies carried out using a very precise model of the CoolMOS transistor manufactured by Infineon (IPW60R070C6). The theoretical analysis has been verified in experimental measurements of power dissipated during turn-off transient of MOSFET operating in a full bridge converter with switching frequency of 100 kHz. To estimate these switching losses an original thermovision method based on the measurement of heat dissipated in the power semiconductor switches has been used. The obtained results confirm the correctness of the conclusions drawn from the theoretical analysis presented in this paper.

Keywords: *Power MOSFET, turn-off transient, parasitic capacitance, switching losses, thermovision measurements*

1. INTRODUCTION

In the case of power converters operating at high switching frequency, the significant component of the total power losses are switching losses occurring in the transistors [1]. One way of limiting the power losses dissipated in dynamic states of transistors is to shorten the turn-on and turn-off durations by reducing the resistance of the gate circuit [2]. In the commercially available fast gate drivers designed for new-generation high-frequency power MOSFETs it is possible to use an additional resistor with low resistance or to control even without such a resistor [3], [4]. Due to this, switching processes are achieved, the description of which differs from that commonly

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used for switches of this type [5]. The classic definition of dynamic states of the MOSFET may lead to an erroneous interpretation of the results of measurements of switching energy losses E_{off} based on the drain-source voltage v_{ds} and drain current i_d waveforms during a transistor turn-off (Fig. 1) [2].

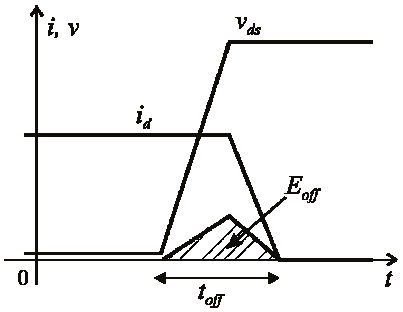


Fig. 1. Commonly used voltage and current waveforms in order to determine the loss of energy during MOSFET turn-off transient

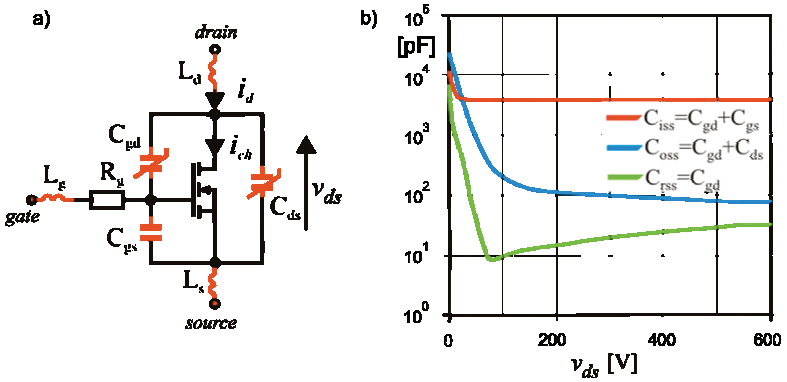


Fig. 2. Equivalent circuit of the MOSFET useful for the analysis of the dynamic states (a) and the parasitic capacitances of an IPW60R070C6 transistor as functions of the voltage (b) (C_{gs}, C_{gd}, $C_{ds.}$ – transistor capacitances, L_g, L_d, L_s – lead (inner wires) inductances, R_g – gate circuit resistance)

The article provides a detailed analytical description of the turn-off process in a high-voltage power MOSFET, characterized by a large and strongly nonlinear junction capacity. With the use of a gate circuit with a very low resistance and considering the internal parasitic parameters (junction capacitance and lead inductance) of the switch (Fig. 2), the phenomena occurring during switching process inside the semiconductor structure are crucial to correctly determine the value of the energy dissipated in the transistor. A full explanation of these phenomena is quite difficult because of the limited

experimental measurements inside the transistor; therefore, for example, simulation studies using advanced programs for modelling switching transients can be of assistance.

In explaining the switching phenomena considered in this paper, the results of dynamic process simulations performed in the PSpice were used. In these studies, a precise IPW60R070C6 transistor model (600 V, 70 mΩ, 52 A) [6] was used, which had been previously verified in laboratory tests for the correctness of operation under static and dynamic conditions, including the consistence of the $C_{oss} = f(v_{ds})$ characteristics and the dependence of the parameters on temperature [7].

2. TURN-OFF TRANSIENT WITH A NEGLIGIBLE RESISTANCE IN THE GATE CIRCUIT

The essence of the problem of the fast MOSFET turn-off transient, discussed in this paper, is illustrated by the voltage and current waveforms obtained in the simulation model (Fig. 3). The differences visible in the waveforms result from using a very low gate resistance R_g in one driver (Fig. 3a), compared to the conventional driver that can be found in low and medium switching frequency converters.

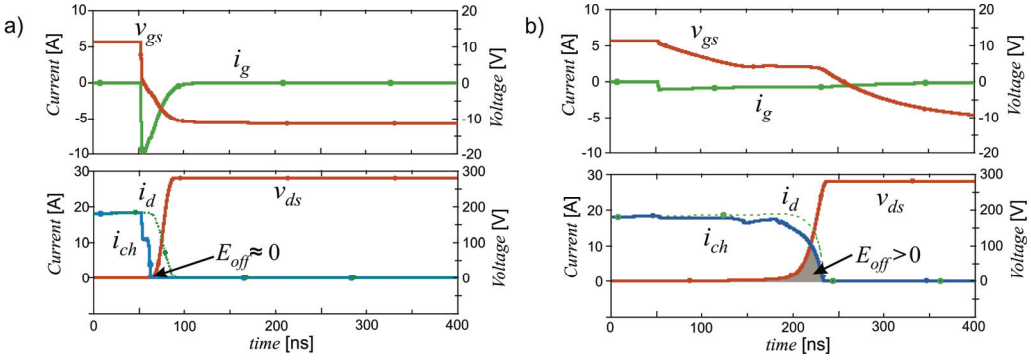


Fig. 3. Waveforms of gate voltage v_{gs} and current i_g, drain to source voltage v_{ds}, drain current i_d, and internal current i_{ch}, flowing through the MOSFET channel for two different resistances in gate circuit (with no inductance effect): a) $R_{g,off} = 0{,}5\ \Omega$; b) $R_{g,off} = 20\ \Omega$; ($L_s = 0$, $I_{d,off} = 20$ A, $V_{dc} = 280$ V)

Discharging of transistor input capacitance, C_{iss}, in the case of negligibly low resistance of the gate circuit is very quick. Therefore, it is difficult to distinguish the switching off stages, which is characteristic of the conventional description. Particularly noticeable is the lack of the Miller effect in the gate voltage waveform, which is associated with the discharge of the nonlinear Miller capacitance C_{gd}. This means that the current flowing through the channel decreases very rapidly, by contrast to the voltage v_{ds} increase process, which is dependent on the C_{oss} output capacitance charging

level. As for low values of drain-source voltage this capacitance is very large (Fig. 2b), at the initial turn-off stage the instantaneous value of voltage v_{ds} increases very slowly. Hence, it can be assumed that turn-off process of the MOSFET with $R_g = 0$ has the features of soft switching and occurs lossless at zero voltage (ZVS). If, similarly as in Fig. 3a, the effect of the parasitic lead inductances is neglected, then, assuming a very low resistance R_g, the turn-off power loss will always be close to zero, regardless of the magnitude of current being turned off.

3. DETAILED ANALYSIS OF THE TURN-OFF TRANSIENT

A detailed analysis was carried out taking into account the parasitic lead inductances in the equivalent circuit diagram (Fig. 2a), which have an influence on the rate of current changes during the commutation process. The most important of them, from the point of view of the main and the control circuit, is the MOSFET source lead inductance L_s [8], which has a direct effect on the drain current time derivative. The voltage induced on L_s forms a feedback signal from main circuit to the control circuit. The remaining parasitic inductances of the transistor have also effect on the commutation process although their influence is only indirect. For example, the inductance of the gate connection L_g slows down the control dynamics, similarly as the R_g resistance does. In the further analysis also the inductance of source lead L_s is considered.

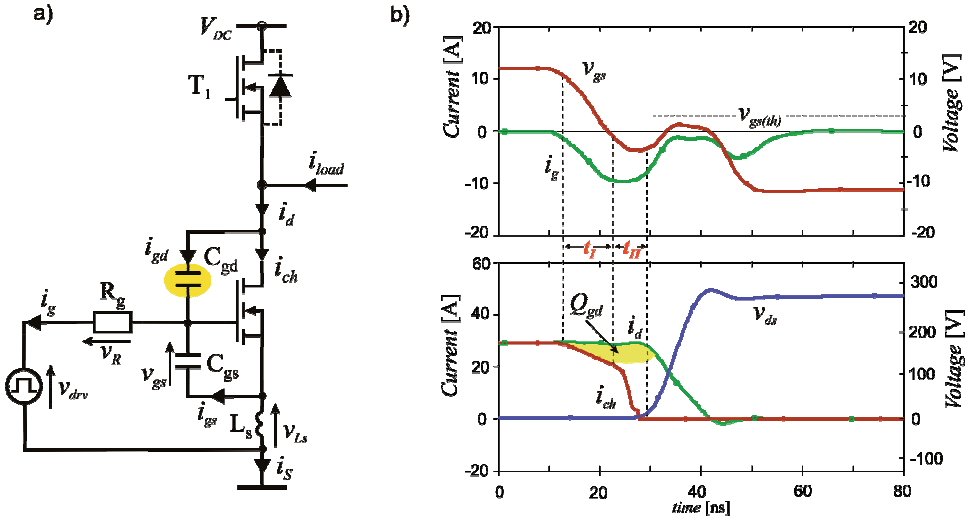


Fig. 4. The equivalent scheme of the leg with two MOSFETs in relation to initial time interval of turn-off process (a) and the characteristic waveforms (b)

3.1. TIME INTERVAL t_I

The MOSFET gate circuit (Fig. 4a) in the first stage of turn-off process (the time interval t_I in Fig. 4b) can be described by the following relation

$$v_{drv} = i_g R_g + v_{Ls} + v_{gs} \tag{1}$$

where v_{drv} – gate driver voltage ($v_{drv(0)} = V_{drv}$); v_{gs} – gate-source voltage ($v_{gs(0)} = V_{drv}$); v_{ds} – drain-source voltage ($v_{ds(0)} = 0$).

Since the gate current i_g for $t = 0$ is equal to zero, therefore the voltages on the resistance (v_R) and on the inductance (v_{Ls}) in the circuits are initially equal to zero ($v_{gs} = v_{drv}$).

The transistor turn-off process starts at the moment when the gate driver voltage changes its polarization from positive to negative. At a very low resistance R_g, a rapid increase in gate current i_g occurs, which causes the input capacitance C_{iss} to discharge quick. The formula describing the current i_g has the following form

$$i_g = C_{iss} \frac{dv_{gs}}{dt} = (C_{gs} + C_{gd}) \frac{dv_{gs}}{dt}. \tag{2}$$

In the time interval t_I, the drain current, whose magnitude is forced by an external main circuit, has a constant value of $i_d = i_{\text{load}} = \text{const}$. On account of the low resistance value R_g and the large initial value of capacitance C_{gd} (Fig. 2b), the value of current i_{gd} has decisive effect on the split of the current i_d inside the transistor according to the relation (Fig. 4)

$$i_d = i_{ch} + i_{gd} \tag{3}$$

where i_{ch} – channel current of the MOSFET.

This means that in the time interval t_I the current flowing through the MOSFET channel is smaller than the drain current. If the initial value of the drain current is comparable to or smaller than the peak value of i_{gd}, the vanish of current channel may even occur.

Except the current i_{gd}, the capacitance C_{gs} discharge current i_{gs} also flows. Hence, the following relation can be written

$$i_s = i_{ch} - i_{gs} \tag{4}$$

where i_s – source current of the MOSFET.

If the parasitic inductance L_s of the source lead (Fig. 4) is additionally considered, then, in spite of constant i_d, under the influence of current i_{gs} variations, the voltage v_{Ls} will be induced

$$v_{Ls} = -L_s \frac{di_{gs}}{dt}. \tag{5}$$

According to equation (1), the voltage v_{Ls} counteracts the changes in voltage v_{drv}, thus slowing down the channel turn-off process.

3.2. TIME INTERVAL t_{II}

In the second stage of the turn-off process (time interval t_{II} in Fig. 4b), a further decrease in the voltage v_{gs} takes place. This means the transition of the MOSFET to the region of linear control characteristics, where the channel current is described by the relationship

$$i_{ch} = g(v_{gs} - v_{gs(th)}) \tag{6}$$

where g – MOSFET's transconductance, $v_{gs(th)}$ – threshold voltage of the MOSFET.

According to this relationship, the channel current in time interval t_{II} starts rapidly decreasing, which, at the constant drain current value, causes the flow of current associated with the charge of the drain-source junction beyond the transistor channel, giving rise to the process of charging of non-linear capacitance C_{ds} (Fig. 5a). As also the i_{gd} current continues to flow, the internal current spread within the transistor is described by the formula

$$i_d = i_{ch} + i_{gd} + i_{ds} \,. \tag{7}$$

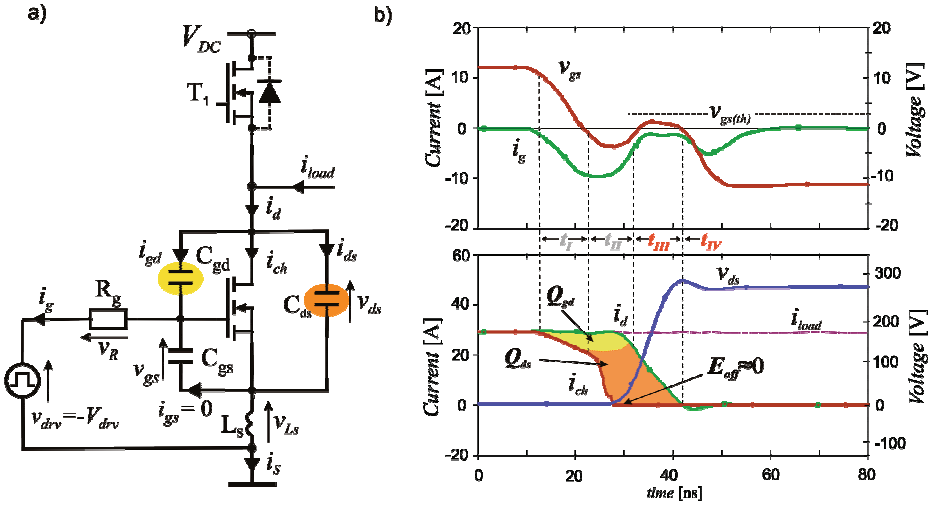


Fig. 5. The illustration of the MOSFET soft turn-off transient, allowing for the parasitic lead inductance: (a) the equivalent circuit diagram, (b) the characteristic MOSFET voltage and current waveforms

The inflow of the charge to the source-drain junction capacitance causes a gradual increase in voltage v_{ds} which, due to the strongly nonlinear behaviour of this capaci-

tance as a function of voltage, initially increases very slowly. Therefore, with the very rapid discharge of capacitance C_{gd} by the negligible-resistance circuit, the channel current decrease duration is much shorter than the duration of the C_{ds} capacitance charging process. As a result, the MOSFET channel is turned off when the v_{ds} voltage has still a very low value, so the turn-off energy losses are in this case very low (Fig. 5b).

3.3. TIME INTERVAL t_{III}

The third stage of the turn-off process (the time interval t_{III} in Fig. 5) is also associated with the existence of the parasitic connection inductance L_s of the power MOSFET. Depending on the magnitude of switch-off current $I_{d,off}$, and hence on its time derivative, this inductance may cause a change in the behaviour of the soft turn-off process under examination, and thus an increase in the energy loss level. From the moment the external current i_d starts decreasing with the time derivative $di_d/dt \approx di_s/dt$, the inductance L_s causes the induction of voltage, whose value can be determined by the equation

$$v_{L_S} = L_s \frac{di_s}{dt} \approx L_s \frac{di_d}{dt} \tag{8}$$

which influences the gate circuit even stronger than in time interval t_I. At a very low R_g resistance and the already decreasing i_g current, equation (1) can be reduced to the following form

$$v_{gs} = v_{drv} - L_s \frac{di_d}{dt}. \tag{9}$$

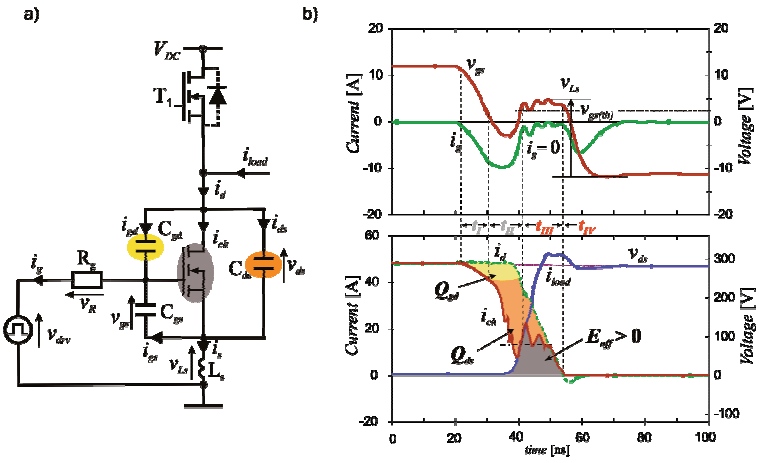


Fig. 6. The effect of parasitic inductance L_s of the source connection on the turn-off transient of the $I_{d,off}$ current with a large magnitude: (a) the equivalent circuit diagram of the commutation circuit; (b) the MOSFET current and voltage waveforms

At the sufficiently high increase of current i_d, the voltage v_{Ls} may reach levels close to the V_{drv} value. In this case, in accordance with equation (9), the v_{gs} voltage may increase above the threshold value of $v_{gs(th)}$, whereby the channel turn-off process will be stopped. If this happens before the i_{ch} current has decreased to zero, the channel current may be sustained until the moment the i_d current decays. During this time, the v_{ds} voltage will already assume large values, causing increased switching losses (Fig. 6b).

3.4. TIME INTERVAL t_{IV}

The last stage of the commutation process (the time interval t_{IV} in Figs. 5 and 6) can be characterized by damped oscillations associated with the exchange of stored energy between the junction capacitance C_{ds} and parasitic inductance L_s of the MOSFET.

The energy losses in the turn-off transient depend chiefly on the source parasitic inductance L_s, the charge Q_{oss} needed for charging the MOSFET output capacitance and on the current i_d time derivative associated with the magnitude of turn-off current $I_{d,off}$. The analysis performed has shown that, in the case of high-voltage power MOSFET with a very low on-state resistance of the channel, the charge Q_{oss} has a magnitude sufficient for slowing down the v_{ds} voltage increase process such that the channel current will still decay at a very small v_{ds} voltage value. Hence, in practice, the situation illustrated in Fig. 6b will take place only when the current being switched off has very large magnitudes.

4. EXPERIMENTAL VERIFICATION

In order to estimate the switching losses in MOSFET turn-off transient, a measuring system was made, which included a H-bridge converter made up of four IPW60R070C6 transistors, supplied from a 280 V direct voltage source and loaded with an inductive receiver (Fig. 7a). The power switches of the bridge were conductive for a duration equal to approx. 50% of the switching period, whereby a rectangular voltage waveform and a triangular current waveform were obtained in the output circuit (Fig. 7b). Thus, soft turn-on of the MOSFET transistors was ensured, which means that the total inverter power losses were equal to the sum of the conduction losses of the transistors and the structural body diodes and the switching losses in turn-off transient. For controlling the transistors, gate drivers were employed, which ensure very short turn-on and turn-off times, achieved owing to the use of a very low additional resistance in the gate circuit and a specialized IXDD614 IC driver with a current output up to 14 A. In addition, in order to increase the fraction of switching losses of the total losses, the test system operated at a switching frequency of 100 kHz.

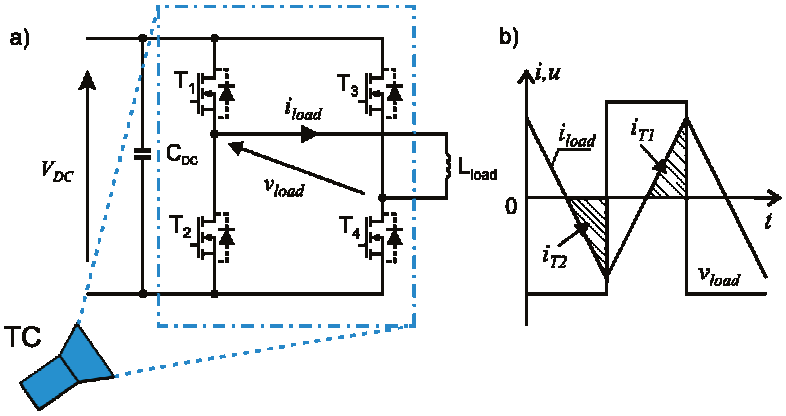
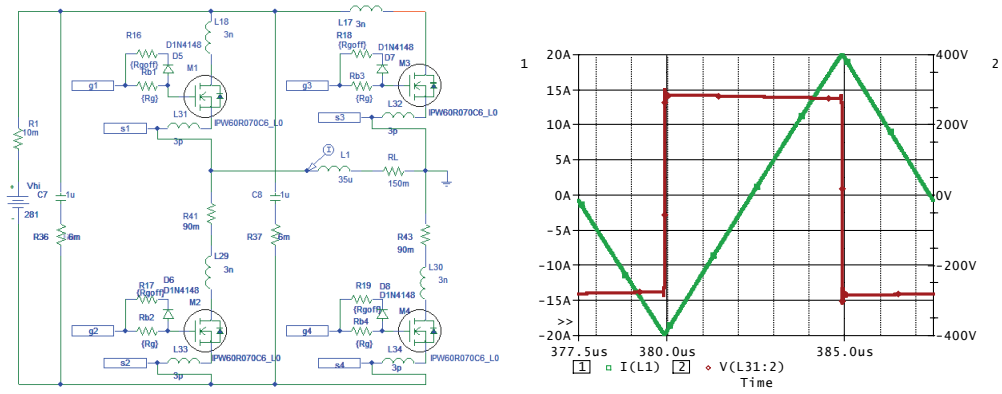


Fig. 7. The system for the measurement of power losses in the MOSFET turn-off transient (a), the load voltage and current waveforms, with the transistor currents T1 (T4) and T2 (T3) indicated (b); (TC – thermal camera)

Firstly, the simulation MOSFET H-bridge model in PSpice was developed (Fig. 8). This model was created using the precise IPW60R070C6 transistor model, which had been previously experimentally verified [10]. This model was used for estimating conduction and switching losses of semiconductor switches under the same conditions as in experimental setup.



a) b)

Fig. 8. Precise PSpice simulation model of power MOSFET H-bridge converter with inductive load (a) and output current and voltage waveforms for L_{load} = 35 μH (b)

The complexity of the phenomena occurring during turn-off transient of the transistors belonging to the MOSFET group under consideration makes the correct identification of energy losses in this process difficult. Due to the internal processes associated with the

existence of a considerable parasitic junction capacitance, the phenomena under discussion cannot be observed using oscilloscope measurements. Similarly, on account of their very small values, these losses cannot be measured by other methods based on the measurements of the input power and output power of the converter [9], since the uncertainty of measurement of relatively large power converted is many times greater than the expected power dissipated in the semiconductor switches due to the turn-off transient.

Hence, to determine the total power losses released in the converter's power switches, the thermovision method [10] was employed, which enables the power losses to be determined based on the average heat sink temperature T_{hs}, on which the transistors are placed. For this purpose, the MOSFET H-bridge in Fig. 7 had been previously subjected to thermal calibration, in which the steady-state heat sink temperature was measured, which resulted from transistor conduction power losses dissipated, caused by the flow strictly specified DC current. As a result of the calibration process, the thermal calibration characteristic (Fig. 9) was obtained, which relates the heat sink temperature with the value of power released in the semiconductor switches.

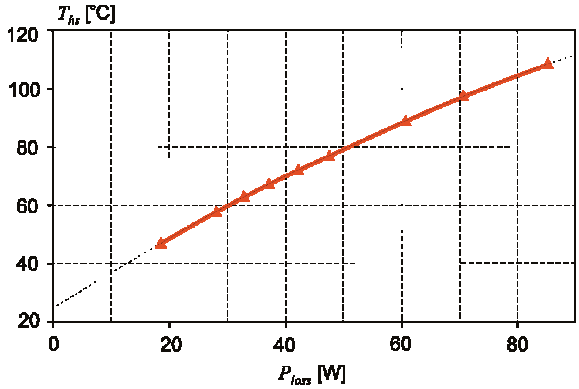


Fig. 9. The thermal calibration characteristic curve for the full bridge MOSFET placed on one heat sink used in the test system in Fig. 7

The test was performed for several different output currents i_{load} (Fig. 10), with their peak value being, at the same time, the value of the current turned off by the transistors. The values of the switching power losses P_{off}, of a single transistor were calculated from the relationship

$$P_{off} = \frac{1}{4}(P_{loss} - P_{con}) \tag{10}$$

where P_{loss} – total full-bridge power losses, as determined by the thermovision method, P_{con} – conduction power losses in all switches, estimated in PSpice simulations based on the instantaneous MOSFET current value and the on-state resistance corresponding to its junction temperature.

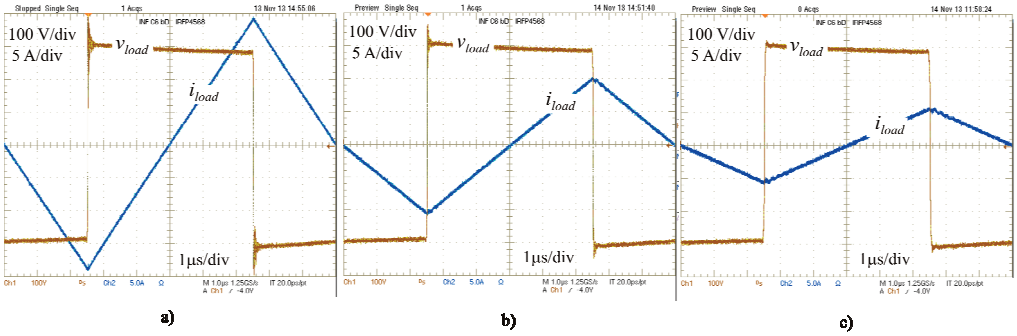


Fig. 10. H-bridge output current and voltage waveforms for different turn-off MOSFET current $I_{d,off}$: (a) L_{load} = 35 µH; (b) L_{load} = 68 µH; (c) L_{load} = 125 µH

The obtained results are shown in Table 1 and Fig. 12. The results indicate very low values of energy E_{off} dissipated in the turn-off process of the transistors under consideration, even at a drain current of approx. 20 A.

It can also be observed that the value of the switching losses does not depend on the value of the turn-off current, which directly confirms the inferences resulting from the aforementioned analysis of the phenomena occurring during switching off of power MOSFET.

Table 1. The power losses of the IPW60R070C6 MOSFET transistor operating in the system shown in Fig. 7

Fig. No.	L_{load}	$I_{d,off}$	I_{load}	T_{hs}	P_{loss}	P_{con}	P_{off}*	E_{off}*
–	[µH]	[A]	[A]	[°C]	[W]	[W]	[W]	[µJ]
Fig. 10a	35	19.85	11.00	52.7	23.53	21.05	0.617	6.17
Fig. 10b	68	10.25	5.95	34.7	7.92	5.49	0.610	6.1
Fig. 10c	125	5.82	3.26	29.9	3.96	1.59	0.592	5.92

*) values referred to a single transistor

The results of measurements with the oscilloscope differ significantly from those obtained from simulation studies and observations using the infrared camera (for all current values of $I_{d,off}$ assumed in the study). This is due to the fact that calculation of the energy loss takes into account an external waveform of the drain current i_d (instead of just the channel current i_{ch}, as shown in Fig. 5) and the voltage at the terminals of the transistor, including the voltage-drop across the transistor lead inductance.

Additional sources of the measurement error are the influences in the gate-source and drain-source circuits by the oscilloscope voltage probe (additional probe capaci-

tance), limited bandwidth and delay of the active probes (e.g., current probe with Rogowsky coil). Detailed discussions of these issues were carried out in [10].

In the case of simulation tests and measurements using an infrared camera there is no influence of external factors on the switching processes of the transistor.

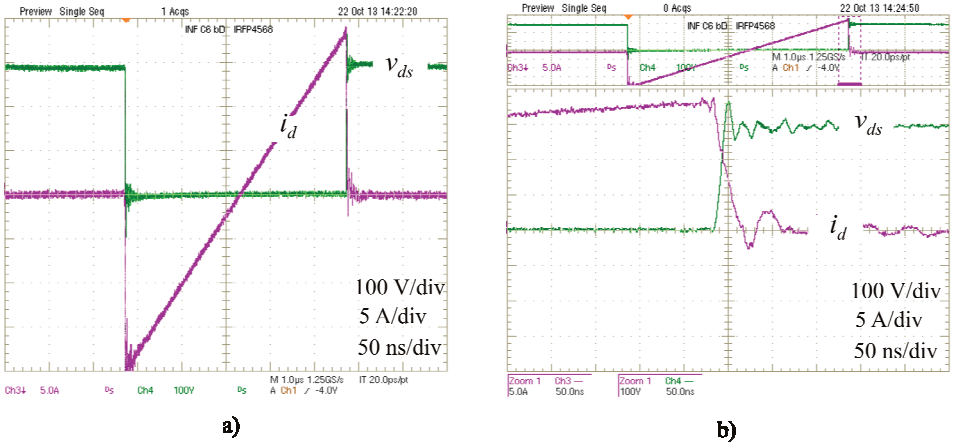


Fig. 11. Oscilloscope waveforms of MOSFET drain current i_d and drain-source voltage v_{ds} during one switching period (a) and during turn-off transient (b) (oscilloscope TDS5034, active current probe – Rogowsky coil ultra mini CWT01 with 20 ns delay time, passive voltage probe TEK P5050)

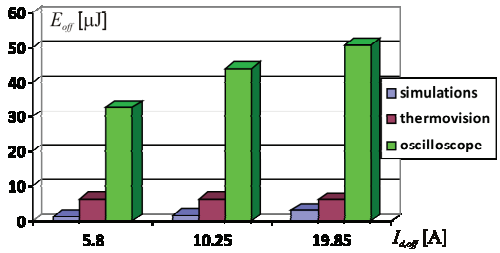


Fig. 12. Comparison of the results of the simulation studies and the thermovision and oscilloscope measurements for the determination of the energy dissipated during turn-off transient of the MOSFET

5. SUMMARY

The paper presents an analytical description explaining the real processes occurring in power MOSFET during their turn-off transient with a driver with a very low gate resistance. The effect of the natural properties on the soft turn-off transient has been confirmed by indicating that only a small part of energy is dissipated, relative to the energy stored in

the output capacitance of the switch. At the same time, it has indicated the causes of the inaccuracies of measurements relying on the determination of switching losses based on observation of the MOSFET's i_d current and v_{ds} voltage waveforms. Both the high dynamism of the variations of transistor current and voltage, as well as the small value of power lost at the turn-off relative to the total converter power make the measurements of switching losses very difficult to accomplish. From the presented experimental measurement results (Fig. 11), one can clearly see the scale of the error of measurements of energy dissipated in the MOSFET turn-off transient when using oscilloscope measurements (Fig. 12). The results provided in the paper confirm good metrological properties of the thermovision method proposed by authors and employed in the study for the determination of energy losses in converters with very high energy efficiency. The present analysis of the dynamic properties of modern silicon MOSFET transistors can be valid also for similar ultra fast power electronic switches manufactured in other technologies (SiC or GaN).

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