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Automatic Parameter Extraction Technique for MOS Structures by C-V Characterization Including the Effects of Interface States

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An automatic MOS structure parameter extraction algorithm accounting for quantum effects has been developed and applied in the semiconductor device analyzer Agilent B1500A. Parameter extraction is based on matching the experimental C-V data with numerical modeling results. The algorithm is used to extract the parameters of test MOS structures with ultrathin gate dielectrics. The applicability of the algorithm for the determination of distribution function of DOS and finding the donor defect level in silicon is shown.

Keywords: C-V measurement, parameter extraction, interface states, quantum simulation, MOS.

1. INTRODUCTION

One of the main elements in microelectronics is the metal-oxide-semiconductor (MOS) structure. When the thickness of the gate dielectric material is scaled down to the nanometer range, the measurement of the structure parameters implies the need to move from analytical formulas to numerical modeling in order to take quantum effects into account [1], [2].

In this article, the measurement of MOS structure parameters is based on capacitance-voltage (C-V) characteristics.

As the dielectric layer thickness is reduced, the effects of discrete energy levels in the gate dielectric interface region, the influence of defects in the dielectric and on the semiconductor/dielectric interface, and the possibility of tunneling through the dielectric are increased, and when polysilicon gate is used, the depletion layer in the border region with the dielectric should also be taken into consideration [3], [4].

A large number of methods exist for the extraction of parameters and calculation of C-V characteristics that account for quantum effects [5]. These methods are based on the calculation of C-V characteristics for each set of parameters. In other works, [6], [7], a statistical approach is suggested, which is based on the comparison of the experimental curve to a database created in advance. This can work for silicon-on-insulator (SOI) structures as well as bulk substrate. The usage of a database containing the self-consistent solutions of Schrodinger-Poisson equations can decrease the modeling time noticeably. However, the influence of interface states and their energy distribution is not considered in the aforementioned works.

It should be noted that interface states can have a large influence on the correctness of the extracted parameters [8], [9], and this is taken into account in the automatic MOS structure parameter extraction procedure described in this work. The energy distribution of the interface states density can provide additional information for the evaluation of technological processes.

In this work, our approach is based on the creation of a database containing numerical solutions of Schrodinger-Poisson equations with the surface states at the dielectric/semiconductor interface region. On this basis, an automatic MOS structure parameter extraction program for the measurement system is created, which can be used to extract parameters and is applicable to structures with ultrathin dielectric layers.

2. SUBJECT & METHODS

By self-consistent, one-dimensional solution of Schrodinger (1)-Poisson (2) equations with the Fermi-Dirac probability density function (3), a database of charge distribution in the substrate is created, which depends on the surface potential. Equations (1), (2) are solved by finite difference method using the effective mass approximation [10], [11] for electrons and holes taking the crystallographic orientation of the substrate into account. This approach accounts for quantum effects that arise with scaling of the dielectric oxide.

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$$\frac{\hbar^2}{2}\frac{\partial}{\partial x}\left[-\frac{1}{2m^*(x)}\frac{\partial}{\partial x}\psi_i(x)\right]+ \\ +U(x)\psi_i(x)=E_i\psi_i(x) \tag{1}$$

$$\frac{\partial}{\partial x}(\varepsilon(x)\frac{\partial}{\partial x}\varphi)= \\ =-e\cdot\frac{p(x)-n(x)+N_D(x)-N_A(x)}{\varepsilon_0} \tag{2}$$

$$f(E)=\frac{1}{1+g\cdot exp\left(\frac{E-E_f}{kT}\right)}, \tag{3}$$

where e - electron charge, k - Boltzmann's constant, T - temperature, ε_0 - dielectric constant, $\hbar$ - normalized Planck's constants, x – coordinate, ψ - wave function, E_i - eigenvalue, U - potential energy, ε - material permittivity, φ - potential, p, n – holes and electrons density, N_D, N_A - the density of ionized donors and acceptors, g – degeneracy factor, E – energy, E_f - Fermi energy.

The interface states charge Q_{ss} is calculated without the database and can depend on many parameters.

For a linear energy distribution of interface states density, an analytic function (4) with the parameter N_{ss0} is used.

The integral (5) of the product of the density of states (DOS) $N_{ss}(E)$ and the probability distribution in all possible energy states with the degeneracy factor g is calculated in the presence of energy distribution of surface defects.

$$Q_{ss}(\varphi)=e(\varphi-\varphi_F)\cdot N_{ss0} \tag{4}$$

$$Q_{ss}(\varphi)=e\int_{E_v}^{E_c}N_{ss}(E)\cdot\frac{dE}{1+g\cdot exp\left[\frac{(e\varphi-E)}{kT}\right]}, \tag{5}$$

where φ_F - Fermi potential, E_c - conductance band minimum energy, E_v - valence band maximum energy.

Density of states can be described by a Gaussian distribution function [12]-[15]. In this paper, two DOS functions based on Gaussian function are used: a distribution with three parameters E_0, N_0, and E_s (6) and more complex distribution (7) with parameters E_0, N_{01}, N_{02}, E_{s1}, E_{s2} using Heaviside function (8).

A more detailed description of the DOS function is in better agreement with the experimental data.

$$N_{ss}(E)=N_0\cdot exp(\frac{-(E-E_0)^2}{E_s^2}) \tag{6}$$

$$N_{ss}(E)=\theta(E_0-E)\cdot \\ \cdot(N_{01}-N_{02}+N_{01}\cdot exp\left[\frac{-(E-E_0)^2}{E_{s1}^2}\right])+ \\ +\theta(E-E_0)\cdot(N_{02}\cdot exp\left[\frac{-(E-E_0)^2}{E_{s2}^2}\right]), \tag{7}$$

$$\theta(x)=\begin{cases}0, & x<0;\\ 0.5, & x=0;\\ 1, & x>0.\end{cases} \tag{8}$$

The dependence of the voltages applied to the structure is calculated by the equation (9), which accounts for the contribution of the work function and effective oxide charge W_{eff}, gate area S, bulk charge Q_s, and gate dielectric capacitance C_{ox}. The dependence of the total capacitance on the gate voltage V_g is defined in (10).

$$V_g=W_{eff}+\varphi-\frac{(Q_s+Q_{ss})\cdot S}{C_{ox}} \tag{9}$$

$$C=\frac{d(Q_s+Q_{ss})}{dV_g} \tag{10}$$

Parameters of the MOS structure are determined by matching the experimental and theoretical C-V characteristics using the algorithm shown in Fig.1. This algorithm and C-V calculations are written in MATLAB.

At each step this algorithm chooses the best value for each parameter ($par_{10},\ldots,par_{n0}$) from all intersections of variable parameters with minimal relative error (ERR). Parameters are varied cyclically about the best values obtained in previous iterations, until the required accuracy (Δ_{ERR}) is obtained or until the maximum iteration limit ($iter_{\max}$) is reached.

In general, the method of parameter variation depends on the iteration step and matching accuracy of experimental data and simulation results.

Matching accuracy or relative error (ERR) is determined by the root mean square (RMS) value (11) or maximum deviation of capacitance (Y_{max}) value (12).

$$RMS=\sqrt{\frac{1}{n}\cdot\sum_{i=1}^{n}\left(\frac{(C_{th})_i-(C_{exp})_i}{C_{max}}\right)^2}\cdot 100\% \tag{11}$$

$$Y_{max}=max\left|\frac{C_{th}-C_{exp}}{C_{max}}\right|\cdot 100\%, \tag{12}$$

where C_{th} - capacitance value of theoretical C-V curve, $C_{\exp}$ - capacitance value of experimental C-V curve, $C_{\max}$

- maximum capacitance value of experimental C-V curve, n - the number of voltage points.

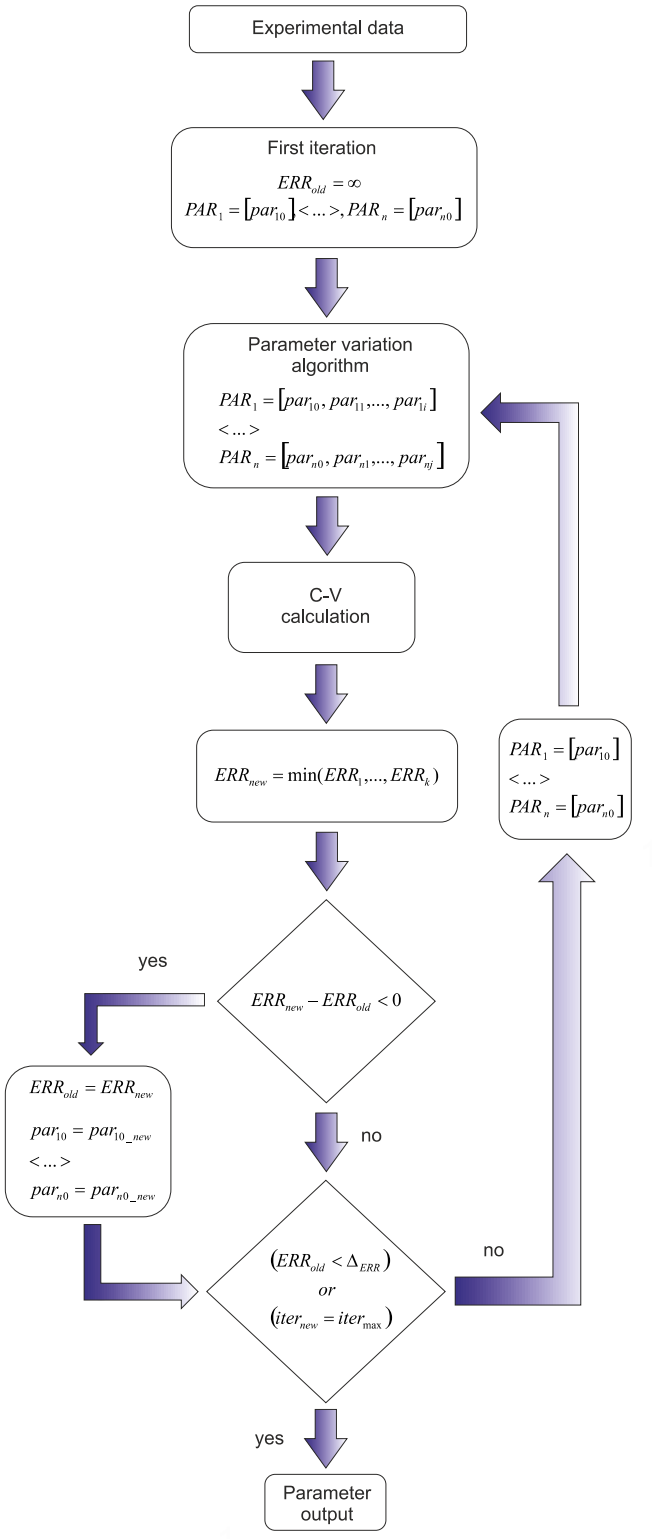

Fig.1. The flowchart of the MOS structure parameter extraction algorithm, which uses the matching of the modeling results and the experimental data.

The calculation of the work function W_{wf} with the contribution of oxide fixed charge Q_f is calculated by the flat band voltage shift ΔV_{fb} between the experimental and theoretical C-V characteristics (13).

$$W_{eff} = W_{wf} + Q_f = \Delta V_{fb} \tag{13}$$

It is assumed that the experimental curve has the same parameters as the theoretical C-V curve when the required accuracy of *RMS* value and (or) $Y_{\max}$ value is reached.

3. MEASUREMENT METHODS

The accuracy of C-V measurements influences the accuracy of extracted MOS structure parameters. When C-V characteristics are measured, the factors decreasing the measurement accuracy, such as gate leakage currents and the influence of parasitic elements of the measurement circuit, should be taken into account.

In this work, a measurement complex consisting of Agilent B1500A Semiconductor Device Parameter Analyzer and SUSS MicroTec PA 300 semiautomatic probe station is used for the measurement of MOS structure C-V characteristics.

The Agilent B1500A is furnished with a built-in module for quasi-static C-V measurement with the option to compensate the gate leakage current.

For high frequency measurements (> 1 kHz), an impedance analyzer and special probes with minimal parasitic components which maintain 4-terminal pair measurement scheme (such as DCP-100 from Cascade Microtech) should be used. In the B1500A Semiconductor Device Parameter Analyzer, the Multi Frequency Capacitance Measurement Unit (MFCMU), which is based on the auto-balancing bridge scheme [16], is tasked with the impedance measurements. The Semiconductor Device Parameter Analyzer automatically calculates the equivalent 2-element model [17] of any device by measuring the impedance Z and phase θ. The calculation of the total capacitance from the 2-element model can lead to erroneous estimation of its value, especially when measuring at high frequency [3]. For a more accurate estimation of the MOS structure capacitance in view of leakage currents, a 3-element model can be used [18]

It should be noted that the 3-element model is applicable on a limited set of frequencies that depends on the measurement device accuracy and the values of parasitic elements [19].

When the 3-element model cannot be applied, the models containing more parasitic elements should be used. Analytic solutions of such models are considered in [20]-[24], but the general solution method for such models is the numerical solution.

A MOS equivalent capacitance determination algorithm was written for the Agilent B1500A, which utilizes high-frequency measurements and 3-element model calculated from the 2-element model extracted from the experimental data. For the cases when the 3-element model cannot be

applied, an option to numerically calculate the equations system with more parasitic elements for equivalent capacitance determination is included. This option uses basic MATLAB functions.

The algorithm works directly after measurement data is obtained. Measurements and parameter extraction are done in the same program written in Agilent VEE Pro programming language, so there is no need to transfer C-V data to the algorithm manually.

4. MEASUREMENT AND PARAMETER EXTRACTION RESULTS

The MOS structure parameter extraction algorithm was verified using existing MOS structure (Si/SiO_2/PolySi) with thick SiO_2 and low density of interface states N_{ss}.

Dielectric physical thickness was measured by spectroscopic ellipsometry and value of *17.9 nm* was found. Bulk dopant concentration N_{sub} was measured during manufacturing on CSM/Win Semiconductor Measurement System using MDC Model 802-105 mercury probe and value of $1.27 \cdot 10^{17}\, cm^{-3}$ was found. The gate area of the test structure was $4 \cdot 10^{-4}\, cm^2$.

The measurement results and the theoretical C-V curves calculated using the extracted parameters from the developed algorithm are shown in Fig.2. The sets of found values are shown in Table 1. In this and following tables, t_{ox} - equivalent oxide thickness (EOT), N_{sub} - bulk dopant concentration.

Results show agreement between extracted values and values obtained from measurements during manufacturing, which confirms the applicability of the algorithm.

Next, parameter extraction on structures with ultrathin dielectric layers was attempted. Test structures Si/SiO_2/Molybdenum were made with three dielectric thicknesses (*5 nm* and less) for verification of the parameter extraction algorithm. The wafers were p-type silicon ($N = 10^{15}\, cm^{-3}$). Boron implantation was carried out with energy $E = 40keV$ and dose $D = 10 \cdot 10^{-6}\, C \cdot cm^{-2}$, with subsequent annealing in nitrogen N_2, *T = 1000°C, 60 min* and thermal oxidation with *T = 900°C*. The varying dielectric thickness was obtained by wet etching of the base oxide. Dielectric physical thicknesses were measured by spectroscopic ellipsometry and the following values were obtained: for wafer №1 *5 nm*, for wafer №2 *3 nm*, and for wafer №3 *2 nm*. The gate area of MOS structures for wafers №1 and №2 is $1 \cdot 10^{-4}\, cm^2$, for wafer №3 – $2.8 \cdot 10^{-5}\, cm^2$. Silicon effective masses of electrons and holes are calculated for the specific crystallographic orientation of the p-type wafer (100) for self-consistent solution of Schrodinger-Poisson equations.

The test structures have large gate leakage currents. The quasi-static C-V characteristics could not be obtained with high enough accuracy, even when using the B1500A leakage current compensation function. Only high frequency C-V (HFCV) characteristics with correct equivalent MOS structure capacitance model will be considered.

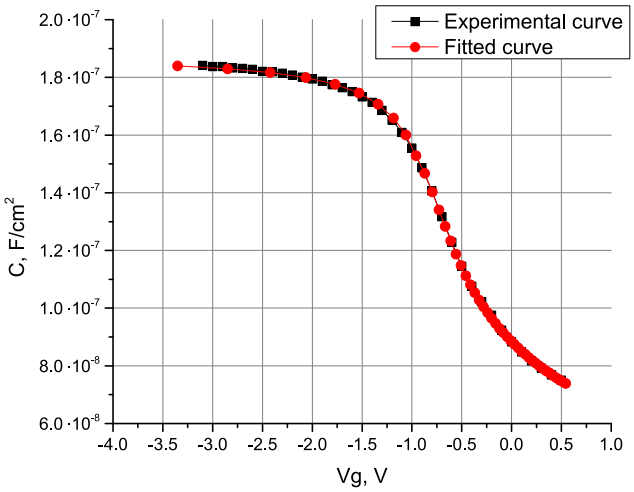

Fig.2. Comparison of high frequency experimental and theoretical C-V characteristics with the parameters from Table 1. using Gaussian function (6) to describe the DOS.

Table 1. Parameter extraction results using (6) to describe the DOS.

t_{ox} [cm]	$18.12 \cdot 10^{-7}$
N_{sub} [cm^{-3}]	$1.15 \cdot 10^{17}$
E_0 [eV]	$-1.58 \cdot 10^{-1}$
N_0 [cm^{-2}]	$2.50 \cdot 10^{10}$
E_s [eV]	$9.52 \cdot 10^{-1}$
V_{fb} [V]	$-9.59 \cdot 10^{-1}$
W_{eff} [V]	$-5.89 \cdot 10^{-1}$
RMS [%]	$2.75 \cdot 10^{-1}$
Ymax [%]	0.01

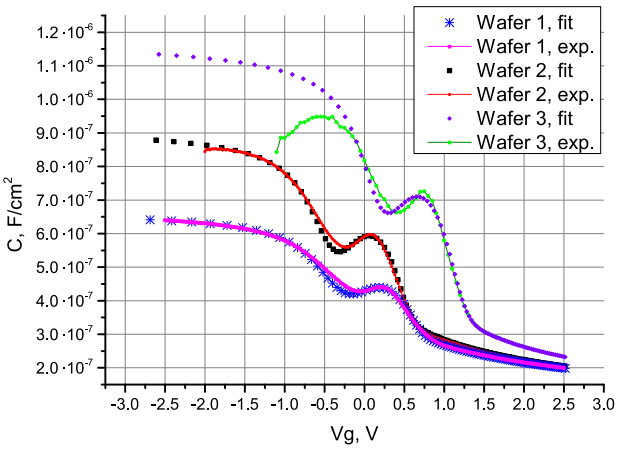

Fig.3. Comparison of high frequency experimental and theoretical C-V characteristics with the parameters from Table 2. using Gaussian function (6) to describe the DOS.

The HFCV measurement results and the theoretical C-V curves calculated using the extracted parameters from the developed algorithm are shown in Fig.3. These curves exhibit a step in the depletion region, which is assumed to arise from existence of an impurity defect level with high

N_{ss} value. To address this issue, Gaussian function (6) was used to describe the DOS. The sets of found values are shown in Table 2. The values of E_0 were found with respect to the middle of the bandgap.

Table 2. Parameter extraction results using (6) to describe the DOS.

Wafer	№1	№2	№3
t_{ox} [cm]	$5.01\cdot10^{-7}$	$3.60\cdot10^{-7}$	$2.78\cdot10^{-7}$
N_{sub} [cm^{-3}]	$1.61\cdot10^{18}$	$1.60\cdot10^{18}$	$1.55\cdot10^{18}$
E_0 [eV]	$-1.30\cdot10^{-1}$	$-1.52\cdot10^{-1}$	$-1.40\cdot10^{-1}$
N_0 [cm^{-2}]	$3.88\cdot10^{12}$	$6.13\cdot10^{12}$	$6.62\cdot10^{13}$
E_s [eV]	$1.24\cdot10^{-1}$	$1.32\cdot10^{-1}$	$1.76\cdot10^{-1}$
V_{fb} [V]	$-8.38\cdot10^{-1}$	$-7.93\cdot10^{-1}$	$-9.87\cdot10^{-2}$
W_{eff} [V]	$-1.36\cdot10^{-1}$	$-5.35\cdot10^{-2}$	$6.67\cdot10^{-1}$
RMS [%]	$9.93\cdot10^{-1}$	$9.17\cdot10^{-1}$	1.82
Ymax [%]	5.29	5.02	5.40

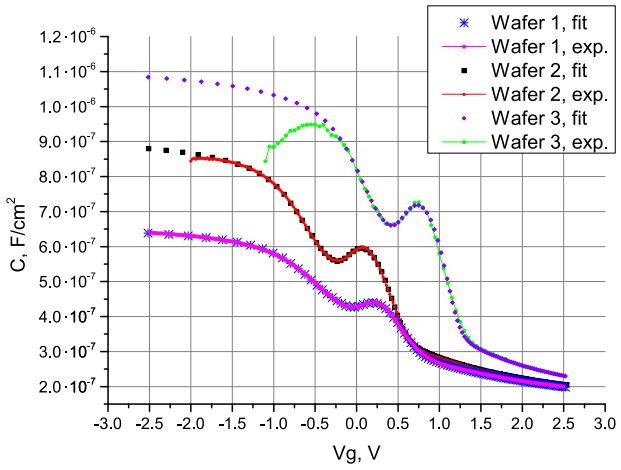

Fig.4. Comparison of high frequency experimental and theoretical C-V characteristics with the parameters from Table 3. using function (7) to describe the DOS.

Table 3. Parameter extraction results using (7) to describe the DOS.

Wafer	№1	№2	№3
t_{ox} [cm]	$5.01\cdot10^{-7}$	$3.57\cdot10^{-7}$	$2.88\cdot10^{-7}$
N_{sub} [cm^{-3}]	$1.61\cdot10^{18}$	$1.62\cdot10^{18}$	$1.62\cdot10^{18}$
E_0 [eV]	$-1.62\cdot10^{-1}$	$-1.61\cdot10^{-1}$	$-1.60\cdot10^{-1}$
N_{01} [cm^{-2}]	$2.53\cdot10^{12}$	$4.01\cdot10^{12}$	$4.90\cdot10^{12}$
N_{02} [cm^{-2}]	$4.13\cdot10^{12}$	$6.32\cdot10^{12}$	$8.31\cdot10^{12}$
E_{s1} [eV]	$3.20\cdot10^{-2}$	$5.35\cdot10^{-2}$	$3.91\cdot10^{-2}$
E_{s2} [eV]	$1.50\cdot10^{-1}$	$1.49\cdot10^{-1}$	$1.54\cdot10^{-1}$
V_{fb} [V]	$-8.94\cdot10^{-1}$	$-8.75\cdot10^{-1}$	$-1.62\cdot10^{-1}$
W_{eff} [V]	$-1.33\cdot10^{-1}$	$-7.96\cdot10^{-2}$	$6.60\cdot10^{-1}$
RMS [%]	$1.89\cdot10^{-1}$	$2.24\cdot10^{-1}$	$8.77\cdot10^{-1}$
Ymax [%]	1.16	1.72	4.46

The usage of function (7) to describe the DOS leads to better accuracy, which is shown in Fig.4. The extracted parameters are shown in Table 3.

The difference between energy distributions of interface states density (6) and (7) using extracted parameters is shown in Fig.5. The Fermi-Dirac probability density function of occupancy of energy levels (3) with degeneracy factor 2 was used to calculate the interface states charge.

The accumulation region on wafer №3 could not be measured because of the high leakage currents and the difficulty of the equivalent MOS capacitance model extraction. For the correct extraction of the oxide thickness on wafer №3, the value of the energy distribution maximum E_0 was taken as mean value from wafers №1 and №2, and fixed on this level.

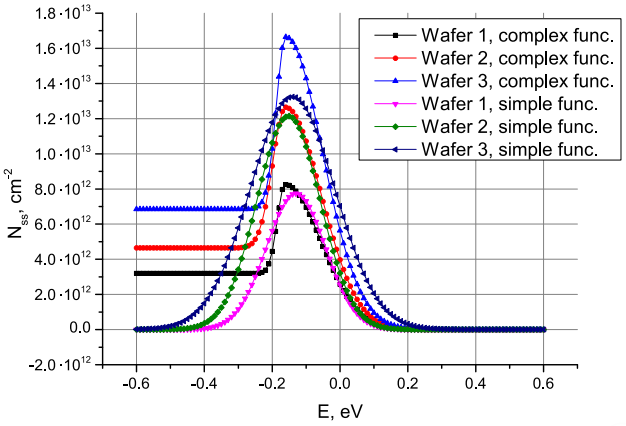

Fig.5. Energy distributions of interface states density (6) and (7) using extracted parameters from Table 2. and Table 3.

5. Discussion

Using the experimental data, the main MOS structure parameters are determined, including EOT for the three wafers (*5 nm*, *3.6 nm*, and *2.9 nm*). Regarding wafer №3, the correctness of the determined dielectric thickness value depends on the assumption that test structures on this wafer have exactly the same defect energy level as the structures on other wafers. The sharp decrease in capacitance value in the accumulation region of test structure on wafer №3 arises because of a measurement error caused by high gate leakage current (namely, in case of high leakage currents, parallel resistance R_p in the 3-element model is very small, which corresponds to extremely small values of phase θ and, consequently, inability to correctly measure the imaginary part of impedance Z which contains capacitance). Test structures with smaller leakage current (which would mean gate area less than $2.8\cdot10^{-5}cm^2$) are not available at this time.

Value of EOT from experimental data extraction and physical thickness value of SiO2 obtained from spectroscopic ellipsometry can differ due to transition layers with different ε at the interface of the SiO2 layer.

EOT calculated from parameter extraction algorithm is smaller than capacitance equivalent thickness obtained from the same curves in Fig.3., Fig.4. due to influence of quantum effects.

The validity of extracted parameters is also indirectly confirmed by the fact that the values of energy distribution coefficients of DOS are increasing when the dielectric layer thickness is reduced (Fig.5.), as the probability of the tunneling of dopant atoms through the dielectric layer to the silicon/dielectric interface is also increased.

Therefore, the developed algorithm can be used for MOS structures whose measured C-V characteristics lack accumulation region either partially or fully, including structures on SOI substrates.

The measurements have shown a defect donor level with the energy value about *0.39-0.41 eV* from the valence band level, close to the middle of bandgap, which is around the level of iron (Fe) atoms in silicon [25]. The presence of iron atoms can be explained by the properties of the sputtering device, in which the molybdenum target was attached to a base made of iron. The accuracy of the defect energy level determination depends on C-V characteristics measurement accuracy and on the charge calculation functions.

It can be seen from the energy distributions of DOS (Fig.5.) calculated using (7) that other defects (i.e., molybdenum) can also exist with smaller DOS values and lower energy values (closer to the Si valence band). For the description of those defects, a linear energy distribution of DOS should suffice.

The MOS structure parameter extraction algorithm is based on the simultaneous comparison of numerous theoretical data arrays with experimental data, and takes only a few seconds to calculate the parameters.

The sensitivity of C-V characteristics to the distribution of DOS depends on the region of the C-V curve (accumulation, depletion or inversion) and on the substrate concentration near the dielectric/semiconductor interface for depletion/weak inversion regions. The minimum values of the coefficients N_{01}, N_{02} in the distribution of DOS (7) for MOS structures with $N_{sub} = 1.6 \cdot 10^{18} cm^{-2}$, for which the effects of defect levels in depletion/weak inversion regions can be detected, are about $N_0 = 5 \cdot 10^{11} cm^{-2}$. Higher sensitivity can be achieved with lower values of substrate concentration.

6. Conclusion

A MOS structure parameter extraction algorithm which accounts for quantum effects, DOS and their energy distributions is developed.

The parameters of test structures with ultrathin dielectric layers, high leakage currents and high defects concentration level are extracted using the developed algorithm. A defect donor level was found with its value close to the energy level of Fe atoms in silicon. For the verification of this assumption, additional investigations of the test structures must be conducted.

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