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Improved efficiency of p-type quasi-mono silicon blanket emitter solar cell by ion implantation and backside rounding

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A novel type of silicon material, p-type quasi-mono wafer, has been produced using a seed directional solidification technique. This material is a promising alternative to traditional high-cost Czochralski (CZ) and float-zone (FZ) materials. This study evaluates the application of an advanced solar cell process that features a novel method of ion-implantation and backside rounding process on p-type quasi-mono silicon wafer. The ion implantation process substituted for thermal $POCl_3$ diffusion leads to better R_{sheet} uniformity (<3 %). After screen-printing, the interface of Al and back surface field (BSF) layers was analyzed for the as prepared samples and the samples etched to three different depth. SEM showed that increased etch depth improved both BSF layer and Al–Si layer. The IQE result also showed that the samples with higher etching depth had better performance at long wavelength. The I – V cell tester showed that the sample with the etching depth of 6 μm ± 0.1 μm had the greatest efficiency, due to the highest V_{oc} and I_{sc}. The solar cell fabricated in this innovative process on 156 × 156mm p-type quasi-mono silicon wafer achieved 18.82 % efficiency.

Keywords: *quasi-mono wafer; ion implantation; $POCl_3$*

1. Introduction

Many governments have provided policy incentives to increase the demand for photovoltaics (PVs) such as solar rooftop systems, with the result that the solar energy market has grown at least 20 % per annum over the past ten years. However, the final purpose of solar electric power is to achieve grid parity, for which reduced manufacturing cost and increased efficiency are very important. This study presents a novel material, p-type quasi-mono wafer, processed by ion implantation and backside rounding, which can help achieve these goals.

Multicrystalline silicon (mc–Si) wafers are used in solar industry due to their relatively low cost as compared to Czochralski (CZ) grown monocrystalline material. However, multicrystalline silicon wafers have lower efficiency. This results from the defects which could be attributed to grain boundaries. A novel type silicon material, p-type quasi-mono, produced by a seed directional solidification technique [1] used for multicrystalline ingots, is a candidate for high efficiency photovoltaics. It has the potential to achieve higher cell efficiencies compared to multicrystalline silicon material, with the same average minority carrier lifetime [2], and higher power output than monocrystalline pseudo-square silicon wafers, due to higher packing density with full-square dimension. In this study, p-type quasi-mono wafers were used as the initial substrate material to produce high-efficiency solar cells.

There are several industrial processes available to produce high-efficiency solar cells, including metal wrap-through (MWT) [3], emitter wrap-through (EWT) [4], interdigitated backside contact (IBC) [5], laser fired contacts [6], and ion implanted cells [7]. Of these methods, ion implantation is attractive for mass production. In this paper, a blanket emitter processed by ion implantation is combined with a backside rounding process to achieve high efficiency >18.8 % on p-type quasi-mono wafers.

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2. Experiment

A 6-inch (156 × 156 mm^2, full square-shaped) p-type quasi-mono wafer (GCL-Poly Energy Holdings Limited) with a resistivity of 1.5 ohmcm, and a thickness of 200 μm was used as the substrate in this study. A mono-crystalline seed was placed at the bottom of a crucible, and polysilicon was then loaded on the top of the seed. The underlying seed allowed quasi-mono silicon ingots to grow in the DS furnace. In this paper, 9 ingots were picked from the center of a brick for use as starting material. The wafer surface from the inner 9 ingots had more than 90 % area oriented in <100> direction, and less than 10 % in other directions. These 9 inner ingots were then sliced into wafers. Fig. 1 shows the distribution diagram of the inner 9 ingots in the brick. Fig. 2 compares the ion implantation process both with (experimental group) and without (control group) backside rounding. First, in order to reduce the surface stress caused by the wire saw, an alkaline cleaner – KOH solution (5.04 wt.%) was used to remove the saw damage. As the <100> crystalline area exceeded 90 %, an alkaline texturing process was carried out in KOH:IPA:H_2O with a volume ratio 1:1.6:34. Surface texture produced pyramids that absorbed incoming light and increased the light path in the silicon bulk.

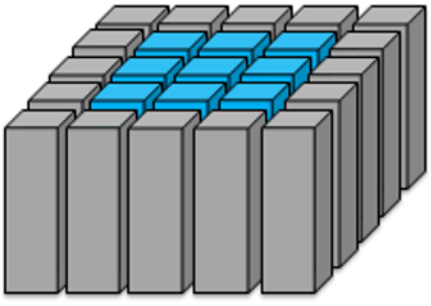


Fig. 1. Distribution diagram of 9 inner ingots.

The next step for the experimental group was backside rounding. An inline backside rounding processing system with roller-type transportation, InOxSide tool (Rena, GmbH) was used to prepare the backside surface pyramids.

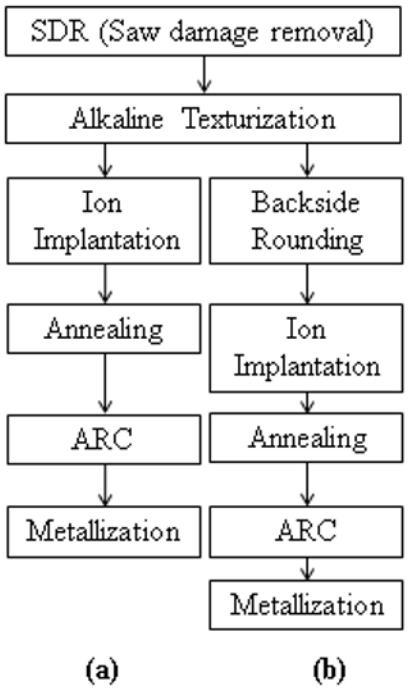


Fig. 2. Comparison of ion implantation process without (a) and with (b) backside rounding process.

The backside rounding process was carried out to achieve four different etching depths, termed as ED0, ED3, ED6, and ED9, corresponding to etching depths of 0 (control), 3, 6, and 9 μm (± 0.1 μm), respectively. In order to achieve these etching depths, the process temperatures were 10 °C, 15 °C, and 20 °C for ED3, ED6 and ED9 groups, respectively. Ion implantation was performed with an inline, high-throughput (>1000 pcs/h) machine (VESA, Varian Semiconductor Equipment Associates). The surface was bombarded by P^+ ions at the ion beam energy of 10 keV and a dose of 3.0×10^{15} P^+/cm^2. Crystal damage that occurred during the ion bombardment procedure was recovered by a subsequent high-temperature thermal annealing step, in which a thin silicon oxide layer formed on the wafer surface.

The dopant concentration profile after the high-temperature annealing process was different from the profile of $POCl_3$ made by diffusion [8–11].

After annealing, SiNx was deposited on the silicon surface by PECVD (plasma-enhanced vapor phase deposition). In this study, wafers were

automatically placed into a batch-type machine (Centrotherm, GmbH) and subjected to PECVD process. The SiNx layer functioned as an anti-reflection coating (ARC), which increased the amount of light absorbed by silicon and also passivated the silicon surface.

After ARC deposition, metallization was formed by a Baccini belt-type screen-printing system and co-fired by a Despatch system. Silver (Ag) paste (DuPont 17F) was used to screen-printing three busbars and 83 finger lines. Backside silver (Ag) paste (DuPont PV-157) and backside aluminum (Al) paste (Monocrystal 1203) were used.

A single-cell flasher system with two illumination ranges in one flash was used for measurement under standard test conditions (STC): irradiance of 1000 W/m^2, solar spectrum of AM 1.5 and temperature of 25 °C. Electrical characteristics, including V_{oc}, I_{sc}, FF, P_{max}, and cell efficiency were obtained from the I – V curves. The shunt resistance R_{sh} was determined from the linear slope of the reverse dark current on each cell. According to IEC 60891 conditions, R_{sh} was calculated from two I – V curves at 1000 W/m^2 and 500 W/m^2 irradiance.

3. Results and discussion

In order to determine the process performance, 400 pieces were textured for the same time. Fig. 3(a) shows the appearance of quasi-mono silicon after texturing. The figure shows the area which is not <100> oriented around the edge. Fig. 3(b) shows 550 × SEM image (taken with JSM-6510, JEOL Ltd.) of the pyramid topology around the edge. As seen, there are three different pyramid orientations around the edge. Fig. 4 shows a photoluminescence (PL) image of quasi-mono silicon after texturing by LIS-R1 (BT Imaging Pty., Ltd.). Unlike monocrystalline wafers, quasi-mono silicon wafers have an area of high recombination (dark area) within the wafer, which reduces their efficiency compared with the monocrystalline ones. After texturing, the wafers were randomly split into 4 groups of 100 pieces. Then, 3 groups underwent backside rounding process with the InOxSide machine (Rena GmbH). The remaining group was the control group, which was not backside rounded. Here, SEM was used to analyze the pyramid topology on the backside <100> surface. Fig. 5(a) shows a 3000 × SEM image of the pyramid topology without backside rounding. As can be seen, the pyramids are well visible on the wafer surface. Fig. 5(b) shows a 3000 × SEM image of the pyramid topology for the etching depth of 3µm ± 0.1 µm after the backside rounding process. The figure shows that the chemicals started to isotropically etch the concave part of the pyramids. Fig. 5(c) and Fig. 5(d) show 3000 × SEM images of the pyramid topology for etching depths of 6 µm ± 0.1 µm and 9 µm ± 0.1 µm, respectively. As the etching depth increases, the concavity of the pyramids becomes larger.

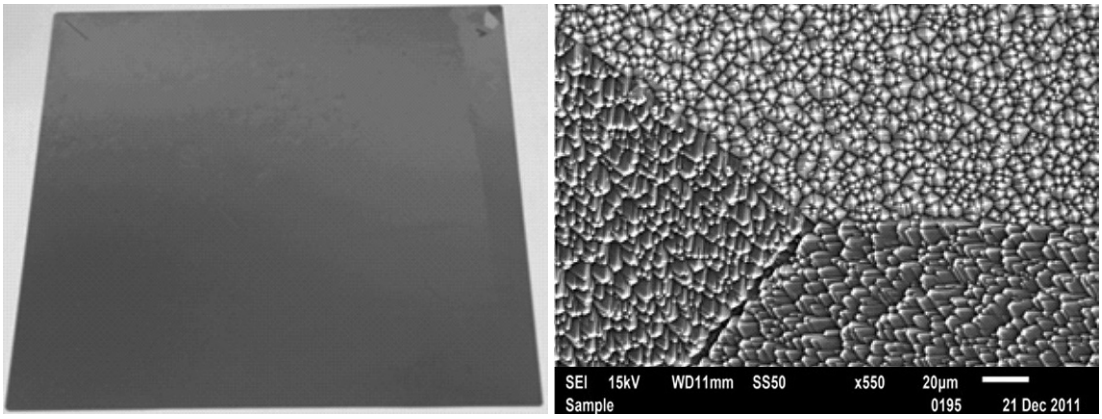
After backside rounding etching, a U-4100 UV-vis-NIR spectrophotometer (Hitachi) with an integrating sphere was used to measure the reflectivity on the (100) surface. Four pieces of the wafer were randomly selected from each group and measured at five points to give an average value. Fig. 6 compares the (100) surface reflectivity for the samples with four different etching depths after backside rounding.

As seen in Fig. 6, there is an apparent difference between the samples at long wavelengths (>1100 nm). As the etching depth increases, so does reflectivity. This is due to the altered topology of the backside pyramids. The weighted reflectance $R_w\%$ is calculated to identify reflectivity, using the formula 1 given in [12].

$$R_w\% = \frac{\int_{\lambda 1}^{\lambda 2} F_i(\lambda) Q_i(\lambda) R(\lambda) d\lambda}{\int_{\lambda 1}^{\lambda 2} F_i(\lambda) Q_i(\lambda) d\lambda}. \qquad (1)$$

Here, $F_i(\lambda)$ is the photon flux, and $Q_i(\lambda)$ is the cell internal quantum efficiency [13, 14]. Table 1 compares the R_w % for four different etching depths. The R_w % of ED9 is 15.03 %, which is higher than for the other samples. This is due to poor response at the long wavelengths.

After backside rounding, the four groups of wafers were automatically transferred into an implantator chamber and the P^+ ions were implanted onto the wafer surface. Then, high-temperature (800 °C) annealing was performed to activate



(a) (b)

Fig. 3. (a) Appearance of quasi-mono silicon after texturing; (b) 550 × SEM images of pyramid topology around the edge.

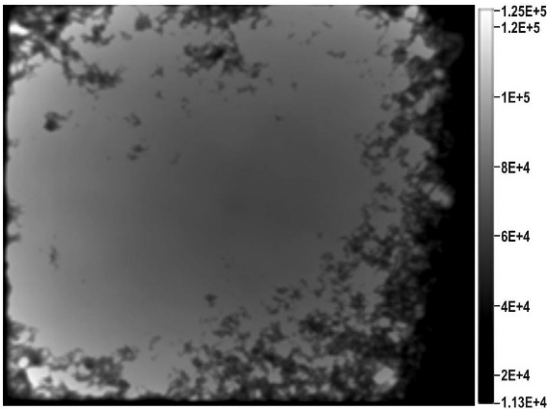


Fig. 4. Photoluminescence (PL) image of quasi-mono silicon after texturing.

Table 1. R_w % comparison for different etching depths.

	ED0	ED3	ED6	ED9
R_w %	14.61	14.83	14.91	15.03

the dopant on the wafer surface. Sheet resistance (R_{sheet}) was measured with a four-point probe (Quatek Co., Ltd.). Table 2 lists the R_{sheet} results for different etching depths after annealing. The R_{sheet} values of the four groups have an average 65.27 ohm/sq and good uniformity (<3 %). The better uniformity compared with other methods is due to precise control of the ion implantation

Table 2. R_{sheet} results for different etching depths after annealing.

R_{sheet} [ohm/sq]	**Max**	**Average**	**Min**	**Uniformity (%)**
ED0	67.48	65.31	63.82	2.80%
ED3	67.41	65.82	63.91	2.66%
ED6	67.21	64.72	63.64	2.76%
ED9	67.67	65.26	63.93	2.87%

process. During annealing, a thin SiO_2 layer was also formed on the wafer surface, and an ellipsometer (SEMILAB Semiconductor) with a single-wavelength HeNe laser operating at a wavelength of 632.8 nm was used to measure the thickness of SiO_2. The thickness of SiO_2 was measured on four pieces randomly selected from the wafer representing each group. Each wafer was measured at 9 points, and the results were averaged. Table 3 compares SiO_2 thicknesses and uniformities for the samples ED0, ED3, ED6, and ED9. The results show that the thickness of SiO_2 is around 16.6 nm and has good uniformity (<1 %). The R_{sheet} resistance and the thickness of SiO_2 are not related to etching depth.

After the annealing process, the anti-reflective SiN_x layer was deposited on the top of the SiO_2 in order to minimize reflection from the front surface

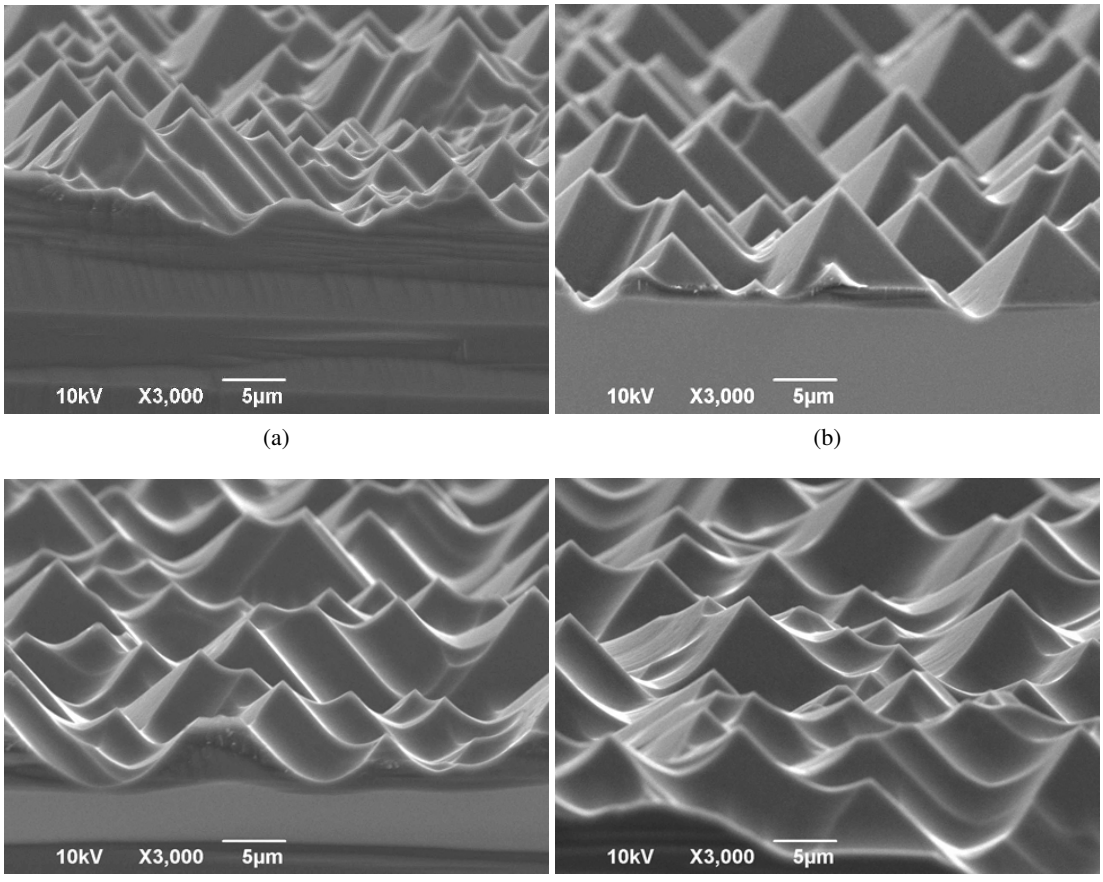


Fig. 5. SEM images of pyramid topology: (a) 3000 × process without backside rounding process; (b) 3000 × process with backside rounding of 3 μm ± 0.1 μm; (c) 3000 × process with backside rounding of 6 μm ± 0.1 μm; (d) 3000 × process with backside rounding of 9 μm ± 0.1 μm.

Table 3. Comparison of SiO_2 thickness and uniformity for different etching depths.

	ED0	**ED3**	**ED6**	**ED9**
SiO_2 thickness (nm)	16.62	16.53	16.74	16.51
Uniformity (%)	0.82%	0.74%	0.85%	0.62%

Table 4. R_w% comparison for different etching depths after ARC deposition.

	ED0	**ED3**	**ED6**	**ED9**
R_w%	4.94	5.18	5.20	5.28

of the cell. Fig. 7 shows the reflection from the samples ED0, ED3, ED6, and ED9 on <100> surface. The profile shows that the reflectivity of ED9 is the highest at long wavelengths. Comparing the results after backside rounding, the differences between each group are reduced at longer wavelengths. Table 4 lists the values of R_w% after ARC deposition, in which ED9 has the highest R_w of 5.28 %.

Finally, metallization was performed by screen-printing and co-firing, and the relationship between the four different etching depths and back surface field (BSF) was investigated by SEM. The samples ED0, ED3, ED6, and ED9 were broken along the <100> direction, and were etched in 1:3:6-HF:HNO_3:CH_3COOH for 10 s. The area of the Al-BSF (heavily p-doped) and the bulk (lightly p-doped) regions were defined by this

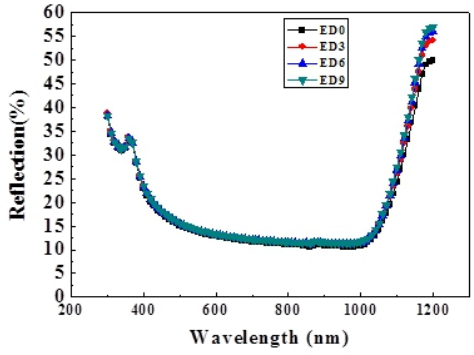


Fig. 6. Comparison of <100> surface reflectivity for four different etching depths after backside rounding process.

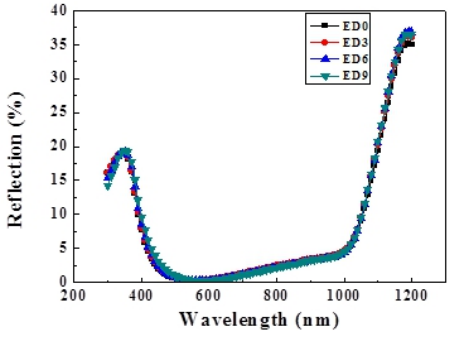


Fig. 7. Comparison of <100> surface reflectivity for four different etching depths after ARC.

etching [15]. Fig. 8(a) shows a cross-sectional SEM image of the BSF topology without backside rounding process. In this figure, the BSF layer and Al–Si alloy layer are rougher than in the other samples. Fig. 8(b) shows the cross-sectional SEM image of ED3, in which the BSF and Al–Si alloy layers are much smoother than those of ED0. Figs. 8(c) and 8(d) show cross-sectional SEM images of ED6 and ED9, in which the uniformity of BSF and Al–Si is better than that of ED0 and ED3. Better BSF resulted in higher V_{oc} and I_{sc} values for ED6 and ED9 samples than those achieved for ED0 and ED3.

Fig. 9 shows the internal quantum efficiency (IQE) response of the samples with four different etching depths. In the mid- and long wavelength region, the IQE response of ED6 and ED9 samples is higher than that of ED0 and ED3. The better IQE performance is due to uniform BSF and Al–Si layer. All electrical characteristics were measured with an I – V cell tester system. Fig. 10 shows that V_{oc} and I_{sc} increase with greater etching depth. Higher V_{oc} and I_{sc} are due to higher carrier lifetimes resulting from better performance of BSF and Al–Si alloy layer after backside rounding. Better BSF and Al–Si alloy reduce the dangling bonds and density of surface defect states, which, on the other hand, inhibit recombination velocity on the back surface [16]. The lower I_{sc} of ED9 than I_{sc} of ED6 is due to the higher reflectance of ED9 sample. Fig. 11 shows that R_S and FF of the samples subjected to backside rounding process are better than that of control group. This is due to uniform BSF and Al–Si layers, which provides better metal and silicon contact. Fig. 12 shows the efficiency of ED0, ED3, ED6, and ED9 samples. The best performance is obtained for the sample ED6. The electrical characteristics (Table 5) show that the best average efficiency is 18.82 % and the highest efficiency is 19.08 %. Higher efficiency is due to higher V_{oc} and I_{sc} values, which result from better BSF performance.

4. Conclusions

This study investigated quasi-mono wafer, a novel type of silicon material for high-efficiency solar cells produced by ion implanted emitter formation and backside rounding. This innovative process increased the cell efficiency to 18.82 %. In the backside rounding process, backside pyramids were prepared with a high-throughput (>2500 pcs/hr) InOxSide tool. SEM images showed that, for the etching depth greater than 6 μm, the concavity of pyramids became larger. As the etching depth increased, reflectivity increased at long wavelengths. The R_{sheet} uniformity was less than 3 %, which was due to precise control of the ion implantation process. SEM images taken after metallization showed that the samples with etching depths of 6 μm ± 0.1 μm and 9 μm ± 0.1 μm had more uniform BSF and Al–Si alloy layers. The IQE result showed that the samples with the higher etching depth had better

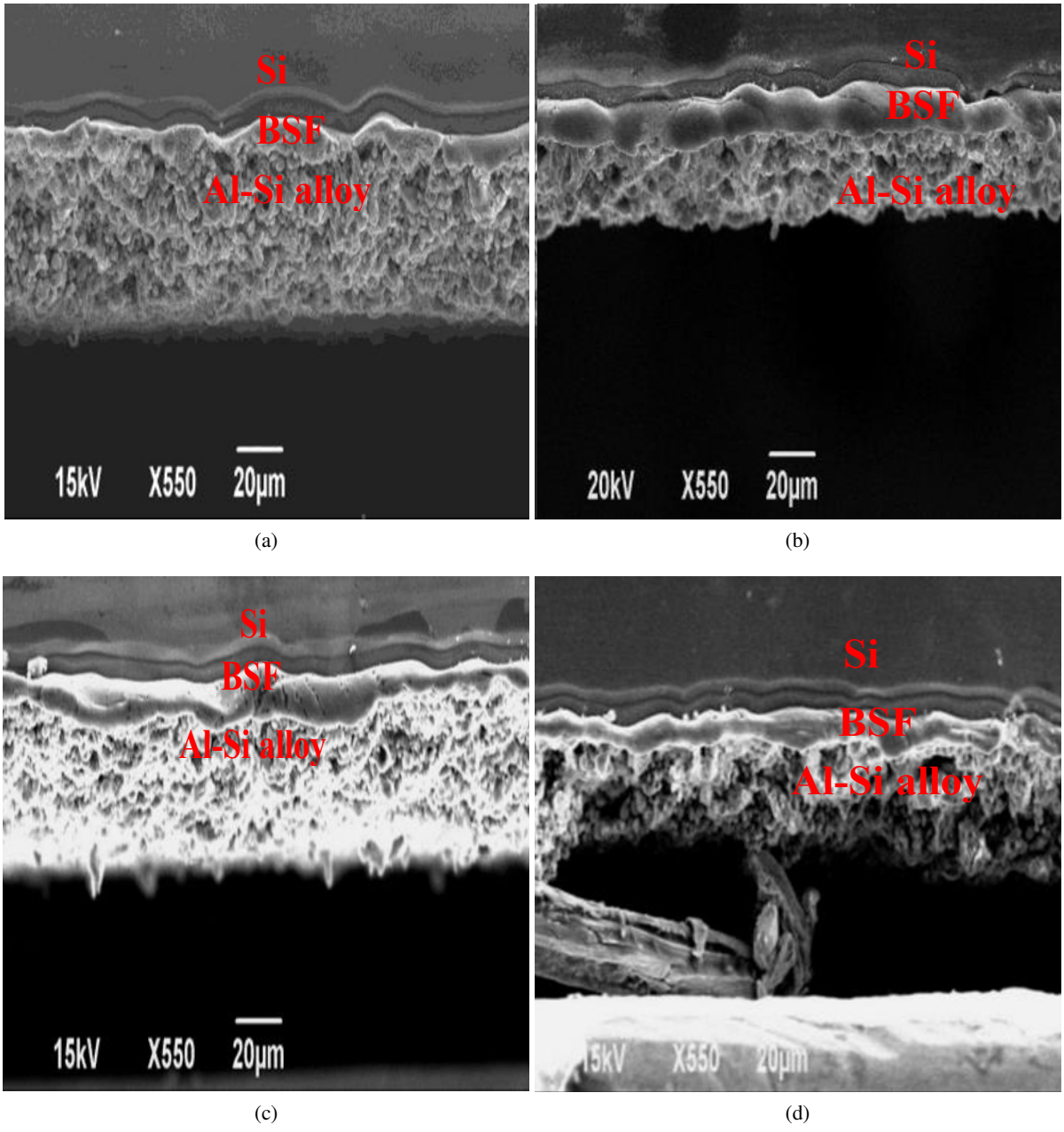


Fig. 8. SEM comparison of cross-section of the BSF topology and Al–Si alloy layer of (a) ED; (b) ED3; (c) ED6; (d) ED9.

Table 5. Device characteristics for the samples with different etching depths.

Item	V_{oc} (V)	I_{sc} (A)	Rs (mohm)	R_{sh} (Ω)	FF (%)	Ncell (%)	Irev (A)
ED0	0.634	9.04	2.74	100.86	78.33	18.44	0.57
ED3	0.635	9.04	2.55	103.13	78.55	18.54	0.45
ED6	0.638	9.13	2.61	106.41	78.67	18.82	0.38
ED9	0.637	9.06	2.53	102.54	78.73	18.68	0.49

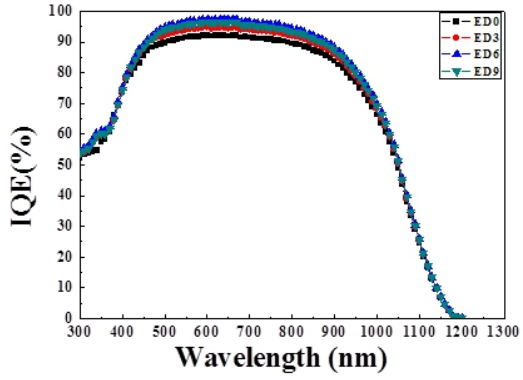


Fig. 9. The internal quantum efficiency (IQE) for four different etching depths.

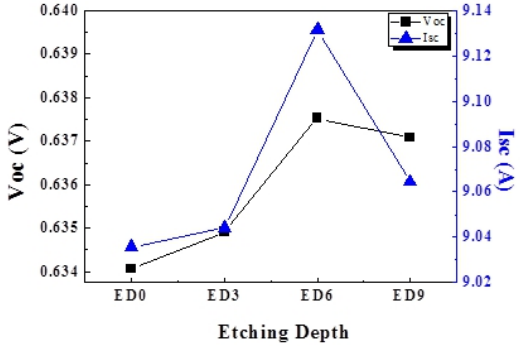


Fig. 10. V_{oc} and I_{sc} for four different etching depths.

performance at long wavelength. Finally, the studies carrried out with I – V tester indicated that the etching depth of 6 μm ± 0.1 μm resulted in the best V_{oc} and I_{sc} values. This was due to a higher carrier lifetime, resulting from better BSF and Al–Si layer.

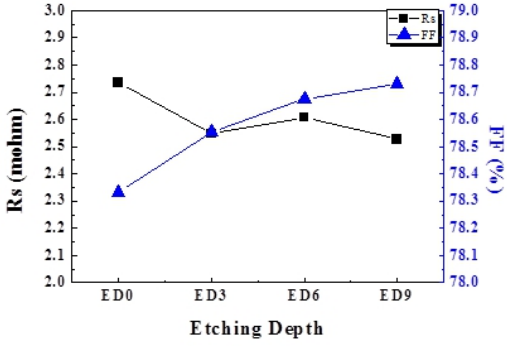


Fig. 11. R_S and FF for four different etching depths.

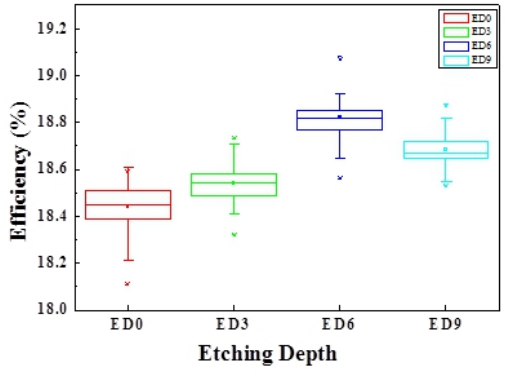


Fig. 12. Efficiency for four different etching depths.

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