LATVIAN JOURNAL OF PHYSICS AND TECHNICAL SCIENCES
2017, N 5

DOI: 10.1515/lpts-2017-0030

DESIGN CONSIDERATIONS FOR GAN-BASED MICROINVERTER FOR ENERGY STORAGE INTEGRATION INTO AC GRID

K. Kroics[1,2], J.Zakis[2], A. Suzdalenko[2], O. Husev[2]

[1]Institute of Physical Energetics
11 Krivu Str., Riga, LV-1006, LATVIA
e-mail: kaspars.kroics@gmail.com
[2]Riga Technical University
1 Kalku Str., Riga, LV-1658, LATVIA
e-mail: janis.zakis@rtu.lv

A full bridge converter with electrolytic capacitor on the dc bus is a widely used approach for a single phase interface for renewable energy source generation or energy storage integration in the utility grid. New wide bandgap devices enable higher switching frequency, higher efficiency and higher power density. In the paper, the authors introduce the challenges associated with an increase in switching frequency of a single phase inverter and implementation of wide bandgap GaN-based transistors instead of traditional Si-based transistors. The low gate threshold voltage of GaN transistor and unique reverse conduction behaviour require different driving circuit. The design of the driver circuit and other practical issues are analysed in the paper. The paper also presents some practical results. The research results can be useful to avoid mistakes by designing GaN-based power converters as these devices become increasingly interesting for commercial applications.

Keywords: *energy storage, GaN transistor, high frequency power converter, microinverter, wide bandgap devices*

1. INTRODUCTION

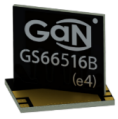
Wide bandgap (WBG) semiconductors such as Silicon Carbide (SiC) and Gallium Nitride (GaN) provide advantages over conventional Silicon (Si) power devices, as shown in Fig. 1. Higher breakdown field of a WBG semiconductor allows for devices to be optimised with thinner drift regions, resulting in power devices with lower specific on-resistance [1]. High electron mobility of GaN allows reducing on-resistance of transistors. This allows achieving high current capability with smaller die; therefore, input and output capacitances are lower than in the case of Si transistors (Table 1). Lower capacitance means that faster switching on and off is possible. Material properties of GaN semiconductors result in a device with lower

on-resistance and switching losses than a Si-based semiconductor with comparable voltage and current capabilities.

In high power density and high efficiency power electronics applications with power ratings around several kilowatts, wide bandgap semiconductors are progressively replacing Si MOSFETs [2] due to the improved switching performance and lower switching losses. The comparison of the main parameters of GaN transistor GS66516B and Si IPT65R033G7 is given in Table 1; the data are taken from the online electronic part catalogue (www.mouser.com). Both semiconductors have quite similar breakdown voltages and nominal current; therefore, other parameters should also be analysed in order to choose the transistor that is appropriate for implementation in the switching converter. Si-based transistors have significantly larger output capacitance and bad reverse recovery behaviour of the body diode. In contrast, GaN semiconductors feature much smaller output capacitance and do not suffer from reverse recovery, thus allowing one to achieve higher efficiency, especially, at high switching frequency and in hard switching topologies. The main reason why GaN transistors are not widely used is a significantly higher price and a lack of knowledge of engineers about the right schematic, layout design, EMI, passive component selection and calculation for higher frequencies, etc. to get benefit from using GaN transistors.

Table 1

Comparison of GaN and Si-Based Transistors

Symbol			**Value**	**Parameter**
	GS66516B	IPT65R033G7		transistor
V_{DS}	650	700	V	drain source voltage
$R_{DS(on)}$, T_J=25°C	25	29	mΩ	drain to source on resistance
$R_{DS(on)}$, T_J=150°C	65	72	mΩ	drain to source on resistance
$V_{GS(th)}$	1.3	3.5	V	gate to source voltage threshold
$V_{GS(max)}$	-10 … +7	-20 … +20	V	maximum gate to source voltage
C_{ISS}	500	5000	pF	input capacitance
Q_G	12.1	110	nC	total gate charge
Q_{GD}	3.4	35	nC	gate to drain charge
Q_{GS}	4.4	27	nC	gate to source charge
Q_{RR}	0	9	µC	reverse recovery charge
	40	13	€	price

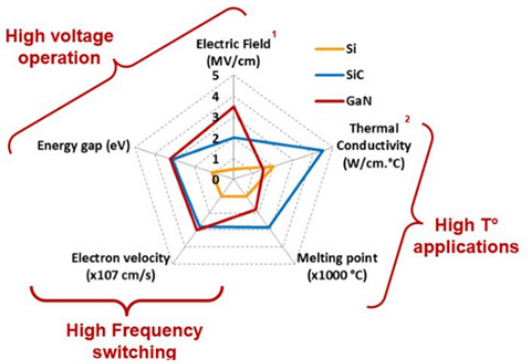


Fig. 1. Comparison of different types of transistor materials [3].

2. GATE DRIVER DESIGN

As can be seen in Table 1, GaN transistors typically come with much lower gate charge Q_G compared to similarly rated Si MOSFETs. Therefore, GaN semiconductors are a promising way to increase the switching frequency without suffering high additional power losses. The gate control of GaN transistors significantly differs from typical silicon Si MOSFETs. One of the main differences in terms of gate control is the gate threshold voltage $V_{GS(th)}$, the gate plateau and the maximum gate voltage $V_{GS(max)}$. As can be seen in Table 1, the maximum gate voltage V_{GS} is much lower than in Si MOSFETs, but anyway most GaN FETs are not fully turned on until V_{GS} reaches about 4 V [4]. To turn off the GaN transistor, the gate voltage must be kept below the minimum gate threshold voltage, which is 1.3 V in this case. This can be a challenge in topologies where the GaN semiconductor drain is exposed to a high dv/dt or the GaN transistor can be switched on from the EMI voltage spikes on the gate.

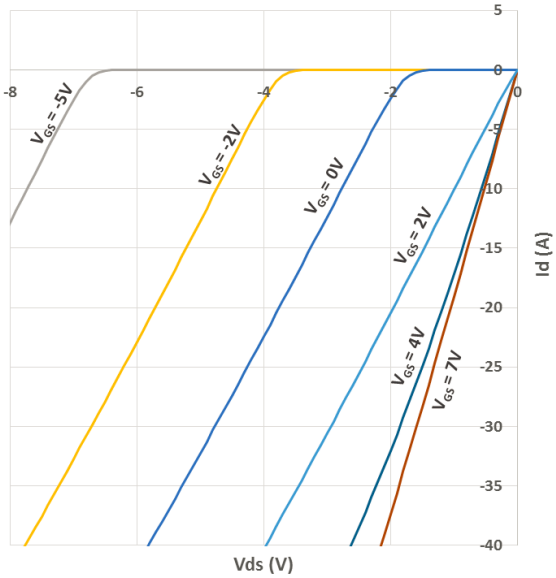


Fig. 2. GaN transistor GS66508P reverse bias characteristics [5].

To increase driver circuit stability against EMI and to increase dv/dt immunity, negative V_{GS} can be applied when the transistor is in off state. The enhancement-mode GaN transistors have specific behaviour: they do not have internal body diode but when the gate is turned off and drain is negative with respect to source, the GaN transistor conducts current from source to drain. The reverse bias characteristics of GaN transistor can be seen in Fig. 2. Applying a negative gate voltage to the transistor increases the voltage drop between source and drain during dead-time conduction. This voltage drop decreases efficiency of the converter; therefore, large negative voltage is not desirable. Even with precise dead-timing, the large voltage drop from drain to source still results in a significant variation of the bootstrap voltage [4]; therefore, bootstrap voltage source for driver is not preferable in this case.

Larger forward voltage drop of GaN transistors compared to MOSFETs during dead-time conduction produces additional power losses. Manufacturers of GaN semiconductors advise short dead-timing control to improve efficiency or add external anti-parallel fast Schottky diode [6]. Loss measurements have been carried out for switching converter with a negative gate voltage of GaN transistors in [7], [8]. Usually, in the scientific papers a gate drive which keeps the device turned off by applying zero volt to the gate to reduce losses during dead time, but for high frequency switching converter such design cannot be suitable as the energy stored in the parasitic loop inductance and the dv/dt stress are high. In the present paper, an approach to use -3V negative gate voltage $V_{GS(off)}$ is demonstrated in order to increase reliability of the converter despite the fact that there will be additional power losses. As can be seen in Table 1, there are no reverse recovery losses during switching; therefore, the required dead time is short.

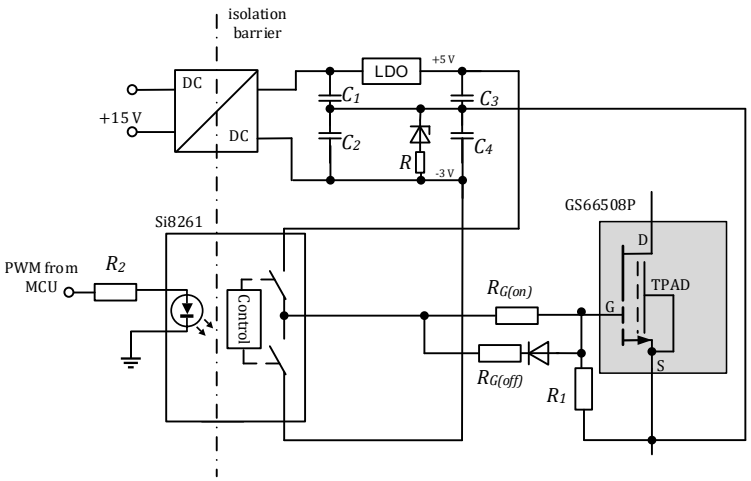


Fig. 3. The schematic of the developed driver.

There are only a few gate driver integrated circuits on the market that fit the requirements of GaN transistors. The LM5113 is a good solution for GaN transistors in applications below 100 V. Silicon Labs produces isolated gate driver integrated circuits that are suitable for GaN devices, compatible with voltages in the kV range. The digital isolation in these drivers is based on radio frequency; therefore, driver

has high common-mode transient immunity. Although common-mode transient immunity of driver is high, the printed circuit board should be designed very carefully to limit stray inductances and capacitances.

Figure 3 shows schematic of the driver circuit. As gate driver Si8261 integrated circuit is used, isolated DC-DC converter is used as power supply for both low side and high side driver circuits because in the case of non-isolated gate driver gate current flows through parasitic inductance L_S (Fig. 4) causing grounding problems. To protect gate from voltage spikes above threshold or maximum rating Zener diodes should be applied between G and S terminals, pull down resistor R_1 equal to 10 kΩ should be connected to prevent false turn on. Gate resistors with $R_{G(on)}$ = 10 Ω and $R_{G(off)}$ = 5 Ω are used for turn-on and turn-off processes. If zero voltage is used to turn off, the transistor diode with low voltage drop should be used to provide successful turn off of the transistor.

Gate drive impedance (R_G and L_G) is critical for turn off; therefore, the gate needs to be held down as strong as possible with minimum impedance. Miller effect is more prominent at 650V than 100V design due to higher dv/dt. The equivalent circuit during turn off of the transistor is shown in Fig. 4. To minimise parasitic gate inductance, the driver should be placed as close as possible to the transistor gate. As GaN transistors have extremely low Q_G and drive loss 0603 SMD resistors can be used and driver placed near the gate. Gate resistor allows determining switching speed. High value of $R_{G(on)}$ slows down switching and increases loss, whereas too small $R_{G(on)}$ leads to high dv/dt that can cause gate oscillations and additional losses. High dv/dt causes high common mode currents; therefore, it is important to minimise coupling capacitances of isolated power supply and use a gate driver with high common mode transient immunity.

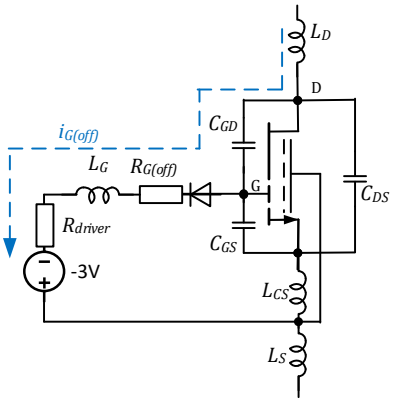


Fig. 4. The equivalent circuit of GaN transistor with a driver during turning off.

3. THE EXPERIMENTAL PROTOTYPE

In order to test the performance of 650 V GaN transistors, a full bridge inverter with LC filter has been designed (Fig. 5). The converter consists of four GS66508P GaN transistors. These transistors have package with low inductance of inner con-

nections, the device is bottom side cooled, so the thermal vias should be introduced into PCB and heat sink placed from the opposite side of the PCB; the proper cooling design is described in [9].

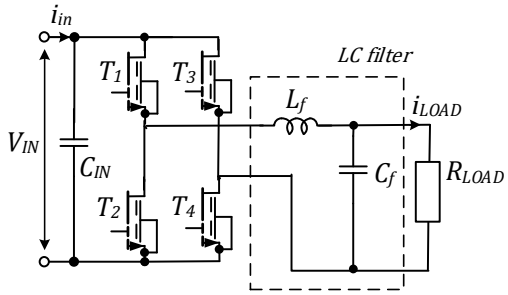


Fig. 5. AC single phase inverter with GaN transistors.

Figure 6 shows a photo of GaN-based inverter prototype; capacitive leg of the full bridge inverter consist of 1 mF electrolytic capacitor and additional ceramic capacitors close to the connection to the transistors. The PCB is intended to extend inverter functionality with a possibility to integrate renewable energy source and energy storage by using single stage quasi Z source topology that is analysed in [10]–[12]. The radiator is placed on the opposite side of the PCB. For the control of the inverter STM32F4 microcontroller was used. For measurement of the current the PCB was extended with a wire to be able to impose oscilloscope current clamp. This additional parasitic inductance introduced significant current ripple; therefore, this loop was removed.

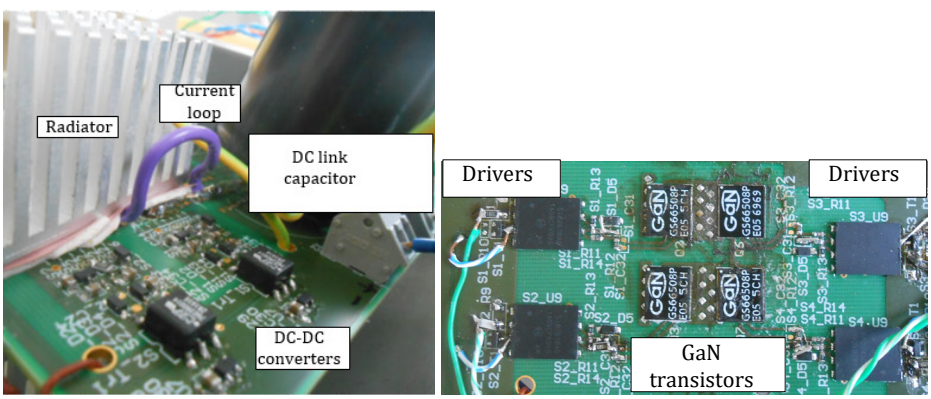


Fig. 6. Photo of the experimental prototype: top side and bottom side of the PCB.

The measurement of the signals of the high frequency GaN power converter is really challenging because any measurement has some impact on measurement results. Some measurement solutions are given in [13], one of the methods to avoid impact on the operation of the converter is to use the calorimetric measurement method. The performance of GaN transistor by using a calorimetric method is measured in [14], [15]. The simple temperature measurement (Fig. 7) via a thermal imaging camera was used to make a relative assessment of efficiency improvement or decrease by changing parameters.

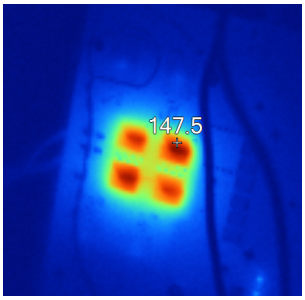


Fig. 7. Thermal image of GaN transistors (temperature in Fahrenheit).

4. THE EXPERIMENTAL RESULTS AND DISCUSSION

As can be seen in Fig. 2, in reverse conduction region the losses are significant; therefore all of the traditional modulation methods (unipolar, asymmetrical unipolar, bipolar) but with using of synchronous rectification and for efficiency improvement dead time should be as short as possible. For hard switching dead time set in PWM from a microcontroller should be larger than the worst-case propagation delay difference plus gate turn on and turn off delay difference that is typically equal to ± 5 ns [16] and varies with the value of R_G. Figure 8 shows driver input and output signals. Driver turn on delay is equal to 40 ns but turn off delay is equal to 30 ns and this corresponds to the information in Si8261 datasheet [17]. In [17] the worst-case propagation delay is given and it is equal to 25 ns. It means that for practical applications the dead time must be set larger than 30ns and plus some safety margin. In the scientific papers for 650 V GaN transistors dead time is usually in the range from 40 to 120 ns and this is mainly determined by the driver delay.

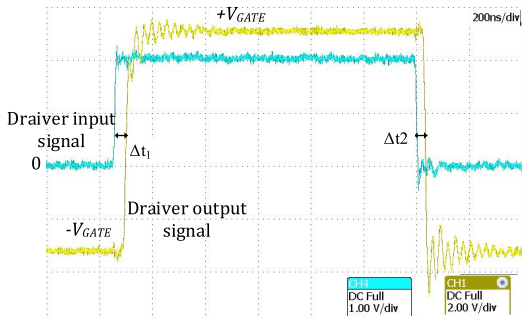


Fig. 8. Oscillogram of the driver input and output signals.

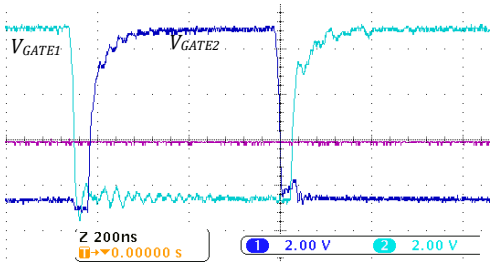


Fig. 9. Signals to the gate with inserted dead time, $R_{G(on)}$ =30 Ω.

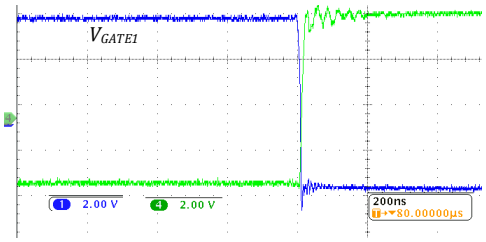


Fig. 10. Signals to the gate with small dead time, $R_{G(on)}$ =10 Ω.

As can be seen in Figs. 9 and 10, the gate resistor determines how fast gate capacitance is charged and how fast GaN transistor is switched on and off. As can be seen in Figs. 9 and 10, 30 Ω does not allow using all benefits from fast switching of GaN transistor and switching losses will be high. Too small gate resistor can lead to high dv/dt that causes EMI problems. In this case, gate resistance is selected equal to 10 Ω as compromise between both cases.

The dead time was changed and temperature of GaN transistors was measured to determine the most efficient dead time. Although these measurements give only a very approximate idea about losses, they can provide a comparative analysis. As the difference between driver turn off and turn on delays is equal to 10 ns (Fig. 8), the most efficient dead time generated from a microcontroller in temperature measurements is 0 ns since the dead time equal to 10 ns will be on the driver output (Fig. 10) due to driver delay and this dead time is enough for GaN transistor switching transitions. The impact of dead time on the efficiency of GaN transistors is also analysed in [4], [6], [7], [16]. In the literature, it is proposed to use 0 ns dead time for switching on and about 30 ns dead time for switching off, but the analysis is provided for driver with 0V turn off voltage. Different turn off and turn on dead time is more complicated to implement as in microcontrollers there is usually no such a choice to set different dead time. Optimal dead time also varies depending on current, duty cycle and other parameters; therefore, the selection of optimal dead time is a complicated task, especially, in inverter as the current varies during the time. In practical applications, the worst-case driver delay difference should be taken into account and dead time should be at least 30 ns.

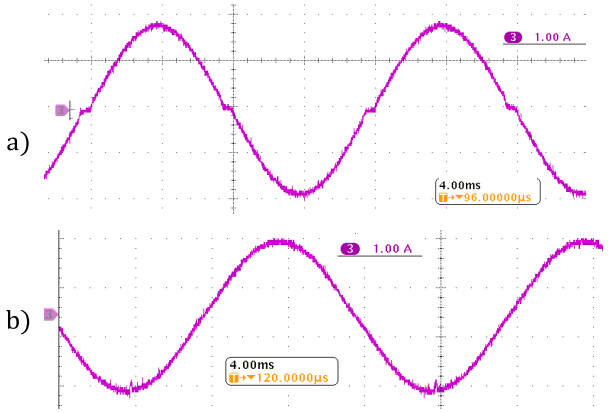


Fig. 11. Oscillogram of the load current a) with 170 kHz and small dead time; b) with 350 kHz and higher dead time.

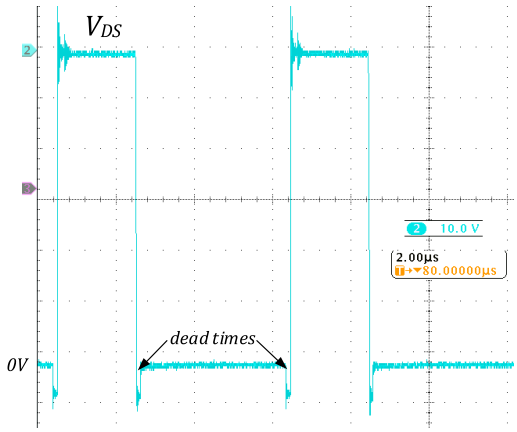


Fig. 12. Oscillogram of drain to source voltage.

Figure 11 shows waveforms of output current. The inverter is tested in the open loop condition without any feedback. The temperature measured during an increase in switching frequency shows a decrease in efficiency. The results of Little Box Challenge show that optimal frequency that reduces volume of passive components but does not significantly increase volume of heatsink is in the range from 80 to 200 kHz [18]. The dead time also influences waveform of the output sinusoidal signal as can be seen in Fig. 11b. If the working frequency is high, the high performance microcontroller or FPGA is needed to generate PWM with high resolution.

Figure 12 shows a waveform of drain-to-source voltage during the switching operation. Very high dv/dt can be achieved by using GaN transistors. In this case, 10 Ω gate resistor was used but this value could be reduced to increase dv/dt even more. The challenge is to design proper PCB to deal with such high dv/dt and di/dt. The first prototype had a few mistakes that did not allow increasing dv/dt and produced some EMI issues. Design of the converter with tight loop and low parasitic inductances is very important to get full benefit from GaN transistor applications.

5. CONCLUSIONS

The practical implementation of GaN transistors needs new knowledge, especially, in high frequency applications. Due to fast transients, decoupling of the voltage bus has to be done with minimal loop inductance; therefore, the current measurement through transistor can be challenging and calorimetric measurement methods can be applied. GaN transistor has no body diode but the channel reverse conduction is possible when gate voltage is below threshold voltage. Using 0V voltage to turn off is the simplest solution that limits power losses during dead time, but such gate voltage does not ensure sufficient safety against the false turn on and limits maximum dv/dt. Using negative voltage during turn off produces additional losses during dead time, the optimum of dead time is complicated to find and mainly minimum dead time is determined by the worst-case delay differences of driver circuit. The value of the gate resistor determines switching speed – a value less than 10 Ω allows increasing dv/dt, but losses in the gate capacitance increase and high dv/dt requires proper design of the converter.

ACKNOWLEDGEMENTS

The present research has been supported by the Latvian National Research Programme "LATENERGI" and the Latvian Council of Science (Grant 673/2014).

REFERENCES

1. Jones, E. A., Wang F. F., & Costinett, D. (2016). Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, *4*(3), 707–719.
2. Bortis, D., Knecht, O., Neumayr, D., & Kolar, J. W. (2016). Comprehensive evaluation of GaN GIT in low- and high-frequency bridge leg applications. In *IEEE 8th International Power Electronics and Motion Control Conference*, 22–25 May 2016 (pp. 21–30). Hefei, China.
3. Rise of the 3rd Generation Semiconductor Silicon Carbide Technology. [Online]. Available at http://www.iabrasive.com/articles/rise-of-the-3rd-generation-semiconductor-silicon-carbide-technology. [Accessed: 04-Aug-2017].
4. Roschatt, P. M., McMahon, R. A., & Pickering, S. (2015). Investigation of dead-time behaviour in GaN DC-DC buck converter with a negative gate voltage. In *9th International Conference on Power Electronics and ECCE Asia*, 1–5 June 2015 (pp. 1047–1052). Seoul, Korea.
5. Sørensen, C., Lindblad Fogsgaard, M., Christiansen, M. N., Kjeldal Graungaard, M., Nørgaard, J. B., Uhrenfeldt, C., & Trintis, I. (2015). Conduction, reverse conduction and switching characteristics of GaN E-HEMT. In *2015 IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 22 –25 June 2015 (pp. 1–7). Aachen, Germany: IEEE Press.
6. Strydom, J., & Reusch, D. (2013). Dead-time optimization for maximum efficiency. *Efficient Power Conversion (EPC) Whitepaper*.
7. Hoffmann, L., Gautier, C., Lefebvre, S. & Costa, F. (2014). Optimization of the Driver of GaN Power Transistors through Measurement of Their Thermal Behavior. *IEEE Transactions on Power Electronics*, *29*(5), 2359–2366.
8. Chub, A., Zdanowski, M., Blinov A., & Rabkowski, J. (2016). Evaluation of GaN HEMTs for high-voltage stage of isolated DC-DC converters. In *10th International Conference on Compatibility, Power Electronics and Power Engineering*, 29 June–1 July 2016 (pp. 375–379). IEEE.
9. PCB Thermal Design Guide for GaN Enhancement Mode Power Transistors. [Online]. Available at http://www.ecomal.com/fileadmin/Datenblaetter/GaN_Systems/App_Notes/GN005_App_Note-PCB_Thermal_Design_Guide_for_GaN_Enhancement_Mode_Power_Transistors.pdf [Accessed: 06-Aug-2017].
10. Matiushkin, O., Husev, O., Tytelmaier, K., Kroics, K., Veligorskyi, O., & Zakis, J. (2017). Comparative analysis of qZS-based bidirectional dc-dc converter for storage energy application. In *Technological Innovation for Smart Systems*, 3–5 May 2017 (pp. 409–418). Costa de Caparica, Portugal.
11. Kroics, K., Zakis, J., & Husev, O. (2017). Capacitance reduction using ripple suppression control of single phase energy stored quasi-z-source inverter. In *11th International Scientific and Practical Conference Environment. Technology. Resources, 15–17 June 2017* (pp. 154–158). Rezekne Academy of Technology.

12. Makovenko, E., Husev, O., Zakis, J., Roncero-Clemente, C., Romero-Cadaval, E., & Vinnikov, D. (2017). Passive power decoupling approach for three-level single-phase impedance source inverter based on resonant and PID controllers. In *11th IEEE International Conference on Compatibility, Power Electronics and Power Engineering*, 4-6 April 2017 (pp. 516–521). IEEE.
13. Lidow, A., Strydom, J., de Rooij, M., & Reusch, D. (2014). *GaN transistors for efficient power conversion.* New Jersey: Willey.
14. Rothmund, D., Bortis, D., & Kolar, J. W. (2016). Accurate transient calorimetric measurement of soft-switching losses of 10kV SiC MOSFETs. In *IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 27–30 June 2016 (pp. 1–10). IEEE.
15. Hoffmann, L., Gautier, C., Lefebvre, S., & Costa, F. (2013). Thermal measurement of losses of GaN power transistors for optimization of their drive. In *15th European Conference on Power Electronics and Applications (EPE)*, 2–6 September 2013 (pp. 1–8). Lille, France.
16. Han, D., & Sarlioglu, B. (2016). Deadtime effect on GaN-based synchronous boost converter and analytical model for optimal deadtime selection. *IEEE Transactions on Power Electronics*, *31*(1), 601–612.
17. Si826x: 5 kV LED Emulator Input, 4.0 A Isolated Gate Drivers . [Online]. Available at https://www.silabs.com/documents/public/data-sheets/Si826x.pdf [Accessed: 08-Aug-2017].
18. Zhao, C., Trento, B., Jiang, L., Jones, E. A., Liu, B., Zhang, Z., … Langley, R. (2016). Design and implementation of a GaN-based, 100-kHz, 102-W/in3 single-phase inverter. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, *4*(3), 824–840.

GAN TRANSISTORU PIELIETOŠANAS APSVĒRUMI MIKROINVERTORĀ ENERĢIJAS UZKRĀJĒJU INTEGRĒŠANAI MAIŅSTRĀVAS TĪKLĀ

K. Kroičs, J. Zaķis, A. Suzdaļenko, O. Husevs

Kopsavilkums

Šajā rakstā apskatīti izaicinājumi, kas jāņem vērā tradicionālos Si tranzistorus, aizvietojot ar GaN tranzistoriem un paaugstinot invertora darba frekvenci. Paaugstinot darba frekvenci, liela uzmanība ir jāpievērš spiestās plates dizainam, pēc iespējas samazinot parazītiskās induktivitātes un kapacitātes. Tranzistoru ieslēgšanās un izslēgšanās straujumu var mainīt izvēloties attiecīgu aizvara pretestību: pārāk liela pretestība izsauc palielinātus komutācijas zudumus, bet pārāk maza pretestība izsauc zudumus aizvara kapacitātes pārlādē, ka arī strauju sprieguma izmaiņu, kas izsauc paaugstinātus elektromagnētiskos traucējumus, kā arī pārspriegumus. Tranzistora draivera barošanai var tikt izmantots bipolārs vai unipolārs spriegums. Negatīva sprieguma izmantošana ļauj pasargāties pret tranzistora kļūdainu atvēršanos, taču tranzistora zudumi, strāvai plūstot pretējā virzienā, pieaug. Strāva plūst pretējā virzienā laikā, kurā augšējā un apakšējā pleca tranzistori ir neaktīvā stāvoklī. Šāda stāvokļa ieviešana ir nepieciešama, lai novērstu īslaicīgu īslēgumu, kas rastos tāpēc,

ka tranzistora aizvēršanās process nav momentāns. Šo neaktīvā stāvokļa laiku, galvenokārt, nosaka draivera mikroshēmas aiztures laiku izkliede, tāpēc efektivitātes uzlabošanai paralēli var tikt pieslēgta ātrdarbīga diode ar mazāku sprieguma kritumu nekā GaN tranzistoram. Strāvu un spriegumu mērīšana var ietekmēt pārveidotāja darba režīmu, tāpēc ir jāizvēlas atbilstošas mērīšanas metodes. Rakstā ir parādīts uz GaN tranzistoriem balstīta invertora prototips un dotas dažas invertora oscilogrammas.

07.09.2017.