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DIGITAL BASE BAND CONVERTER AS RADAR VLBI BACKEND

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A digital base band converter (DBBC) system has been developed by the Istituto di Radioastronomia (Noto, Italy) for increasing the sensitivity of European VLBI Network (EVN) by expanding the full observed bandwidth using numerical methods. The output data rate of this VLBI-backend is raised from 1 to 4 Gbps for each radiotelescope. All operations related to the signal processing (frequency translation, amplification, frequency generation with local oscillators, etc.) are transferred to the digital domain, which allows – in addition to well-known advantages coming from digital technologies – achieving better repeatability, precision, simplicity, etc. The maximum input band of DBBC system is 3.5 GHz, and the instantaneous bandwidth is up to 1 GHz for each radio frequency/intermediate frequency (RF/IF) out of the eight possible. This backend is a highly powerful platform for other radioastronomy applications, and a number of additional so-called personalities have been developed and used. This includes PFB (polyphase filter bank) receivers and Spectra for high resolution spectroscopy. An additional new development with the same aim – to use the DBBC system as a multi-purpose backend – is related to the bi-static radar observations including Radar VLBI. In such observations it is possible to study the population of space debris, with detection of even centimetre class fragments. A powerful transmitter is used to illuminate the sky region to be analyzed, and the echoes coming from known or unknown objects are reflected to one or more ground-based telescopes thus producing a single-dish or interferometric detection. The DBBC Radar VLBI personality is able to realize a high-resolution spectrum analysis, maintaining in the central area the echo signal at the expected frequency including the Doppler shift of frequency. For extremely weak signals a very large integration time is needed, so for this personality different input parameters are provided. The real-time information can then allow exploring easily the desired range of search for unknown or not fully determined orbit objects. These features make Radar VLBI personality most useful in the space debris measurements.

Key words: *VLBI; digital base band converter; data acquisition system*

1. INTRODUCTION

The Digital Base Band Converter (DBBC) is a project developed in the last decade inside the EVN community for the generic modular radioastronomical data acquisition architecture. In the framework of this project, the general method and a

class of boards, firmware and software have been produced, giving the possibility to build a general-purpose backend system for VLBI or single-dish observational activities. Such approach suggests the realization of a digital radio system which would include receivers with conversion not realized with analog techniques, still maintaining only amplification stages in the analog domain in order to satisfy the requirements for an analog-to-digital conversion unit [1].

The current DBBC version (DBBC2, presented in Fig. 1), with the maximum instantaneous bandwidth of 0.512–1.024 GHz and the maximum input frequency around 3.5 GHz, allows this concept to be applied up to the decimetric frequency bands and processing in the digital domain the intermediate frequency (IF) signal of a radiotelescope in the centimetre and millimetre observations. The ongoing Version 3 of DBBC project is expected to extend the direct digital radio system concept to a maximum input frequency up to ~ 16 GHz.

We will shortly describe here the DBBC architecture and the applications already developed in the DBBC project: a Direct Digital Conversion (DDC) VLBI terminal, a VLBI Polyphase Digital Filter Bank (PFB), and a Multiband Scanning Spectrometer (SPECTRA). In particular, we will point out the dedicated applications of the Radar VLBI observing capability [2].

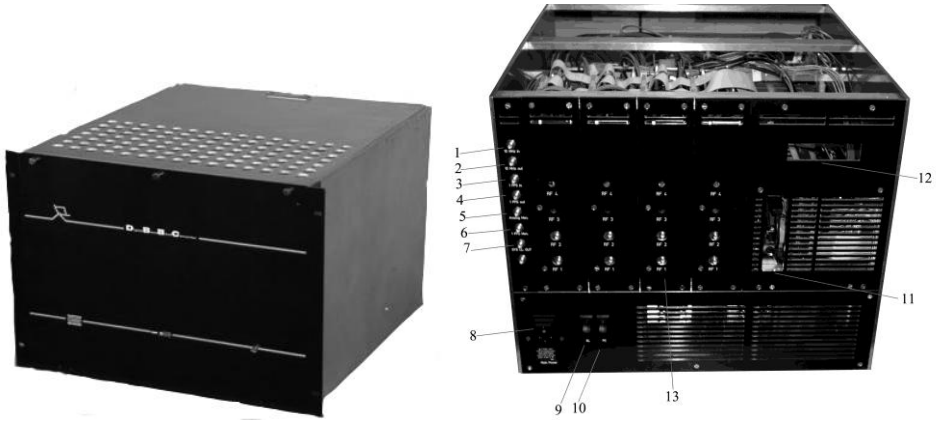

Fig. 1. DBBC2: front view (left), rear view (right). Connection interfaces: *1* – 10 MHz input; *2* – 10 MHZ output; *3* – 1PPS input; *4* – 1PPS output; *5* – analog monitor; *6* – 1PPS monitor; *7* – 80 Hz constant calibration; *8* – main power switch; *9* – electronics power switch; *10* – PC power switch; *11* – PS/2 for mouse and keyboard, LAN, monitor connection; *12* – VSI-H interface; *13* – RF/IF inputs.

2. DBBC ARCHITECTURE

The DBBC comprises a base box containing power supply, control computer, clock distribution and JTAG (Joint Test Action Group, standard IEEE 1149.1) interface (Fig. 2), and a stack of small modular boards that can be composed according to user needs (Fig. 3, centre). The first and the last modules in the system (FILA boards, Fig. 3, left) provide the control signal distribution, digital-to-analog conversion (DAC) for monitoring, and the electric interface to the standard VSI bus to the VLBI data recorder. An optional FILA10G board (Fig. 3, right) provides two XFP optical transceiver cages for 10G Ethernet.

2.1. Data processing pipeline

Between two FILA boards up to eight ADC boards and up to eight CORE2 (processing) boards can be stacked (in almost any order). The ADC modules contain a single high-speed ADC, while the CORE modules – a single field programmable gate array (FPGA). The modules can be upgraded without changing the rest of the system. The current version uses a 2 GS/s ADC for the ADC2 module, and a Virtex5 XC5VLX220 FPGA for the CORE2 processing module.

Each ADC board receives its input from an analog conditioning module. The module (directly controlled by the control processor) contains basically a set of filters for selecting one of its possible Nyquist sampling bands, an isolation amplifier and a programmable attenuator.

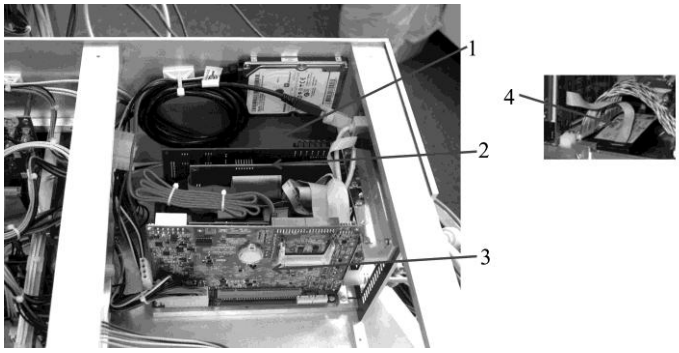

Fig. 2. (top right) PS set: *1* - ADLink PCI9111HR – communication with conditioning modules for IF total power measurement, automatic gain control, register control, etc; *2* - ADLink PCI7200 – communication with a 32-bit bus for CORE2 register setting, total power measurement, state statistics, etc; *3* - Adventech PCI-7030 – half-size PCI motherboard (based on Intel Atom) in PCI backplane; *4* - Xilinx programmer – FPGA device configuration through USB – JTAG interface.

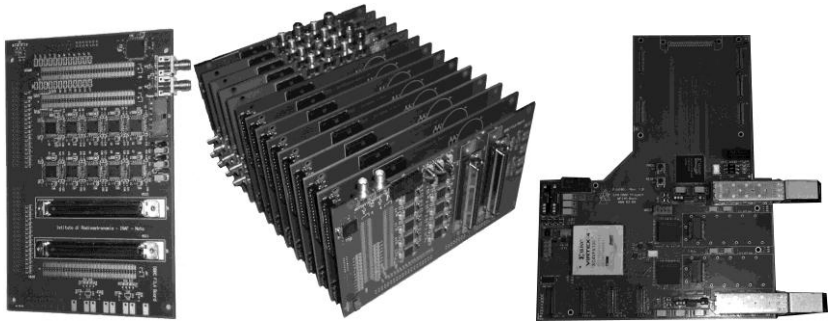

Fig. 3. *Left:* Fila Board – first and last board in the stack. First board includes communication interface, JTAG programming channel and 1PPS input. Last board includes 2 VSI interfaces, DA converter, 1PPS monitor output and 80 Hz output for continuous noise calibration. *Centre:* DBBC2 module stack ADC, CORE2 and Fila Boards. *Right:* optional Fila10G board providing two XFP optical transceiver cages for 10G Ethernet.

The modules are interconnected using stackable surface-mount differential connectors. Signals enter from one side of the board, are regenerated inside the FPGA, and exit on the other side of the board. Three data buses are used:

- High Speed Input (HSI) bus: ADC-generated, contains unprocessed data samples. It is structured as 8 LVDS buses at a sample rate of 512 MS/s, and

may be used for two data streams at 2 GS/s or up to four at 1 GS/s. A clock at 512 MHz is associated with each data stream.

- High Speed Output (HSO) bus: generated by CORE boards, with each board passing on the signals generated by the previous boards. It is a single differential 64-bit wide bus, with the maximum data rate of 128 Mb/s. It maps directly to the VSI VLBI bus, and contains auxiliary clock, data valid and strobe signals.
- Control, Command and Monitor (CCM) bus: a low-speed bus containing various signals used for the system control. A bus of the type – a 32 bit bidirectional bus with associated strobe signal is generated by a parallel interface in the control computer, and is used to address, read and write generic registers inside the CORE modules.

The JTAG interface is employed to program the FPGAs. A 12 bit bus is used to send test and debug signals (e.g. partially processed signals inside the FPGAs) to a DAC monitor in the last FILA.

A typical minimum configuration includes one ADC and one CORE module, with the CORE hosting one of the applications described below. For example, it can implement a mini-VLBI terminal, with up to four equivalent broadband converters. The maximum configuration includes eight units, each composed of eight ADC boards followed by a CORE2 board each. It can implement 32 BBC, with up to four input signals, or a multichannel wideband spectrometer with eight 1GHz input signals. This version is named VLBI2010 as it supports the latest VLBI geodetic mode (Fig. 4).

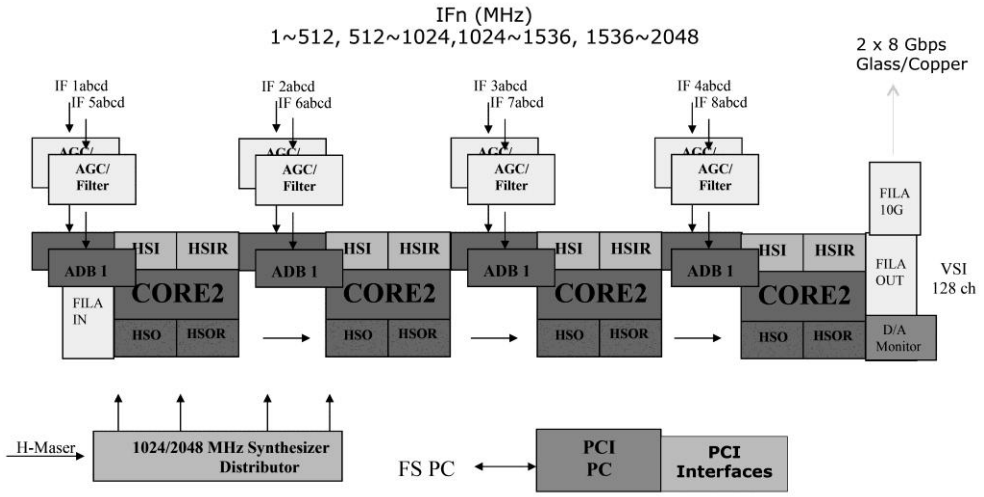

Fig. 4. DBBC2010 schematic architecture with latest VLBI geodetic mode support, includes 8 IF units with bandwidth 512 MHz each. Maximum output data rate using 2 optical transceivers is 16 Gbps.

The data flow is quite straightforward and widely described in the VLBI literature [3–5]: IFs from the receiver are conditioned in the analog domain in order to set the proper bandwidth and amplitude levels before to be converted in the digital domain by the ADB1 boards. Such digital representation is transferred to the Core2 processing boards containing an FPGA where the required operations are numerically performed. This can be the functionality to realize a single- or

multiple-channel down-converter system, or any other instrument providing the proper firmware and capability of the hardware used.

The output from the Core2 boards is the converted/processed data to be recorded or transferred through the network at the final processing point like a VLBI correlator.

2.2. General control structure

The control processor is a standard industrial PC (with Windows operating system). The processor uses a standard Xilinx JTAG interface to program the CORE2 stack, and a commercial 32 bit parallel interface to control both the conditioning modules and any logic embedded in the CORE2 FPGAs.

To control the embedded logic, a generic framework has been developed. Basically, the application in FPGA is controlled by a number of 16 bit write registers (up to 1024 per FPGA); its status (or the observation result) is read using a set of 32 bit read registers [6].

The 32 bit output of the parallel interface is split into a 16 bit address used to identify the register, and 16 bit of data. The read bus is meant (exclusively) for the data. The address is divided into a 5 bit portion identifying the module (often comparing it to a physical address set by switch), a bit discriminating between the read and the write address space, and a 10 bit address space per FPGA. A standard addressing scheme is consistently employed in the system, with some dedicated registers reserved for commonly applied functions such as direct digital syntheser (DDS) reset.

The absolute timing is maintained using an external peak-per-second signal, from which an internal PPS is generated. As signals in the data and HSO buses are regenerated inside each module, a propagation delay is present across different modules in the stack. This is accounted for by adding a programmable offset to the internal PPS signal.

A set of standard modules for the bus interface, clock generation, and control interface are provided as a common system library.

3. DDC: DIGITAL BROADBAND CONVERTER

This application is conceived as a plug-in direct substitution for an analog VLBI terminal. It is composed of an array of individual broad-band converters (BBCs), with the same functionality of the existing VLBI analog BBC modules.

Each BBC is basically a sideband separating radio receiver. It accepts a wideband signal and selects two bands of programmable width at two sides of the tunable centre frequency (Fig. 5). The two output signals are real-valued, with one of them (lower sideband) having a reversed frequency scale.

The centre frequency is selected using a local oscillator. The LO signal is generated by a DDS; this latter has a natural frequency step of 1/2n the clock frequency in order to have the system also programmed at multiple of integer frequencies, e.g. at a multiple of 10 kHz as used in VLBI observations.

The bandwidth of input signal is 512 MHz or 1024 MHz, and its sample rate – 1024 MHz or 2048 MHz, respectively (derived from atomic standard). A digital

SSB process is realized in order to down-convert and to filter the tuned portion of band producing both USB and LSB side bands. The converted signals are scaled by a programmable scale factor, and quantized to a 2 bit representation by comparing the scaled signal to a set of fixed thresholds. A total power detector is used both to correctly set the scale factor for proper quantization and to compute the total power in the band for VLBI calibration. Two additional total power integrators are available for synchronous detection of the power calibration mark. Additional synchronous total power capability is available for the 80 Hz noise diode modulated receivers.

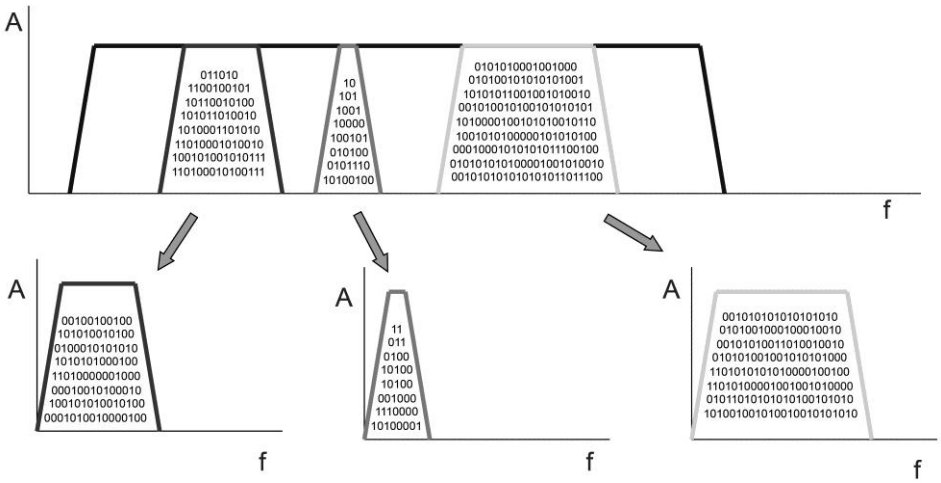

Fig. 5. Digital down conversion to the base band of independent channels.
The bandwidth of input signal is 512 MHz or 1024 MHz.

4. POLYPHASE FILTERBANK

A common problem in radio applications is the need to divide a larger bandwidth into smaller contiguous frequency channels in order to analyze, transmit, or store the signal using slower equipments. When continuous frequency coverage is less important than the total observed bandwidth (like in continuum VLBI), a commonly used architecture is the polyphase filterbank (PFB).

This appliance implements a 16-channel PFB in a single CORE2 for VLBI applications. It decomposes the input signal with 512 MHz bandwidth into 15 parallel VLBI data streams, with a bandwidth of 32 MHz each (Fig. 6). This PFB contains a 32-channel complex polyphase FFT (with only positive frequencies used) followed by conversion to the real output stage.

Both the input and output signals are represented as real-data streams at a Nyquist data rate. Each output channel has the data rate of 64 MHz, and the central frequency at a multiple of 32 MHz.

Channel 0 has a 16 MHz bandwidth, with the upper 16 MHz of the input band discarded.

The design is intended to optimize the polyphase transform operation, merging the final complex-to-real transform with the last stage of the decimation-in-time FFT [7, 8].

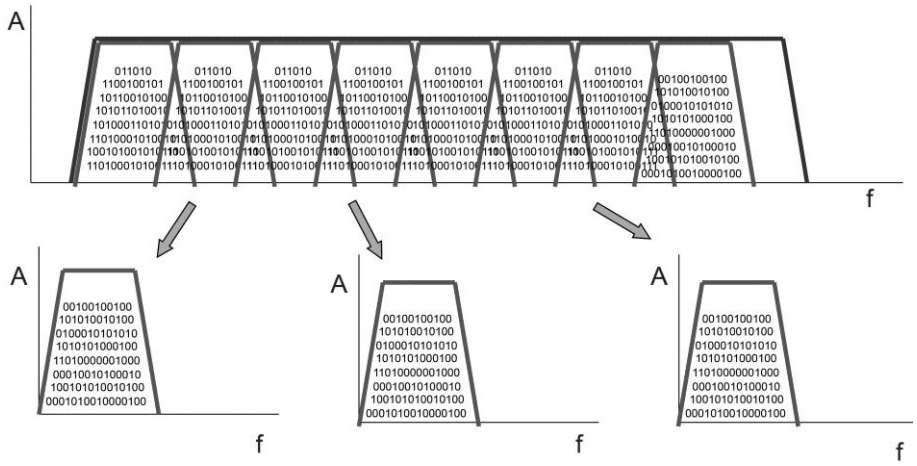

Fig. 6. Polyphase filter bank conversion to base band. PFB decomposes the input signal with 512 MHz bandwidth into 15 parallel VLBI data streams with a bandwidth of 32 MHz each.

5. SPECTRA: SCANNING SPECTROMETER

The gap between output channels in a conventional PFB is not acceptable for spectroscopic observations. Therefore, for wideband spectroscopy a filterbank with overlapping bands is often used. In this approach, the output data rate of filter is doubled with respect to the minimum required by the Nyquist criterion, i.e. the channel spacing is equal to half the data rate, with a 50% overlap between adjacent channels. This allows the channel filters to be designed with wide transition regions, and each portion of the input band is covered by at least one output channel.

The overlapping causes however a waste of resources, and various techniques have been used to delete the overlapped regions from subsequent processing. In this design, we implemented a spectrometer comprising a two-stage PFB in which a second FFT is performed in parallel over couples of overlapping regions from the first FFT. The design automatically deletes the unused portions of each region, providing a seamless uniform channelization of the input band. The design has been implemented as part of a scanning FFT spectrometer used for RFI monitoring at the Italian VLBI radiotelescopes. It employs a single CORE2 module, but can be extended to the whole bandwidth using a second CORE2 in cascade. After the analog-to-digital conversion (ADC) the input signal samples are parallelized in a deserializer. The time multiplexing factor can be either 8 or 16, for the bandwidth of 0.512 and 1.024 GHz, respectively.

The digital parallel data are sent to a parallel polyphase filter bank (PDFB1), which divides the input band-width into 8 or 16 overlapping regions, with a bandwidth of 128 MHz each and a spacing of 64 MHz. These signals are then analyzed by a serial polyphase filter bank (PDFB2) array. The PDFB2 outputs are squared and the total power integrated in time, with the input signal power spectrum obtained. Each PDFB2 block computes simultaneously the spectrum of two PDFB1 channels, and integrates only the central portion of each channel.

The first filterbank (PDFB1) uses a parallel decimation-in-time (DIT) FFT architecture, with a FFT length of twice the multiplexing factor (16 points for the 8-channel version) and an output data rate for each channel of 128 MHz. In this

way, a 50% overlapping between the adjacent FFT complex outputs is obtained. Only the central 64 MHz (±32 MHz) of each region is used, and thus only this part of the prototype filter needs to be flat, with the stop band beginning at 150% of the Nyquist frequency for the output signal. This drastically reduces the number of taps in the Finite Impulse Response (FIR) filter architecture: for the 16 channel version a 64-tap FIR filter has been used, with a stopband attenuation of 45 dB obtained [9, 10].

The 16-point FFT block is the same as in the previous design but optimized for a real-value input signal, and implementing only the butterfly stages required for the positive frequency output channels.

Outputs of the first PDFB are sent in couples to a serial PDFB array. Each PDFB2 block consists of a serial polyphase filter which provides the correct insulation between spectral channels for the next serial decimation-in-frequency (DIF) FFT engine. The FFT length is 1024 points, of which the central 512 are used for a total of 4096 spectral points over the input 512 MHz band. The polyphase low-pass filter has 4096 taps; it has been designed by extending in frequency a smaller FIR filter (computed using the Remez algorithm). It has a passband slightly larger than the channel separation, and the out-of-band rejection around 90 dB.

The standard FFT algorithm is able to produce simultaneous spectra from two independent signals, because the N-point spectrum of a single signal is calculated in N/2 cycles. The FFT engine provides the two spectra sequentially, with two spectral outputs computed at each clock cycle.

In a conventional PFB the spectra of all channels are entirely processed, and at the end of integration good portions are extracted and stitched together. This wastes a considerable amount of resources, especially memory for information that is successively discarded. We exploit the parallelism of the FFT engine to discard the unused portions of the spectra as early as possible, thus saving memory and logic resources in the following data processing (correlation, integration, etc.).

The DIF FFT algorithm produces spectral points in a bit-reversal order. The two spectral samples computed by FFT engine at each clock cycle are always spaced exactly by halfband, and therefore we have always one sample in the central (good) portion of the spectrum while the other – in the external transition band. Due to the bit-reversal order, at each clock cycle the good samples are presented alternately on the two outputs. Therefore, the selection of good portions of the spectra is performed by processing alternately on each cycle one of the two outputs of FFT engine and discarding the other. Using a single CORE2 board, only two PFB2 blocks can be instantiated, for a maximum instantaneous bandwidth of 256 MHz. Larger spectra can be synthesized either in time, by analyzing in turn different channels of the first filterbank or by using a second CORE board.

6. DBBC IMPLEMENTATION FOR RADAR VLBI

A dedicated implementation for Radar VLBI experiment is under development in order to take into account particular goals to be achieved for this type of observations. The typical signal to detect is a single frequency tone embedded in the noise resulting as echo from a powerful signal sent from a radiotelescope on the Earth reflected by the object under study and so sent back as fractional power again to the Earth, where a number of radiotelescopes could be able to detect it.

This detection is typically realized performing a post-processing data analysis in the recorded received data sets, integrating for relatively long periods the data in the echo expected frequency range. Indeed, the returning signal is affected by Doppler's shift variable in time, with parameters depending mainly on the source frequency and on the position and velocity of the object with respect to the receiving point on the Earth. If VLBI detection is needed, a further correlation is performed between all couples of the detected signals; therefore, this requires a dedicated data processing in the correlation phase.

In order to significantly simplify the detection process for such typically weak signals, two elements are introduced into the DBBC structure (i.e. into its firmware and software). Such an approach makes it possible to produce two additional functionalities to the normal capability as described above.

The two main functionalities added are:

- EFD – echo expected frequency "following" and detection in the observed sub-band;
- FSS – VLBI fringes station stop.

6.1. EFD: Echo Following and Detection

The EFD functionality serves the following purposes:

- tuning frequency finely upgraded with a user external software model;
- frequency variation parameters pre-calculated and downloaded each second to the firmware;
- final tuning frequency calculated by the firmware (linear and quadratic increment in time) and applied to the tuner;
- following timing clock (frequency recalculation and upgrade) – 128 MHz;
- arbitrary frequency tone amplitude and phase detection.

As a result, if the predicted parameters are correct the tone is kept at a known down-converted frequency (e.g. band centre) so as to permit an easier further integration or correlation.

In order to directly detect a tone with the DBBC it is possible to set a DDC-SPECTRA configuration on two CORE2 in cascade. The first CORE2 would be in charge to perform the down conversion at the desired and expected frequency, while the second CORE2 would perform the high-frequency resolution spectrum analysis, concentrating most of the resources on the selected range. Due to the frequency stopped tone, the time integration can be easily realized also for very long time, making it possible to detect the extremely weak signals.

6.2. FSS: Fringes Station Stopped

The VLBI cross-correlation process for orbiting objects is greatly complicated by the near-field requirements. Today, the software-based correlators permit a better control over such type of process, but it is still a great problem. In order to simplify the correlation, a VLBI fringe stop (FSS) process is implemented so as to keep the received signal at the expected frequency independent of the receiving position on the Earth. Such functionality requires insertion at the observing phase of all the parameters that are normally used in the correlation process, in order to take into account the Earth rotation, source position, and all other secondary

parameters, so as to calculate and down-convert the tone to a fringe stopped frequency.

If the same approach is adopted at other observing radiotelescopes, a full set of fringe stopped echo is available, so that any VLBI detection is reduced to single zero baseline correlations. This kind of process can be easily realized at any station with simple software tools.

Therefore, the FSS functionality can be described as follows.

- Added to the DBBC software control:
  - observing station geometric parameters;
  - time epoch;
  - observed source coordinates;
  - sky frequency.
- Final tuning frequency calculated by the firmware and applied to the tuner in order to obtain stopped or quasi-stopped fringes.
- Zero baseline correlation software support.

The implementation of two functionalities (EFC and FSS) is underway, and these are expected to be available for real observation tests in the spring of 2013.

7. CONCLUSIONS

From the results obtained in our research, the following conclusions can be drawn.

1. The Digital Base Band Converter (DBBC) can successfully be used in various VLBI applications like European VLBI observations, VLBI geodesy and space debris detection using radar VLBI.

2. DBBC2 allows for easy realization of the space debris radar VLBI observations and detection of the extremely weak signals. Moreover, this system will greatly simplify the subsequent data correlation, which can be done at any station with simple software tools.

3. The ongoing version 3 of the DBBC project is expected to extend the direct digital radio system concept to a maximum input frequency of up to ~ 16 GHz. The version meets the VLBI2010 requirements.

ACKNOWLEDGMENTS

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DBBC KĀ CIPAROŠANAS SISTĒMA RADARA VLBI NOVĒROJUMIEM

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K o p s a v i l k u m s

DBBC sistēma izstrādāta Noto Radioastronomijas institūtā. Sistēmas galvenais uzdevums – palielināt visa Eiropas VLBI tīkla jutību – realizēts, palielinot visas novērojamās joslas platumu un pielietojot ciparu signālu apstrādes metodes. Izejas datu plūsma palielināta no 1 līdz 4 Gbps katram radioteleskopam un visas operācijas, kas saistītas ar signālu apstrādi (frekvences pārveidošana, pastiprinājums, iekšējie ģeneratori, utt.), realizētas digitālā formā, kas ļauj iegūt nozīmīgus uzlabojumus atkārtojamībā, precizitātē, vienkāršībā, nemaz neminot vispārzināmās priekšrocības, ko nodrošina digitālo tehnoloģiju izmantošana. Maksimālā ieejas signāla frekvenču josla ir 3.5 GHz, un momentānais joslas platums ir līdz 1 GHz uz katru no astoņiem iespējamajiem RF/IF kanāliem. Šī datu reģistrācijas sistēma ir ļoti veiktspējīga platforma ne tikai EVN, bet arī citiem radioastronomijas pielietojumiem, un papildus tiek izstrādāta vesela virkne programmatūras pakotņu, kas vēl vairāk paplašina sistēmas funkcionalitāti. Tas ietver PFB (Polifāzes Filtru Banka) uztvērējus „Spectra", kas piemēroti augstas izšķirtspējas spektroskopijas vajadzībām. Papildus realizēts jaunas programmatūras risinājums, ar mērķi izmantot DBBC sistēmu kā daudzfunkcionālu datu ciparošanas iekārtu, kas izmantojama bistatiskiem radara novērojumiem, tai skaitā arī radara VLBI novērojumiem. Šāda veida novērojumos tiek pētīta kosmisko atlūzu populācija, nodrošinot iespēju detektēt pat centimetra izmēru objektus. Debess apgabala apstarošanai tiek izmantots jaudīgs raidītājs, un tiek analizēts atbalss signāls, kas atstarojas no zināmiem vai nezināmiem objektiem un tiek uztverts ar vienu vai vairākiem teleskopiem uz Zemes, tādējādi realizējot vienas antenas vai inter-

ferometrisku signāla detektēšanu. DBBC sistēma ar radara VLBI programmatūru spēj realizēt augstas izšķirtspējas spektra analīzi, saglabājot atbalss signālu ar sagaidāmo frekvenci centrālajā zonā un ieskaitot nepieciešamās Doplera frekvences nobīdes korekcijas. Tālāk, izmantojot dažādus ievadparametrus, iespējams pielietot ļoti ilgu integrācijas laiku ārkārtīgi vāju signālu detektēšanai. Izmantojot reālā laika informāciju, turpmāk ir iespējams viegli analizēt nepieciešamo apgabalu un detektēt nezināmus objektus vai objektus ar neprecīzi zināmiem orbītu parametriem. Rakstā izklāstītas paredzamās minētās programmatūras funkcijas un tās izmantošanas plāni pirmajos novērojumos.