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REDUCING THE PHASE-NOISE IN ΔΣ FRACTIONAL-N SYNTHEZIS – A SIMULINK MODEL

Emil TEODORU

"Nicolae Bălcescu" Land Forces Academy, Sibiu, Romania
eteodoru2002@yahoo.com

Abstract: *The resolution in fractional-N synthesis results as a fractional part of the reference frequency. This category of synthesizers permits a greater f_{ref} and a smaller N, a larger loop bandwidth, faster lock times and reduced output phase-noise. In ΔΣ fractional-N PLL's the main problem is the specific quantization noise. To reduce them many techniques are used. The paper presents a Simulink model of the influence of the requantisation in the phase-noise cancellation process.*

Keywords: frequency synthesis, ΔΣ modulator, phase-noise

1. ΔΣ modulators

ΔΣ modulators are circuits with many applications in electronic devices for audio domain, receivers for communication systems, sensor interface circuits, measurement systems. Analog-to-Digital circuits for high-resolution conversion include such solutions. Sampling rates much higher than the Nyquist rate are used and resolutions up to 18-20 bits can result so these architectures gained a large popularity.

A coarse quantizer included in the feedback loop of the ΔΣ modulator Simulink model injects the quantization noise so the output signal has important distortions. These spurious tones are present in a large discrete-time frequency domain. Based on the configuration of the modulator the inevitable quantization noise will be spread from and suppressed in a frequency band of interest.

The second order ΔΣ modulator (fig.1) consists of two discrete-time integrators, the quantizer and two feedback loops.

The output signal of this linear-time, invariant discrete-time system, is [1]:

$$y[n] = x[n-2] + e_{qm}[n] \quad (1)$$

where $e_{qm}[n]$ is the quantization error of the modulator:

$$e_{qm}[n] = e_q[n] - 2e_q[n-1] + e_q[n-2] \quad (2)$$

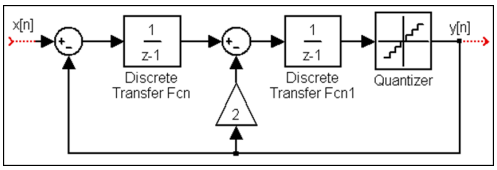

Figure 1: The 2nd order ΔΣ modulator Simulink model.

The sequence $e_q[n]$ must be of the nature of white noise by keeping the magnitude of the input sequence in the limits of ±3Δ (Δ is the quantization step size) and second, the noise in the input signal to be small, but necessary white.

The dynamic range DR of the modulator is defined [1]:

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$$DR = 20\log(M-3) + 50\log\left(\frac{f_s}{2f_{bw}}\right) - 11.1\ \text{dB} \quad (3)$$

where: M = number of the quantizer levels, f_s= the sampling frequency, f_{bw} the bandwidth of the low frequencies where the SNR is evaluated.
The spectrum of the signal to the 2nd order modulator output is in figure 2.

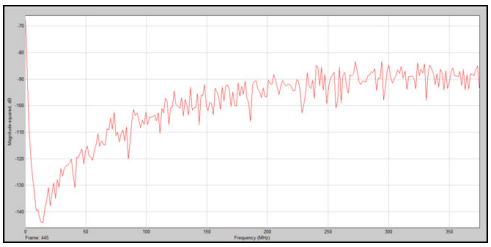

Figure 2: The spectrum of the 2nd order ΔΣ modulator in figure 1.

Other modulators structures realize better attenuation of the quantization error with a higher order loop and a single quantizer with more feedback loops. MASH (Multi-stAge noise SHapping) structures comprises multiple lower (second) order ΔΣ modulators to obtain an equivalent single higher-order ΔΣ modulator.

2. ΔΣ modulators in fractional-N frequency synthesizers

The well-known integer-N frequency synthesizer (Phase Locked Loop) is a structure that generates precise frequencies, but some inconvenient are present. For a high resolution small frequency steps are needed, that means higher divide factors N. Consecutively, the reference source noise will increase, because it is direct proportional with the N value.
When small reference frequencies are needed, that results in also small bandwidth. This is the permanent conflict in integer-N frequency synthesis: a good resolution (small f_{ref}) and a large bandwidth (= f_{ref}).
The best solution is to use the fractional-N frequency synthesis.
Now the output frequency f_{out} is a fractional multiple of the reference frequency f_{ref}:

$$f_{out} = (N + k/M)f_{ref} \quad (4)$$

with k, M integers, where M is the *fractional modulus* and k a integer between 0 and M.
Multiple advantages occur:

- the reference frequency can be higher than the output step between two adjacent frequencies;
- the output reference noise decreases;
- a great f_{ref} permits larger bandwidth and smaller lock times for equal bandwidth.

2.1. The fractional error

The classic fractional-N structure includes a accumulator and a dual-modulus N/(N+1) divider.
By the mechanism of operation in these structures a quantisation error is present, due to the difference between the reference frequency f_{ref} and f_{VCO}/N_a. This error is periodic, increases in the fractional cycle till the accumulator are full and the overflow reduces the phase error by 2π.
Another error, the *fractional spur*, occurs due to:

- the periodicity of changing N→(N+1)
- the abrupt change of the phase.

This spur is present at multiples of f_{ref}/M from the carrier. A lower bandwidth is necessary to reduce these spurs, but again this affect the need to a large bandwidth.
The good solution is to replace the periodic mechanism of generate the fractional modulus by a random manner of selection for the two values of the divider N and N+1.
This way a sequence must approximate a sampled sequence for random variables 1 and 0 with the probabilities of (M-k)/M and k/M.

2.2. The ΔΣ fractional-N frequency synthesizers

In this solution of frequency synthesizers a

randomisation in achieving the N and N+1 divide factors is implemented, so the periodicity of the fractional spur is broken and

A structure of a ΔΣ fractional-N frequency synthesizer is in figure 3.

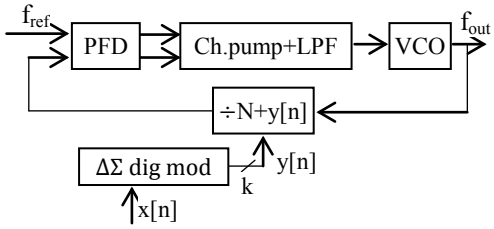

Figure 3: ΔΣ fractional-N synthesizer.

The ΔΣ modulator spread the noise from low to high frequencies based on the characteristic of the modulator depending of his order.

3. Simulink model for the compensation of the quantisation error

In [5] a method to compensate the phase error of a ΔΣ fractional-N frequency synthesizer is described.

To compensate the quantisation error a DAC inject in the loop filter every period of the reference a load of inverse sign (figure 4). Scaled compensation pulses of the compensation DAC will sum with the pulses corresponding to the error $e_Q[n]$. This process does not generate errors. The output of the sum reflects the effect of the compensation and is the output phase error. The pulse duration of the noise sequence and of the correction DAC and their durations satisfy the relation [5]:

$$I_{DAC}\, T_{DAC} = I_{CP}\, T^{*}_{OCT} \qquad (5)$$

The DAC pulse duration T_{DAC} must modify as function of T^{*}_{OCT}, and if this does not happen, a part of the quantisation load $Q_Q[n]$ remain uncompensated and will generate phase noise to the filter output.

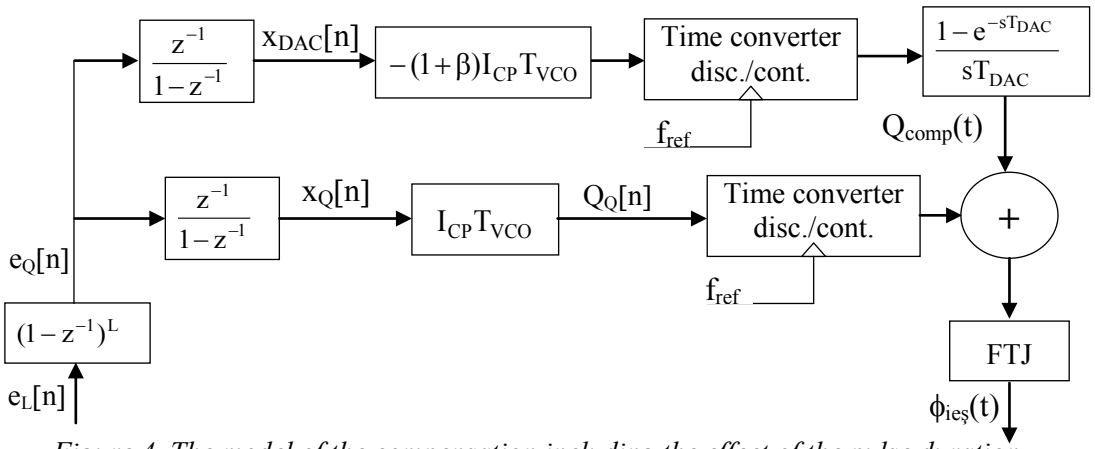

Figure 4. The model of the compensation including the effect of the pulse duration.

With the condition [5]:

$$T_{DAC} = M_{DAC} \cdot T_{OCT} \qquad (6)$$

where M_{DAC} is an integer, so when T_{OCT} change, there is a change also in T_{DAC} and the condition (5) is respected.

In the simulation:

- $f_{ref} = 10^5$ Hz
- $\beta = 0{,}1$

For T_{DAC}:

- the condition (6)
- the inequalities:

$$\Delta T_{DAC}/T_{DAC} < \beta \qquad (7)$$

$$\pi f_{critic}\, T_{DAC} \ll \beta \qquad (8)$$

where f_{critic} is the critically offset frequency where the noise phase conditions of a fractional-N synthesizer are hardest to be accomplished. We use the values:

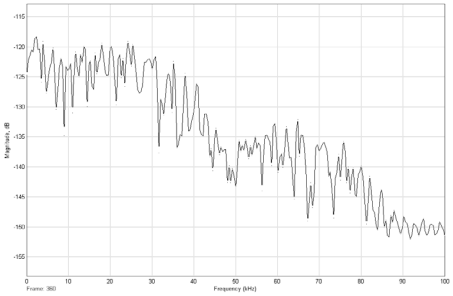

Figure 5. The uncompensated phase noise.

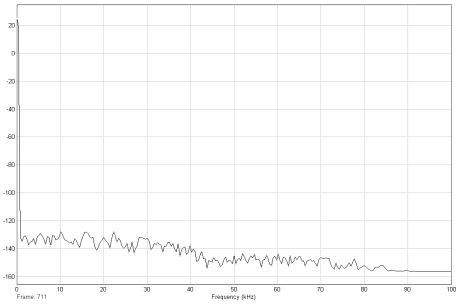

Figure 6. Compensation with $T_{DAC}=4T_{OCT.}$

$\Delta T_{DAC} = 40$ ps
$T_{OCT} \cong 400$ ps

$f_{critic} = 3$ MHz
and we have:

$M_{DAC} >> 1$ and $M_{DAC} << 26$

Spectral diagrams are obtained in the Simulink model in figure 4 for the situations:
$T_{DAC} = 4$; 8; 16 and 32 T_{OCT}
For 8 and $16T_{OCT}$ the output phase noise increase, so the optimum value is:
$T_{DAC} = 4\ T_{OCT}$

4. Conclusions

ΔΣ fractional-N frequency synthesizers are performing solution in frequency synthesis.
The output phase noise depends on the ΔΣ modulator order.
In order to compensate the output phase noise the duration of the DAC compensation pulses is important.
An optimum value is $T_{DAC} = 4\ T_{OCT}$.

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