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PAPERS

Comparative evaluation of multilevel DC link inverter using symmetrical and asymmetrical DC sources

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This paper presents a comparative evaluation of multilevel DC link inverter of photovoltaic (PV) renewable energy system using either symmetrical or asymmetrical dc sources. The four units of dc source can have the same dc voltage level, *ie* 81.32 V, resulting in symmetrical dc sources. The asymmetrical dc sources consist of input dc voltages in binary sequence, 21.68 V, 43.37 V, 86.74 V and 173.48 V. The boost converters with maximum power point tracking (MPPT) capability which is regulated by perturb and observe (P&O) based control are connected between the PV panels and the four dc sources. The varying dc voltages from the PV panels are regulated to track the maximum power available regardless of the irradiance and temperature conditions. The symmetrical dc sources will facilitate the generation of 9 levels of staircase ac waveform rms of 230 V after the H-bridge inverter. Whereas, the asymmetrical dc sources are able to produce 31 levels of staircase ac waveform also with rated rms 230 V. Detailed analysis and comparison on the powers, ac output voltage, output current, total harmonic distortions, and MPPT achievement are described.

K e y w o r d s: multilevel dc link inverter, symmetrical and asymmetrical configuration, perturb and observe, photovoltaic

1 Introduction

Photovoltaic (PV) power generation employing solar panels is one of the most promising types of renewable energy source since the source of energy itself is unlimited, free to acquire and environmentally clean. PV solar energy has been used in a vast amount of applications and has expanded into residential area application in recent years. An example of such application is the standalone PV system which normally consists of PV panels, DC-DC converter, DC-AC inverter and load [1, 2].

Since DC-AC inverter is necessary in a PV system to produce an AC output, the usage of multilevel inverters (MLI) is gaining much more attention nowadays for their ability to generate higher output voltage levels with better harmonics and voltage error performance [3, 4]. The neutral point clamped (NPC), flying capacitor (FC) and cascaded H-Bridge (CHB) are the three widely used traditional topologies of MLI. However, they share one common demerit which is the large number of switching devices required. The required number of devices is further increased for a higher number of output levels [5]. This fact gives rise to the introduction of several reduced switch MLI topologies over the years [6, 7].

One of the most commonly used reduced switch MLI topology is called the multilevel DC link inverter (MLDCL) as proposed in [8]. It is an isolated type MLI which requires separate DC sources based on the number of output levels [9]. The topology can operate using either symmetrical or asymmetrical DC source configuration [10]. Symmetrical DC source configuration requires identical values of DC sources, while asymmetrical DC source configuration uses different value of DC sources selected either by the binary or trinary method [11]. For the same number of switching devices used, the asymmetrical configuration is able to produce a higher number of output levels [12]. To the best of authors knowledge and from the literature review done, comparative analysis on the symmetrical and asymmetrical configurations of the MLDCL inverter is still inadequate to fully understand the operation of the topology especially in terms of power sharing at each power stages of the topology.

The MLDCL inverter is suited for PV system integration since the isolated DC sources can be directly replaced by PV panels. DC-DC converter can be used as the interface between PV panels and inverter [13]. The crucial part of this process is to ensure that the outputs generated from DC-DC converters are fixed before being fed to the inverter so that the desired output level can be achieved. However, the operation of PV panels will vary depending on solar irradiation and surrounding temperature which are not constant over time [14]. Conventionally, proportional-integral (PI) controller is used to fix the voltage by adjusting the duty cycle of a DC-DC converter [15, 16]. However, regular PI controller does not consider maximum power point tracking (MPPT). On the other hand, an MPPT algorithm can be used to track for maximum power point (MPP) [17]. But it is not possible to achieve the fixed DC voltage. It is not possible to control a single DC-DC converter using both techniques.

This work presents a comparative study on MLDCL inverter using either symmetrical or asymmetrical sources in terms of power sharing, input power, output power, total harmonic distortion (THD), pulse width modulation

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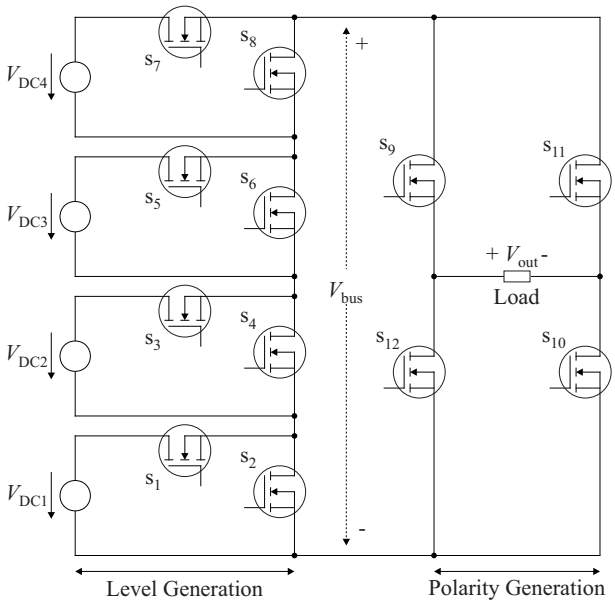

Fig. 1. MLDCL inverter topology with four sources

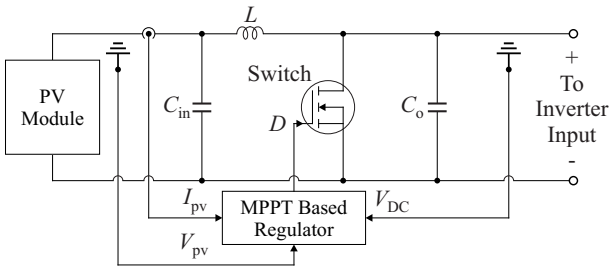

Fig. 2. Boost converter with PV source and MPPT

Table 1. Switching states at level generation stage using symmetrical sources

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V (V)
0	1	0	1	0	1	0	1	0
1	0	0	1	0	1	0	1	1
1	0	1	0	0	1	0	1	2
1	0	1	0	1	0	0	1	3
1	0	1	0	1	0	1	0	4

Table 2. Switching states at polarity generation stage

S_9	S_{10}	S_{11}	S_{12}	Polarity
1	1	0	0	+
0	0	1	1	−

(PWM) approach, number of switches required per generated output level and MPPT capability. The same number of switching devices and PV panels are used in both configurations to compare them fairly. As for the MPPT technique, a perturb and observe (P&O) based voltage regulator is implemented in both tested standalone systems which aims to deliver the maximum possible power to the load while maintaining the fixed DC voltages at the inputs of the MLDCL inverter.

2 System modelling

2.1 9 Level symmetrical multilevel DC link inverter

In general, MLDCL is a hybrid type MLI which composes of level generation stage and polarity generation stage. Figure 1 shows the MLDCL inverter topology consisting of four DC sources. The level generation stage functions to generate positive and zero voltage levels in a staircase waveform pattern. In contrast, the polarity generation stage in the form of an H-Bridge acts to alternately invert each second half-cycle of the generated waveform from the level generation stage into negative levels producing a sine wave like output [18].

For the symmetrical operation of the MLDCL topology, all the voltage sources used are identical in value. In reference to Fig. 1, nine levels of output can be generated from the four sources selected as follows

$$V_1 = V_2 = V_3 = V_4\,. \tag{1}$$

Table 1 indicates the switching states at the generation stage of the 9 level symmetrical MLDCL inverter, while the switching states of the polarity generation stage are given in Table 2. The generalized number of level and switch required is given as [19]

$$N_{L,\mathrm{sym}} = 2n+1\,, \quad N_{S,\mathrm{sym}} = 2n+4 \tag{2,3}$$

where N_L is the number of output level, N_S is the number of switching device required and n is the number of DC source.

2.2 31 Level asymmetrical multilevel DC link inverter

The same topology as in Fig. 1 is used to generate 31 levels of output voltage based on asymmetrical DC source configuration. For 31 output levels by implementing the binary method, the DC sources are determined using geometric progression as follows [20]

$$\frac{V_2}{V_1} = \frac{V_3}{V_2} = \frac{V_n}{V_{n+1}} \quad V_4 = 2V_3 = 2V_2 = 2V_1 \tag{4,5}$$

Switching states at the level generation stage of the 31 level MLDCL inverter are presented in Table 3. The switching states at the polarity generation stage are similar as given in Table 2. Different from the symmetrical configuration, the number of level and switch required in asymmetrical MLDCL inverter can be generalised as [19]

$$N_{L,\mathrm{asym}} = 2n+1\,, \quad N_{S,\mathrm{asym}} = 2n+4\,. \tag{6,7}$$

2.3 Boost DC-DC converter

In this work, boost DC-DC converters are used as the interface units between PV panels and inverter inputs. They are required to regulate the DC voltages generated from PV panels into desired DC voltage values at the inputs of the inverter. Each DC source depicted in Fig. 1 is replaced with PV panels, a boost converter and a feedback controller as shown in Fig. 2.

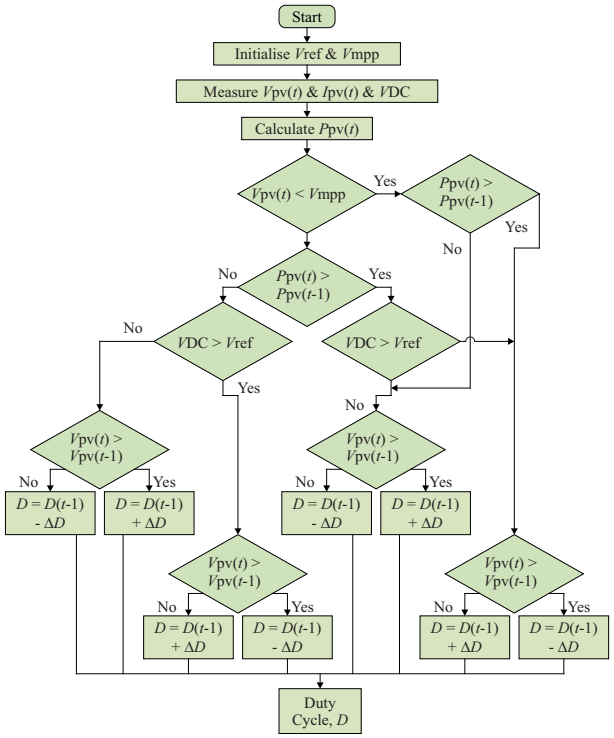

Fig. 3. Proposed MPPT based voltage regulator

Table 3. Switching states at level generation stage using asymmetrical sources

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V (V)
1	0	1	0	1	0	1	0	15
0	1	1	0	1	0	1	0	14
1	0	0	1	1	0	1	0	13
0	1	0	1	1	0	1	0	12
1	0	1	0	0	1	1	0	11
0	1	1	0	0	1	1	0	10
1	0	0	1	0	1	1	0	9
0	1	0	1	0	1	1	0	8
1	0	1	0	1	0	0	1	7
0	1	1	0	1	0	0	1	6
1	0	0	1	1	0	0	1	5
0	1	0	1	1	0	0	1	4
1	0	1	0	0	1	0	1	3
0	1	1	0	0	1	0	1	2
1	0	0	1	0	1	0	1	1
0	1	0	1	0	1	0	1	0

3 Control strategies

3.1 Pulse width modulation strategy

There is no distinct modulation technique required to operate the MLDCL inverter topology except that the combinations of carrier signals to be compared with reference signal using relational operators in generating switching pulses might differ. The most common type of PWM technique that can be used is the carrier-based PWM.

The number of carrier signals required for the operation of MLDCL inverter for both symmetrical and asymmetrical configurations using a single unipolar modulating signal are given as

$$N_{C,\text{sym}} = n\,, \tag{8}$$

$$N_{C,\text{asym}} = 2^{n-2} - 1 \tag{9}$$

where N_C is the number of carrier signal required. In this work, the switching signals for both configurations are generated based on the switching states in Table 1, Table 2 and Table 3.

3.2 P&O MPPT based voltage regulator

In order to achieve constant DC voltage at each input of the MLDCL inverter even under conditions of changing irradiation and temperature, a voltage regulator based on the classic P&O MPPT algorithm is proposed in this work. The algorithm aims to maintain the ability to deliver maximum power to the load under full load operation while achieving the fixed DC voltage based on reference value. Additional constants that need to be initialised in the proposed algorithm apart from step size and initial duty cycle are reference voltage (V_{ref}) and PV voltage at maximum power point (V_{mpp}) under standard test condition (STC). V_{ref} is the desired input DC voltage at inverter input and the value of V_{mpp} can be extracted from PV panel datasheet. Another input that is required to be fed into the proposed MPPT algorithm is the actual output voltage measured at the output of each DC-DC converter. The operation of the proposed algorithm is further explained in the flowchart given in Fig. 3.

4 Results and discussion

All comparative works and evaluations are done using MATLAB/Simulink platform. The aspects that are kept constant for a fair comparison between the symmetrical and asymmetrical MLDCL inverter configurations are the number of PV panels, PV panel model, number of DC sources and PWM technique. The complete simulation block diagram is shown in Fig. 4(a), while the details of each PV and boost stage are given in Fig. 4(b).

PV panel model SPM100-M is selected and modelled carefully in the simulation with its specifications given in Table 4. Fifteen PV panels are used in both configurations so that they have the same power rating. The desired reference values at each inverter input for both configurations of MLDCL inverter are presented in Table 5 and Table 6 respectively. These reference values are chosen on the basis of obtaining 230 Vrms at the inverter output.

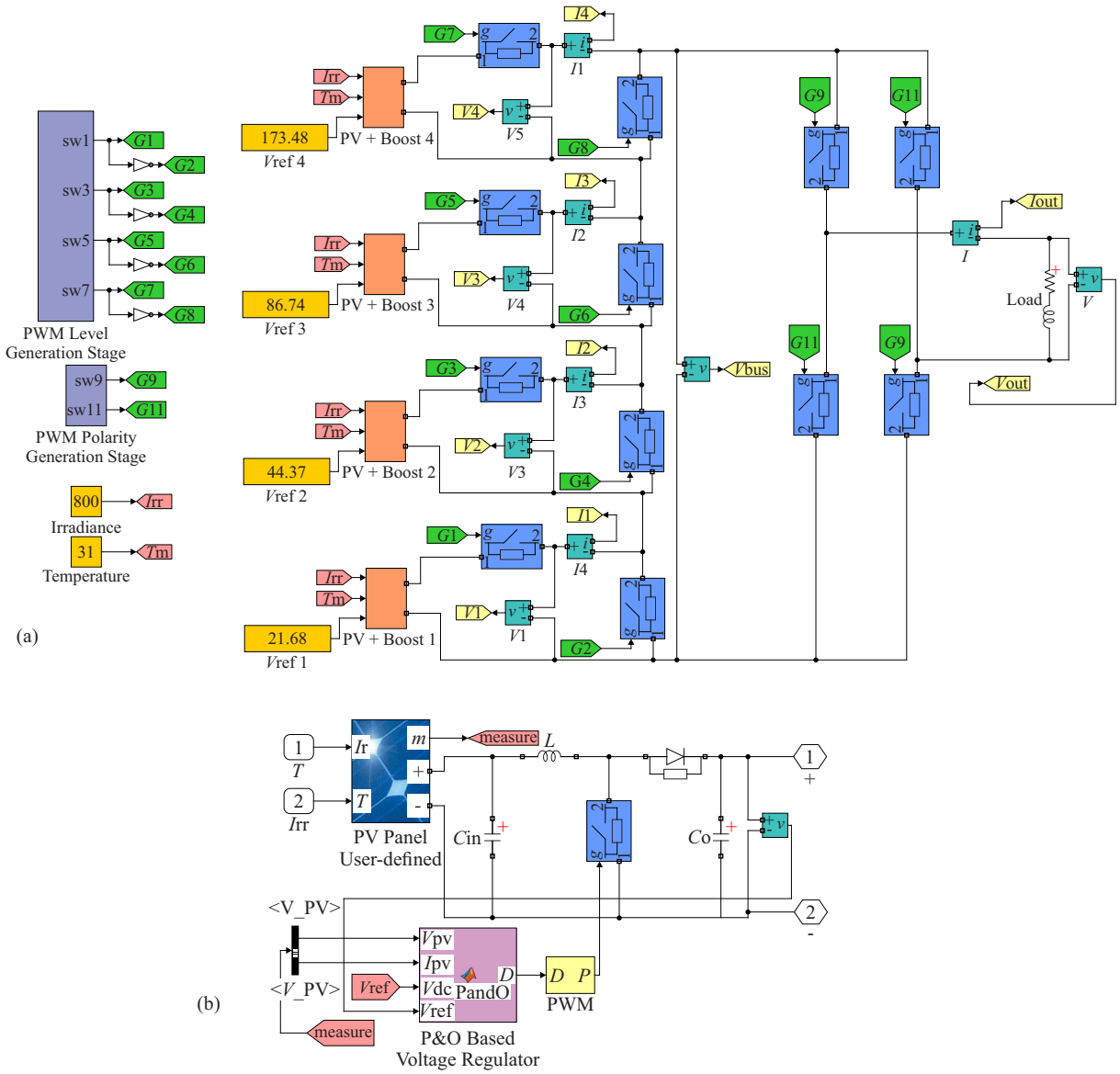

Fig. 4. Proposed MPPT based voltage regulator

4.1 Resistive load test

The PV systems are first tested using resistive loads (R) where the selection of load resistance values are based on output power ranging from 100 W to 900 W with the incremental value of 200 W according to the following equation

$$R = \frac{V_{\text{rms}}^2}{P} \tag{10}$$

where R is the load resistance and P is the targeted output power. Irradiance value of 800 W/m^2 at the temperature of 31 °C is selected as the test conditions. Figure 5 shows the waveforms of the output voltage, current, power and average power with the load of $R = 529\,\Omega$, $P = 100$ W for the symmetrical operation of the MLDCL inverter. Its output harmonic spectrums obtained through fast fourier transform (FFT) analysis are illustrated in Fig. 6. Using the same load value, the waveforms of the output voltage, current, power and average power for the asymmetrical operation of the topology are shown in Fig. 7. Figure 6 also includes the harmonic spectrums and THD values for this asymmetrical configuration.

Other simulation results using different values of R load are presented in Table 7. The table includes power analysis at both input and output of the inverter, power ratio as well as the output THD performance. It can be seen that the symmetrical operation of MLDCL inverter resulted in much higher THD values of above 11 % at all values of R compared to the asymmetrical operation that produced THDs of below 4 %. This is because operating the inverter asymmetrically produced a higher number of output levels for the same number of sources and switches. Referring to the IEEE 519 standard which requires the output THDs to be 5 % at most, filter will most likely be needed for the symmetrical operation of the inverter.

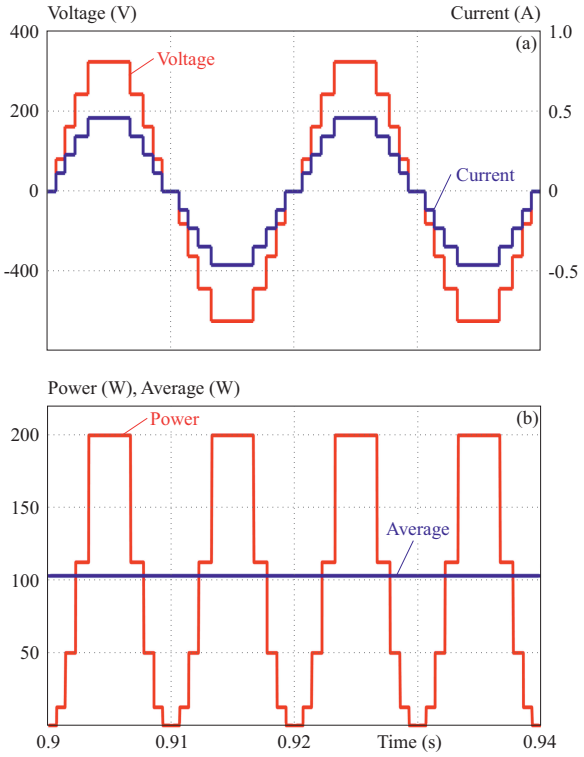

Fig. 5. Output waveforms in symmetrical configuration with $RL = 125\,\Omega$, 243 mH:(a) – voltage and current, (b) – power

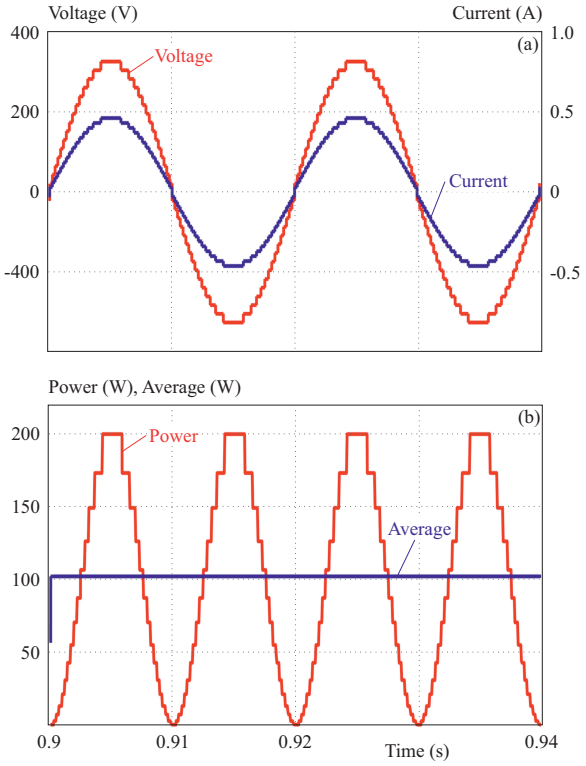

Fig. 7. Output waveforms in asymmetrical configuration with $R = 529\,\Omega$ (a) – voltage and current, (b) – power

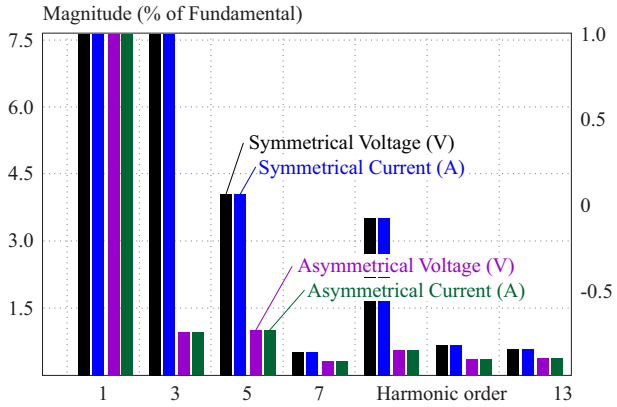

Fig. 6. FFT analysis in both configurations with $R = 529\,\Omega$

Table 4. Paramerers of PV panel model SPM100-M

Parameters	Values
Maximum Power, P_{mpp} (W)	100.125
Voltage at MPP, V_{mp} (V)	18.75
Current at MPP, I_{mp} (A)	5.34
Open-Circuit Voltage, V_{oc} (V)	22.53
Short-Circuit Current, I_{sc} (A)	5.7
Temperature Coefficient of V_{oc} (%/°C)	-0.35
Temperature Coefficient of I_{sc} (%/°C)	0.05
Normal Operating Cell Temperature (°C)	25

It can also be observed that in the symmetrical operation of the MLDCL inverter, the difference in power between stage 1 and 2, stage 2 and 3, stage 3 and 4 are at around 94 %, 86 % and 68 % respectively. The values are almost identical at all tested R loads. As for the asymmetrical operation, at all values of load, the power differences between stages are almost the same between stage 1 and 2, stage 2 and 3, stage 3 and 4 which are at around 230 %. In terms of power ratio, both configurations performed almost ideally with power ratios of approximately above 99.5 %. The term power ratio is used instead of efficiency since the obtained output powers do not yet consider the switching and conduction losses of switching devices used.

4.2 Resistive-inductive (RL) load test

Under the same test conditions as before where the irradiance and temperature are set at 800 W/m^2 and 31 °C respectively, the MLDCL inverter topology is compared using RL loads. Several RL load combinations are selected to produce output power factor (PF) values, ranging from 0.6 lagging to unity. Figure 8 shows the output waveforms of voltage, current and power using the symmetrical configuration with its harmonic spectrums given in Fig. 9 at RL load of $125\,\Omega$, 243 mH ($PF = 0.85$ lagging). Using the same RL load value with asymmetrical source configuration, the output waveforms are illustrated in Fig. 10, while their harmonic spectrums and THDs are also included in Fig. 9.

Simulation results at other selected RL loads are given in Table 8. In terms of THDs, operating the inverter symmetrically produced voltage THD (THDv) of above 11 %

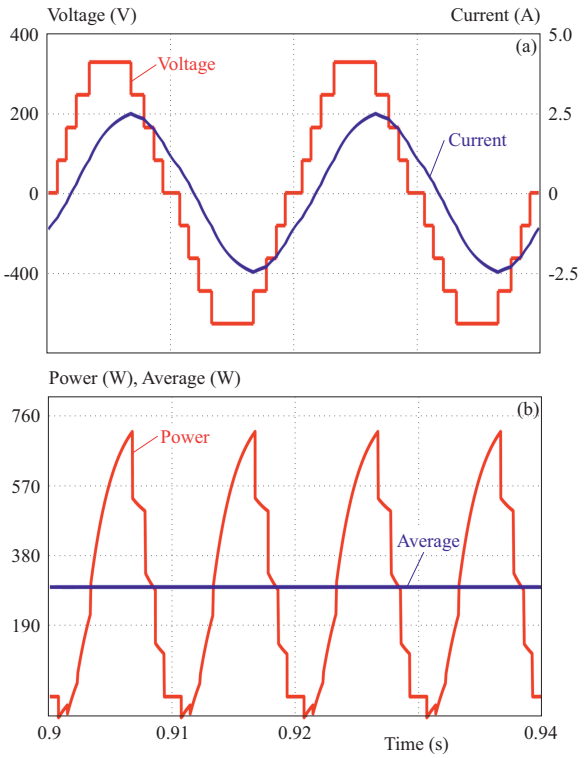

Fig. 8. Output waveforms in asymmetrical configuration with $Rl = 529\,\Omega$, 243 mH (a) – voltage and current, (b) - power

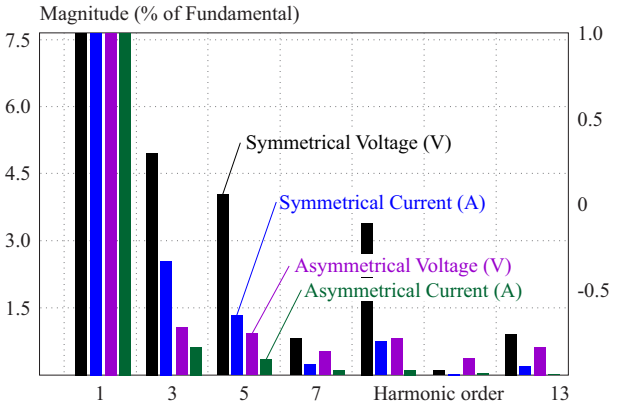

Fig. 9. FFT analysis in both configurations with $RL = 125\,\Omega$, 243 mH

at all RL load values. On the contrary, due to the effect of inductive load, all current THD (THDi) are well below 5 %. In asymmetrical operation of the MLDCL inverter, all values of THDv obtained are still below 4 %, while THDi are lower than 2 %. Regarding the power difference between stages, the results obtained are almost similar to those in the R load test. When using symmetrical sources, the power differences found between stage 1 and 2, stage 2 and 3, stage 3 and 4 are roughly at 93 %, 85 % and 67 % respectively. In the case of asymmetrical sources, the differences in power between each stage are about 230 %. There are no noticeable differences in power factor values in both cases. Concerning the power ratios which are not included in the table, they are all at the value of above 99.5 %.

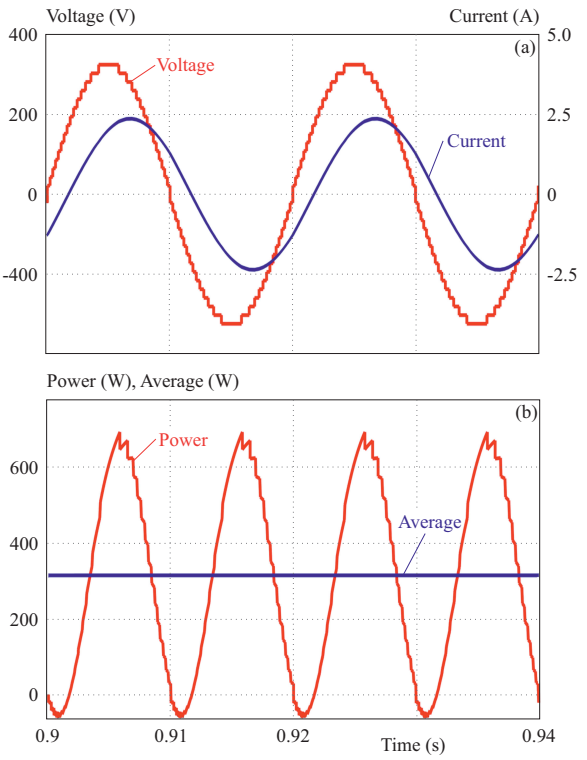

Fig. 10. Output waveforms in asymmetrical configuration with $RL = 125\,\Omega$, 243 mH (a) – voltage and current, (b) – power

Table 5. PV panels arrangement, power and targeted DC voltages using symmetrical configuration

PV	No	$P_{\max}$ (W)	V_{ref} (V)
1	4	312.5	81.317
2	4	312.5	81.317
3	4	312.5	81.317
4	3	234.25	81.317
Total	15	1171.75	325.27

Table 6. PV panels arrangement, power and targeted DC voltages using Asymmetrical configuration

PV	No	$P_{\max}$ (W)	V_{ref} (V)
1	1	78.25	21.68
2	2	156.3	43.37
3	4	312.5	86.74
4	8	624.7	173.48
Total	15	1171.75	325.27

4.3 Maximum power point test

To demonstrate the ability of the proposed MPPT algorithm to deliver maximum power to the load, the PV systems are tested under full-load operation. Selected test conditions of 800 W/m^2 and 31 °C are chosen for this purpose. Using the symmetrical arrangement of DC sources as given in Table 5, the maximum theoretical power that can be extracted by the PV stages in total

Table 7. System Comparison using R-load

Load $R\,\Omega$)	Configuration	Stage power (W) 1	2	3	4	Total	P_o (W)	PR (%)	THD (%) Voltage	Current
529	Symmetric	31.31	29.47	25.35	17.28	103.41	103.12	99.72	11.43	11.43
	Asymmetric	4.98	11.46	26.20	60.85	103.48	103.10	99.63	3.29	3.29
176.33	Symmetric	93.08	87.63	75.34	51.33	307.38	306.91	99.84	11.43	11.43
	Asymmetric	14.82	34.03	77.92	180.61	307.38	306.82	99.82	3.30	3.30
105.8	Symmetric	154.71	145.62	125.20	85.23	510.77	509.74	99.80	11.42	11.42
	Asymmetric	24.65	56.59	129.54	300.00	510.78	509.86	99.82	3.31	3.31
75.57	Symmetric	216.00	203.37	174.76	118.83	712.97	709.96	99.58	11.40	11.40
	Asymmetric	34.44	79.03	180.87	418.71	713.04	710.32	99.62	3.34	3.34

PR - power ratio

Table 8. System Comparison using RL-load

Load $R(\Omega)$	L (mH)	Configuration	Stage power (W) 1	2	3	4	Total	P_R (VA)	k	THD (%) Voltage	Current
684	730	Symmetric	21.90	20.42	17.45	11.77	71.53	71.27	0.95	11.42	4.62
		Asymmetric	3.45	7.96	18.31	42.63	72.35	71.95	0.95	3.29	1.11
125	243	Symmetric	96.03	89.14	75.85	50.93	311.94	311.47	0.85	11.42	3.33
		Asymmetric	15.08	34.77	79.88	185.76	315.49	314.93	0.85	3.30	0.81
54	146	Symmetric	176.42	163.80	139.23	93.43	572.87	571.26	0.76	11.42	2.83
		Asymmetric	27.82	64.04	146.99	341.98	580.83	578.64	0.76	3.31	0.70
32.6	122	Symmetric	211.37	195.97	166.66	111.87	685.87	683.14	0.65	11.47	2.52
		Asymmetric	33.47	76.71	175.76	409.47	695.41	691.99	0.65	3.28	0.59

Table 9. Symmetrical source under full load MPPT test

Stage	Output power (W) PV	Stage	Power ratio (%) MPPT	Stage
1	308.2	304.3	98.62	98.73
2	310.6	301.7	99.39	97.13
3	310.4	304.9	99.33	98.23
4	233.6	228.1	99.72	97.65
Total	1162.8	1139	99.24	97.95
System: Output power 1139 W, Power ratio 97.12				

Table 10. Asymmetrical source under full load MPPT test

Stage	Output power (W) PV	Stage	Power ratio (%) MPPT	Stage
1	73.81	71.28	94.33	96.57
2	153.2	149.4	98.02	97.52
3	310.6	305.3	99.39	98.29
4	623.4	615.0	99.79	98.65
Total	1161.01	1140.98	99.08	98.27
System: Output power 1140 W, Power ratio 97.29				

is 1171.75 W. Therefore, for the full-load operation of the system, R load with the value of 45.15 is selected according to (10) where R is the resistance value for full-load operation and P is the theoretical maximum power of the combined PV stages. The simulated output power at each PV stage and inverter stages along with their power ratios are presented in Table 9. On the other hand, using the asymmetrical configuration of DC sources as in Table 6, the overall theoretical maximum power that can be extracted from the PV stages is 1171.75 W. Applying (10), the same resistance value of 45.15 Ω is selected to operate the system under full-load condition. Table 10 shows the simulation results of output power at each PV stage and inverter stages as well as their power ratios. From these tables, both symmetrical and asymmetrical operation of MLDCL inverter performed quite similarly where the output power of both systems are at around 97 % of the total theoretical maximum PV power of the combined input stages which is satisfactory considering the unbalanced power sharing between stages as demonstrated in the R and RL load tests.

5 Conclusions

A detailed comparative study on multilevel DC link inverter for PV renewable energy system using symmetrical and asymmetrical DC sources has been presented in this paper. Boost converters are used as the interface units between the PV panels and inverter. A P&O based

voltage regulator is proposed to fix the DC voltages from PV panels and to track for PV maximum power despite the varying irradiance and temperature. It is found that using asymmetrical sources, all THD values obtained are within the IEEE 519 standard. THD values using symmetrical sources do not conform to the standard. In the maximum power point test, both system configurations successfully track about 97 % of the theoretical maximum power from the PV panels. Overall, the asymmetrical DC sources arrangement is more favourable since it is able to produce higher output levels which helps reducing the output THDs.

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