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Complex model description and main capacitor sizing for the cross-coupled charge pump synthesis process

Jan Marek[*], **Jiri Hospodka**[*], **Ondrej Subrt**[***]

This paper presents a dynamic part of the pump stage model of the cross-coupled charge pump. The complex model has been used for both the estimation of the N-stage pump properties in a wide range of the input parameters and derivation of equations for synthesis process, as the main capacitor sizing, which is also mentioned in the article. Dynamic part of the model (pump stage capacitances) is determined from Ward's capacitance piece-wise model through the BSIM MOSFET model equations. Main capacitor and load capacitor sizing are based on the time response characteristics fulfilling the system behavior in time. Guideline on the MOS transistor sizing as the nonlinear main pump capacitor and specification of the diode transistor for the design process are also clarified. The characteristics of the proposed circuit have been verified in the professional design environment Mentor graphics and analysis algorithm based on the state-space description of the inner complex model was programmed in Maple SW. The main benefit is to offer the alternative way of the charge pump synthesis by using the complex model and symbolic description of all formulae to find the required pump parameters without long-time simulation process.

K e y w o r d s: time response characteristics, dynamic properties, cross-coupled charge pump, complex model, BSIM equations, pump capacitances

1 Introduction

Cross-coupled charge pump represents the innovative architecture of a two-phase charge pump. They are currently used to power the peripherals on the chip. Easy integrability is among the main advantages of DC/DC converters without inductors. Modern architecture of the cross-coupled charge pump [1] with driving feedback circuit was presented in detail from theoretical analysis [2, 3] through the simulations of real properties [4, 5] to the mathematical model [6, 7], which is including important properties of the circuit structure. The pump stage has been described as an analog subcircuit, labeled X_n and X_L see Fig. 2, through the piece-wise model [5] of the partial blocks using BSIM model MOSFET equations for high-voltage application in microelectronic terminology. This method brings a different view of the quasi-log system behavior, which offers a complicated but fairly accurate analysis of the real circuit.

As a result of this, formulas for the circuit design were derived – CMOS inverter [9], switch transistor and diode transistor sizing [4], including the verification of all formulae in the professional simulator software. Using the state-space description, the creation model also allows estimating static and dynamic parameters in N-stage charge pump [7] through the programme procedure. Certain limitations of the model applicability have been explained. The original model included only static equations, which gives good results only for negligibly small "strange" (parasitic) capacitances [5].

Table 1. Comparison between the static pump model and simulation results [7]

$L = 1\,\mu\mathrm{m},\ W^{\mathrm{S}}/L^{\mathrm{S}} = 2,\ W^{\mathrm{P}}/L^{\mathrm{P}} = 20,\ W^{\mathrm{N}}/L^{\mathrm{N}} = 9,$ $W^{\mathrm{D}}/L^{\mathrm{D}} = 10,\ C = 5\ \mathrm{pF},\ C_{\mathrm{S}} = 0.6\ \mathrm{pF},\ V_{\mathrm{D}} = 1\ \mathrm{V},$ $f_{\mathrm{C}} = 10\,M\,\mathrm{Hz},\ R_{\mathrm{L}} = 1\,\mathrm{M}\Omega,\ C_{\mathrm{L}} = 10\ \mathrm{pF}$				
$\epsilon = 1\,M\,\mathrm{V}$		Calculation	ELDO	
N	n	V_{oA} (V)	V_{oA} (V)	ϵV_{o} (%)
1	33	1.12	1.10	1.8
2	59	1.61	1.53	5.2
3	87	2.02	1.93	4.6
4	109	2.16	2.18	0.91
5	163	2.53	2.48	2
6	202	2.61	2.67	2.2
7	207	2.57	2.47	4

Analysis results of a static pump model, with the given input parameters, are listed in Table 1. The properties were estimated for N-stage charge pump, driven by the clock signal with amplitude V_{D} and frequency f_C. The pump output is loaded by the impedance, consisting the parallel connection of the capacitor C_{L} and resistor R_{L}. Dimensions (width W and length L) of each type of the MOSFETs, M^{D}, M^{S}, M^{N}, M^{P} which are shown in Fig. 1, are the same over all N stages. Moreover, all the MOSFETs have the same length L. The same applies to the main C and parasitic C_{S} capacitances. Parameter ε is the maximal voltage gain, at which the steady state is detected. This was used for the static pump draft, but

* Department of Circuit Theory, Czech Technical University in Prague, FEE, Technická 2, 166 27 Prague, Czech Republic, ASI-Centrum, a company of the Swatch group, Novodvorská 994, 142 21 Prague, Czech Republic, {marekj20, hospodka}@fel.cvut.cz, ondrej.subrt@asicentrum.cz

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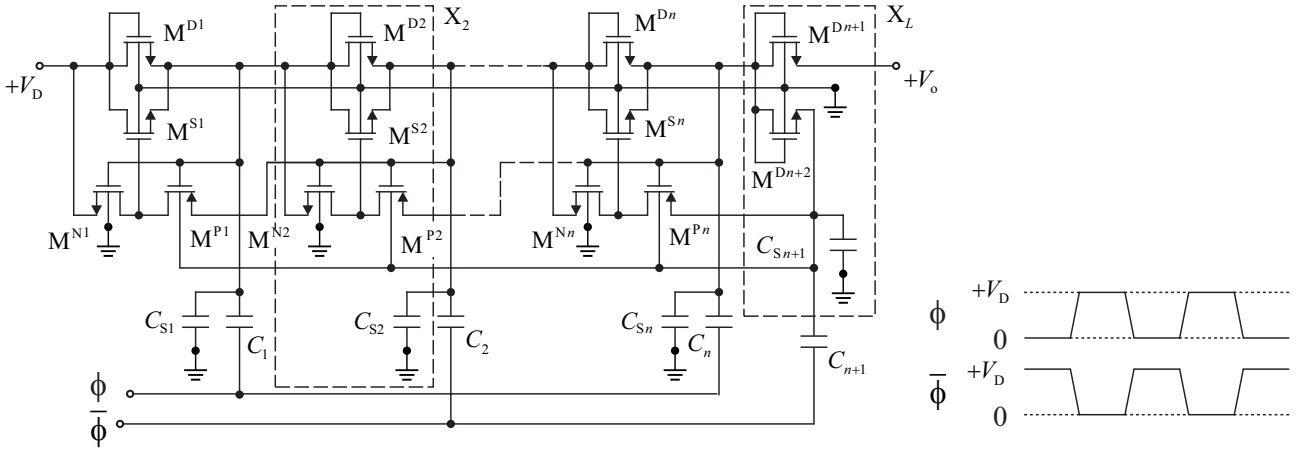

Fig. 1. Cross-coupled charge pump architecture with labeled stage subcircuits, [5]

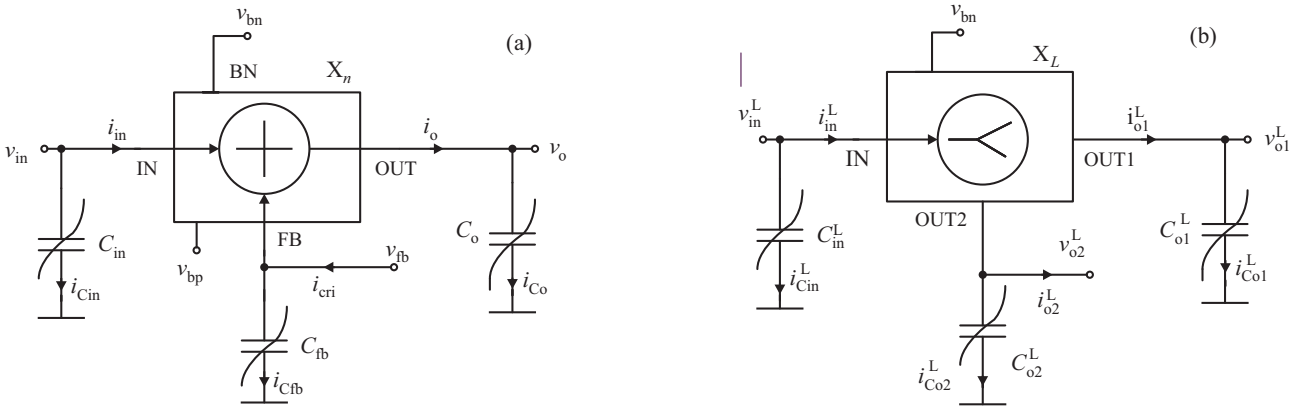

Fig. 2. Dynamic part of the model: (a) – pump stage and (b) – last pump stage

the error in estimating the static and especially dynamic parameters of the pump rapidly increases with setting the main capacity and clock frequency to the extreme values ($C \to C_S$), $f \to f_S$, where the influence of parasitic capacitances cannot be ignored.

In this article, the pump stage model is be completed by the dynamic part including Ward's piece-wise capacitance model. We explain the principle of the capacitance inclusion, and subsequently derive the formulas for the pump stage internal capacitances.

The next part deals with the main capacitor sizing as the last component of the pump stage, which has not been presented yet. Applying specified design criteria, main capacitor value can be found based on the time response characteristics of the first and last pump stage that is additionally connected with the diode transistors. The diode transistor sizing is modified [4] for that task. Finally, the load capacitor sizing for the maximum value of the output ripple voltage is mentioned. All formulae and characteristics were verified in Mentor Graphics Design Architect-IC v2008.2_16.4.

Due to the characterization, the complex model gives correct results for other MOSFET models and allows to analyze variable technological and operational parameters (temperature effect, Monte Carlo analysis, *etc*).

2 Capacitance model of the pump stage

The pump stage model including some dominant properties was created for synthesising design algorithm. Internal controlled current sources [5] are described by the simplified BSIM model equations at defined conditions. The existing model has proved to be satisfactory, in case that the main capacitors value dominates the other (parasitic) capacitances in the circuit. The opposite case will be discussed. Substrate capacitances comparable to main capacitances are well-known design complication because they significantly reduce the voltage potential at each of the stages. The basic principle of inclusion of the dynamic part of the existing model is explained. The aim is to achieve the coincidence of the model and real circuit characteristics on the largest set of input pump parameters, as the low main capacitance ($C \to C_S$) or a wide range of the clock signal frequency. The model does not loose its universality.

The following procedure assumes that substrate-to-ground capacitances are the key part of the model, other effects, like a charge injection, will not be taken into account. The situation is shown in Fig. 2. Each of the blocks X_n, X_L respectively, in N-stage charge pump includes the input and output nonlinear capacitance. Currents i_{in},

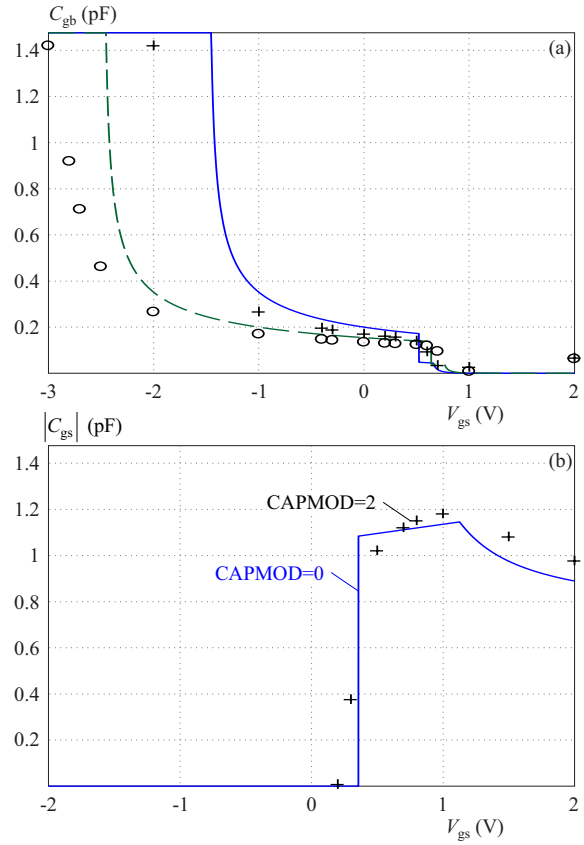

Fig. 3. The variation of the gate-to-base capacitances with DC gate-source voltage: (a) – gate-base and (b) – gate-source capacitance

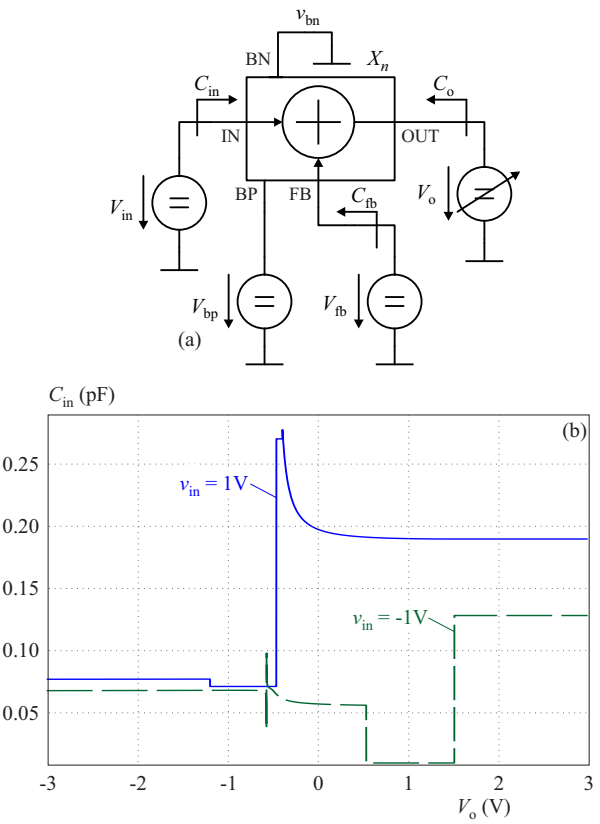

Fig. 4. Analysis of the pump input capacitance: block diagram (a) and waveform (b)

$i_o, \ldots$ represent static part of the model. BSIM capacitance model uses Ward's capacitance model, [8]. Capacitance parameters of the model are derived from the charge Q_i and voltage V_j with respect to the reference point (ground). For small changes the capacitance between electrodes i, j, is

$$C_{ij} = -\frac{\partial Q_i}{\partial V_j}\,. \tag{1}$$

Definition according to (1) makes it quite easy to express particular capacitances that are shown in Fig. 2 without calculation serial-parallel combinations of MOSFETs capacitances. Each of the input/output capacitance is approximately given by the sum of those MOSFETs capacitances, which are connected between the considered external subcircuit terminal and GROUND (substrate in case of the NMOS). According to Fig. 2, the input pump stage capacitance $C_{\rm in}$ is determined by the drain capacitance of $\mathrm{M}^{\rm D}$ and $\mathrm{M}^{\rm S}$ transistors, gate capacitance of $\mathrm{M}^{\rm D}$ transistor and source capacitance of the inverter transistor $\mathrm{M}^{\rm N}$,

$$C_{\rm in} \approx C_{\rm d}^{\rm D} + C_{\rm g}^{\rm D} + C_{\rm d}^{\rm S} + C_{\rm s}^{\rm N}\,. \tag{2}$$

Similarly, for other cases:

$$\begin{aligned} C_{\rm o} &\approx C_{\rm s}^{\rm D} + C_{\rm s}^{\rm S} + C_{\rm s}^{\rm P}\,,\\ C_{\rm fb} &\approx C_{\rm g}^{\rm N} + C_{\rm g}^{\rm P}\,,\\ C_{\rm in}^{\rm L} &\approx C_{\rm d}^{{\rm D}n+1} + C_{\rm g}^{{\rm D}n+1} + \\ &\quad + C_{\rm d}^{{\rm D}n+2} + C_{\rm g}^{{\rm D}n+2}\,,\\ C_{\rm o1}^{\rm L} &\approx C_{\rm s}^{{\rm D}n+1}, \quad C_{\rm o2}^{\rm L} \approx C_{\rm s}^{{\rm D}n+2}\,. \end{aligned} \tag{3}$$

where $C_{\rm s}, C_{\rm d}, C_{\rm g}$ – are the self-capacitances of the source, drain, and gate with respect to the ground.

Here, it is not necessary to take into account all the three charges $Q_{\rm s}$ $Q_{\rm d}$ and $Q_{\rm g}$. Simplification is based on using the charge balance [8]

$$\sum_i C_{ij} = \sum_j C_{ij} = 0 \tag{4}$$

and the fact that some very small, as the drain-source capacitance, can be neglected [11]. As an example, the self-capacitance of the drain is

$$C_{\rm d}^{\rm D} = -\left(C_{\rm dg}^{\rm D} + C_{\rm ds}^{\rm D} + C_{\rm db}^{\rm D}\right) \approx -C_{\rm db}^{\rm D},$$

since $C_{\rm dg}$ is zero due to $V_{\rm dg} = 0$ and $C_{\rm ds} \to 0$, and according to (1)

$$C_{\rm sg}^{\rm D} \approx -\frac{\partial Q_{\rm d}^{\rm D}}{\partial V_g} = -\frac{\partial Q_{\rm g}^{\rm D}}{\partial V_d}.$$

The other components can be rewritten in a similar way. Finally, spare models input/output capacitances, includ-

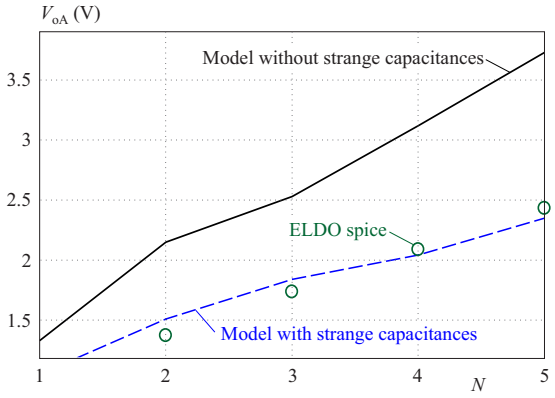

Fig. 5. Influence of the parasitic capacitances in charge pump

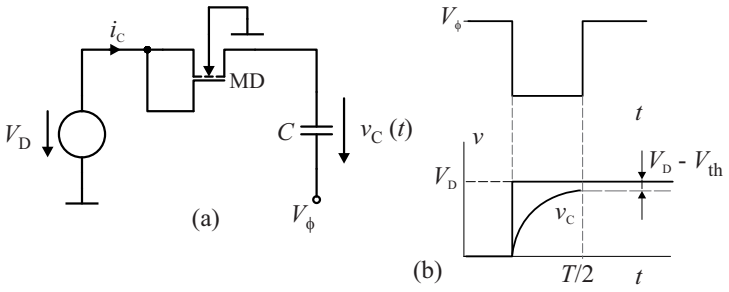

Fig. 6. Charge of the main capacitor in the first pump stage: (a) – diagram and (a) – time response characteristics

ing only two charges: Q_b and Q_g, are

$$
\begin{aligned}
C_\mathrm{in} &\approx -\frac{\partial Q_\mathrm{b}^\mathrm{D}}{\partial V_\mathrm{d}^\mathrm{D}} + \frac{\partial Q_\mathrm{g}^\mathrm{D}}{\partial V_\mathrm{g}^\mathrm{D}} - \frac{\partial (Q_\mathrm{b}^\mathrm{S} + Q_\mathrm{g}^\mathrm{S})}{\partial V_\mathrm{d}^\mathrm{S}} \\
&\quad \frac{\partial (Q_\mathrm{b}^\mathrm{N} + Q_\mathrm{g}^\mathrm{N})}{\partial V_\mathrm{s}^\mathrm{N}}\,, \\
C_\mathrm{o} &\approx -\frac{\partial (Q_\mathrm{b}^\mathrm{D} + Q_\mathrm{g}^\mathrm{D})}{\partial V_\mathrm{s}^\mathrm{D}} - \frac{\partial (Q_\mathrm{b}^\mathrm{S} + Q_\mathrm{g}^\mathrm{S})}{\partial V_\mathrm{s}^\mathrm{S}} \\
&\quad - \frac{\partial (Q_\mathrm{b}^\mathrm{P} + Q_\mathrm{g}^\mathrm{P})}{\partial V_\mathrm{s}^\mathrm{P}}\,, \\
C_\mathrm{fb} &\approx \frac{\partial Q_\mathrm{g}^\mathrm{N}}{\partial V_\mathrm{g}^\mathrm{N}} + \frac{\partial Q_\mathrm{g}^\mathrm{P}}{\partial V_\mathrm{g}^\mathrm{P}}\,, \\
C_\mathrm{in}^\mathrm{L} &\approx \frac{\partial (Q_\mathrm{b}^\mathrm{D} + Q_\mathrm{g}^\mathrm{D})}{\partial V_\mathrm{d}^\mathrm{D}} + \frac{\partial Q_\mathrm{g}^{\mathrm{D}n+1}}{\partial V_\mathrm{g}^{\mathrm{D}n+1}} + \\
&\quad + \frac{\partial (Q_\mathrm{b}^{\mathrm{D}n+2} + Q_\mathrm{g}^{\mathrm{D}n+2})}{\partial V_\mathrm{d}^{\mathrm{D}n+2}} + \frac{\partial Q_\mathrm{g}^{\mathrm{D}n+2}}{\partial V_\mathrm{g}^{\mathrm{D}n+2}}\,, \\
C_\mathrm{o1}^\mathrm{L} &\approx \frac{\partial (Q_\mathrm{b}^{\mathrm{D}n+1} + Q_\mathrm{g}^{\mathrm{D}n+1})}{\partial V_\mathrm{s}^{\mathrm{D}n+1}}\,, \\
C_\mathrm{o2}^\mathrm{L} &\approx \frac{\partial (Q_\mathrm{b}^{\mathrm{D}n+2} + Q_\mathrm{g}^{\mathrm{D}n+2})}{\partial V_\mathrm{s}^{\mathrm{D}n+2}}\,.
\end{aligned}
\tag{5}
$$

BSIM model differentiates the expression of the charge equations Q_s, Q_d, Q_b and Q_g. The expression for a particular circuit is set by the parameter CAPMOD. The basic model (CAPMOD=0 for BSIM 4.6.4) uses the piecewise model, on contrary, modes CAPMOD=1,2 are using single-equation model including many other physical effects in real MOSFET structure (short channel effects, charge thickness). Application of single charge equation is very complicated and its using is even unnecessary with regard to the required capacitance accuracy (tens of pF). Comparison of the analysis results between the piece-wise model (CAPMOD=0) and single equation capacitance model (CAPMOD=2) is shown in Fig. 3. Analytical description of HVT MOSFET capacitances for CAPMOD=0 is indicated by a line in graphs.

The waveform of the voltage-dependent pump stage input/output capacitance was verified in the simulator by using linearized MOSFETs parameters in the operating point, *ie* small signal model (DCOP analysis) [10]. The capacitances waveforms were simulated depending on the selected control voltage, while other voltage sources have been set to a constant. Example of the input capacitance waveform $C_\mathrm{in} = f(v_\mathrm{o})$ at $v_\mathrm{in} = \pm 1$ V, $v_\mathrm{FB} = 2$ V, $v_{bp} = 3$ V and $v_{bn} = 0$ is shown in Fig. 4. Effect of the complex model is appropriate to demonstrate in the N-stage charge pump, where the main capacitance is deliberately set to a low value, for example, $C = 0.5$ pF. Estimation of the output average value was carried out in two ways. Firstly, the original model was implemented without further modifications, secondly, the new version of the model including the dynamic properties according to (5) was used. Complex model is composed of two nonlinear controlled current sources (static part) and three nonlinear capacitances (dynamic part). It is obvious that the original model overestimates the parameters of the real circuit, while the values provided by the new model are closer to those real ones. Maximal relative error $\epsilon_{r_\mathrm{max}} = 10\,\%$ between the calculated and simulated output voltage was found. The behavior of both the models is practically identical with the main capacitance increasing (at the same CLK frequency), as it was expected. The model allows to calculate the parasitic capacitances values in time, which would be practically impossible in the real simulation circuit.

3 Guidlines on the main capacitor sizing

Value of the main capacitor(s) value is important parameter for optimal voltage gain in each of the pump stages. The goal is to achieve such an equivalent internal impedance so that the pump provides the required output voltage at the defined load current I_L. As it is well known, the solution from this point of view is ambiguous [4] because low impedance can be ensured by setting one or more of the other pump parameters (the number of stages, clock frequency, *etc*). However, not only the voltage gain is a design criterion. Other design aspects, for example, power efficiency, total pump area, *etc* should

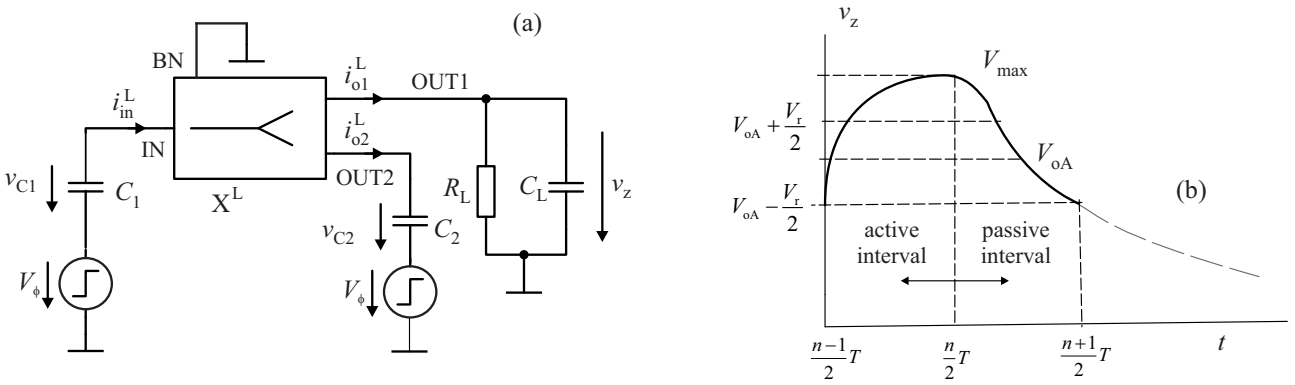

Fig. 7. Energy transport in the last pump stage: block diagram (a) and time response characteristics (b)

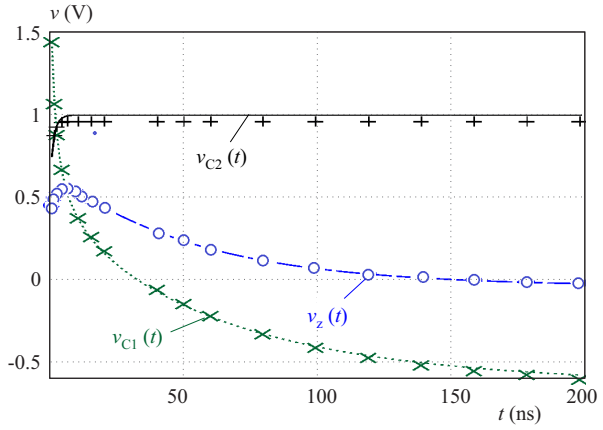

Fig. 8. Time response characteristic of the last pump stage–calculated waveform and simulation results

be taken into account. In this article, the main capacitor sizing is presented through the following design criteria:

- maximal pump voltage gain, while the number stages is minimal
- satisfaction of dynamic properties–rise time

Relation for the switch transistor sizing, which minimizes dominant part of pump losses, assumes known main capacitor value [4]. On the contrary, output voltage and other pump parameters in the steady state are not dependent on the diode transistor sizing, setting of the minimal ratio $W^{\mathrm{D}}/L^{\mathrm{D}}$ is necessary to supply the load current in the active interval of CLK [4]. However, the situation may be quite different in terms of dynamic characteristics. Diode transistors ensure charge transport between capacitors when the output voltage rises from the initial (zero) to the final value. Sufficient voltage increase at each node is a necessary condition of closing the feedback loop in each of the pump stage. Next part is focused on the finding of both parameters C and $W^{\mathrm{D}}/L^{\mathrm{D}}$ that fulfill the previous criteria. Diode transistors must transport the maximum possible amount of charge per half of the switching period, even if the switch transistor of the stage is OFF. The worst case occurs in the first pump stage when the power supply V_{D} is connected and all the capacitors were discharged $(u_c = 0)$. Figure 6 shows the main capacitor charging from the DC voltage source through the M^{D} transistor in the first pump stage, while the down main capacitor terminal is connected to a low logic level $(V_\phi = 0)$ of the clock signal. The symbolic description of the time response characteristic of the equivalent circuit from Fig. 6(a) was derived in [4].

Relation between the main capacitor value and M^{D} transistor sizing follows from the charge stored in passive interval of CLK, $v_c\big|_{t=T/2} = \alpha v_{c_\infty}$, where v_{c_∞} is the end (maximal) value in steady state and parameter α determines the proportion of the charge value and maximal theoretical charge transported during the considered time interval. After that,

$$W = \frac{2C}{v_{c_\infty}\beta T}\,\frac{\alpha}{\alpha - 1}, \quad \text{for } \alpha \in (0,1). \tag{6}$$

Meaning of the other parameters in (6) is explained in [4].

The second equation satisfying required pump voltage gain will be found based on the time response characteristic of the last pump stage, see Fig. 7.

In active interval, current through capacitor C_1 is split to $i^{\mathrm{L}}_{\mathrm{o2}}$ through the main capacitor C_2, and i^{L}_{01} through the load impedance R_{L}, C_{L}. Then

$$i^{\mathrm{L}}_{\mathrm{in}} = i^{\mathrm{L}}_{\mathrm{o1}}(v) + i^{\mathrm{L}}_{\mathrm{o2}}(v).$$

Analytical description of the input/output current is based on simplified BSIM model equation, which are listed in [4, 5, 9]. In steady state, the output voltage $v_z(t)$ varies between values $V_{\mathrm{oA}} - V_{\mathrm{r}}/2$ and $V_{\mathrm{oA}} + V_{\mathrm{r}}/2$, where V_{oA} is average value of the output voltage and V_{r} is peak-ripple voltage value, Fig. 7(b). Circuit from Fig. 7(a) is described by the three following state equations,

$$\begin{aligned} \dot{v}_{\mathrm{C1}} &= \frac{-1}{C_1} i^{\mathrm{L}}_{\mathrm{inl}}, \quad \dot{v}_{\mathrm{C2}} = \frac{1}{C_2} i^{\mathrm{L}}_{\mathrm{in2}}, \\ \dot{v}_z &= \frac{1}{C_{\mathrm{L}}}\left(i^{\mathrm{L}}_{\mathrm{inl}} - \frac{v_z}{R_{\mathrm{L}}}\right), \end{aligned} \tag{7}$$

with general initial conditions $v_{c1}(t_0)$, $v_{c2}(t_0)$, $v_z(t_0)$ and $V_\phi = V_{\mathrm{D}}$ for $t \in \langle \frac{n-1}{2}T, \frac{n}{2}T\rangle$, where $n = \{1, 2, \ldots, k\}$. Solution of (7) for specific values is shown in Fig. 8.

Initial conditions for design purpose are determined from theoretical maximal end values of the node voltages

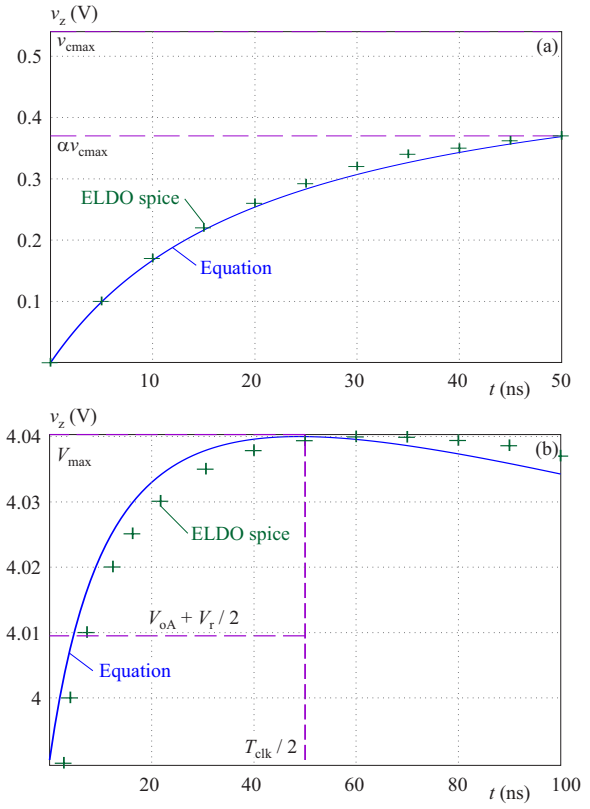

Fig. 9. Time response characteristics of Example

Table 2. Pump output voltage *vs* main capacitance value

$N = 4$								
C (pF)	1	2	4	8	9.9	20	40	80
V_{oA} (V)	2.055	2.5025	2.94	3.31	3.40	3.61	3.71	3.78

in passive interval of CLK at $t = t_0 = (n-1)\frac{T}{2}$, when $V_\phi = 0$ and $V_{\bar{\phi}} = V_D$:

$$\begin{aligned} v_{C1}(t_0) &= \frac{1}{k}(V_{oA} - \frac{V_r}{2}) - V_D \\ &\quad + V_{TH}|_{V_{BS}=-1/kv_z(t_0)}\,, \\ v_{C2}(t_0) &= v_{C1}(t_0)|_{k=1} + V_D - \frac{V_r}{2} \\ &\quad - V_{TH}|_{V_{BS}=-v_{C1}(t_0)|_{k=1}}\,, \\ v_z(t_0) &= V_{oA} - \frac{V_r}{2} \end{aligned} \tag{8}$$

where k has the same meaning as parameter α from (6). It is assumed that $C = C_1 = C_2$ and $C \gg C_S$, where C_S is strange pump capacitance. Parameter k must be less than one, for example $k = 0.95$, to provide the internal transistors are ON at the beginning of the transition and $v_z(t)$ must exceed the value $V_{oA} + V_r/2 < V_{max}$. When k is too small, not the total stored charge can be utilized in the practical circuit.

Final solution for charge pump design is given by numerical intersection of (6) and time response characteristic $v_z(t)$ from (7), which meets the inequality

$$v_z(W^D, C)|_{t=nT/2} \geq V_{oA} + V_r/2 \quad (\leq V_{max})\,. \tag{9}$$

If the numerical algorithm will not find a suitable pair C and W^D, then parameter α must be decreased in the next step. The optimal solution is at the point $v_z = V_{max}$, where the load capacitor is not discharged in the active interval. It is favorable from the view of static efficiency. After that, the output voltage drop in the passive interval is caused only by the real part of the load impedance Z_L (leakage current is neglected) according to the known formula

$$\begin{aligned} v_z(t) &= V_{max} e^{-\frac{t}{\tau}} \\ \text{for } t &\in \langle \frac{n}{2}T,\ \frac{n+1}{2}T \rangle\,. \end{aligned} \tag{10}$$

Using the simplified formulae for start and end values

$$V_{max} \approx V_{oA} + \frac{V_r}{2},$$

$$v_z|_{t=(n+1)T/2} = V_{oA} - \frac{V_r{}'}{2}$$

the ripple output voltage for sufficiently small voltage change during the switching period can be estimated from

$$V_r \approx 2V_{oA}\frac{1 - e^{-\frac{T}{2\tau}}}{1 + e^{-\frac{T}{2\tau}}}, \tag{11}$$

where $\tau = R_L C_L$ is the time constant. Equation (11) allows to estimate the output filter capacitor

$$C_L \geq \frac{T}{2R_L \ln \frac{2V_{oA} + V_{r_{max}}}{2V_{oA} - V_{r_{max}}}}\,. \tag{12}$$

Verification of the mentioned procedure was done on a specific example. The task was to estimate main capacitor value and diode transistor sizing (under given criteria) for a charge pump, giving the output voltage $V_{oA} = 4$ V and load current $I_L = 4\,\mu$A. The maximal peak value of the ripple output voltage at nominal load current must not exceed 20 mV. Power supply voltage is $V_D = 1$ V and clock signal frequency is $f = 10$ MHz. Channel length of MOSFET is $L = 1\,\mu$m.

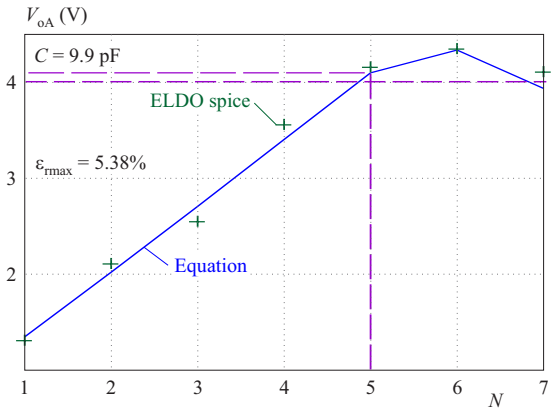

Fig. 10. Pump output voltage vs number of stages

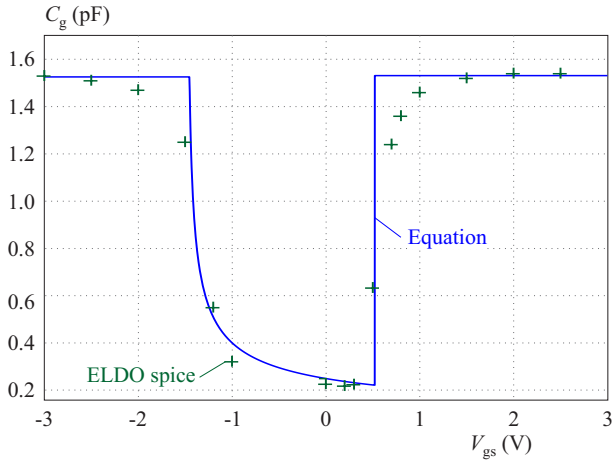

Fig. 11. MOS gate capacitance

- Minimum load capacitor value calculated from (12) is

$$C_{\mathrm{L}} \geq 10\,\mathrm{pF},$$

- initial conditions for solution of state equations (7) are calculated from (8) for $k = 0.95$ with using BSIM model parameters. Active interval, *ie* time range of the response characteristic lies in interval $t \in \langle 0\,, T/2\rangle$,

$$\begin{aligned} v_{\mathrm{C1}}(0) &= 4.17\,\mathrm{V},\\ v_{\mathrm{C2}}(0) &= 3.986\,\mathrm{V},\\ v_z(0) &= 3.99\,\mathrm{V}, \end{aligned}$$

- keeping both design criteria and condition (9), both the parameters are found from numerical solution of (6) and (7). One solution is also set

$$\{C, : W^{\mathrm{D}}\} = \{9.9\,\mathrm{pF}, : 4.8\mu\mathrm{m}\}, \quad \text{for } \alpha = 0.7\,.$$

Responses are shown in Fig. 9. When the diode transistor was sized only under the fist criterion, width is $W^{\mathrm{D}} \simeq 26\,\mu\mathrm{m}$ for $\alpha = 0.95$ at the same capacitor sizing.

It remains to verify obtained results in real-model pump structure, where the other component values are: $W^{\mathrm{P}} = 5\,\mu\mathrm{m}$, $W^{\mathrm{N}} = 16\,\mu\mathrm{m}$ and $W^{\mathrm{S}} = 2\,\mu\mathrm{m}$. The minimal number of stages is $N = 4$, as implies from the following graph in Fig. 10. The characteristic is compared to the simulation results of the complex N-stage pump model. Maximal relative error in the given range is also listed in the graph. Table 2 shows that by reducing the number of pump stages it is no longer possible to reach the required output voltage level while the main capacitor value is distinctly increased. Generally, condition

$$\lim_{C\to\infty} V_{\mathrm{oA}} = V_k, \quad \text{for each } V_k \in \Re$$

is always valid.

3.1 Implementation of the MOS capacitor

Main capacitors are commonly implemented using MOS transistors on design chip, where these MOSFETs are realized in the same technology process. This is one of the main advantages of realization. Nonlinear character of the component can be undesirable in these applications, where the emphasis is placed on analog signal processing (analog-digital converters). Charge transport in voltage converters via non-linear capacitances does not matter much (it may be even beneficial in some cases) but only the minimum capacitance, charge respectively, must be kept due to the correct function. Using BSIM model equations, the symbolic description of the MOS capacitor sizing will be introduced. Supposing the configuration from Fig. 11, total capacitance is given by

$$C_{\mathrm{MOS}} = \frac{\partial Q_{\mathrm{g}}}{\partial V_{\mathrm{g}}}\,. \tag{13}$$

If the MOS will be used as a capacitor, operation in accumulation region ($V_{\mathrm{gs}} \ll V_{\mathrm{th}}$) is required. After that, for long channel technology process, total capacitance is approximately equal to $C \approx W_{\mathrm{eff}} L_{\mathrm{eff}} c_{\mathrm{oxe}}$ [11]. However, during the pump rise time and overcharging, the voltage on capacitors can become to zero or negative value. In the subthreshold region, real MOS capacitance is markedly smaller, see Fig. 11. Charge, defined as A VERB IS MISSING

$$\begin{aligned} Q_{\mathrm{g}}^{\mathrm{sub}} &= W_{\mathrm{eff}} L_{\mathrm{eff}} C_{\mathrm{oxe}} \frac{K_{1\mathrm{ox}}^2}{2}\left(-1+\sqrt{\zeta}\right),\\ \text{where } \zeta &= \frac{4(V_{\mathrm{gs}} - V_{\mathrm{f}} - V_{\mathrm{bs}})}{K_{1\mathrm{ox}}^2}, \end{aligned} \tag{14}$$

C_{oxe} is electrical oxide capacitance, $K_{1\mathrm{ox}}$ is body effect parameter and V_{f} – is flat-band voltage, [8]. If the parameter V_{f} is not given, then is calculated from [8]

$$V_{\mathrm{f}} = V_{0\mathrm{th}} - \phi_{\mathrm{s}} - K_1\sqrt{\phi_{\mathrm{s}}}\,,$$

where ϕ_{s} is surface potential and $V_{0\mathrm{th}}$ is threshold voltage at zero bias voltages. From the both previous equations, minimal capacitor value for charge pump is defined at bias voltage $V_{\mathrm{gs}} = V_{\mathrm{th}}$

$$C_{\mathrm{min}}|_{V=V_{0\mathrm{th}}} = \frac{W_{\mathrm{eff}} L_{\mathrm{eff}} C_{\mathrm{oxe}}}{\sqrt{1 + 4\dfrac{\phi_{\mathrm{s}} + K_1\sqrt{\phi_{\mathrm{s}}}}{K_{1\mathrm{ox}}^2}}}\,. \tag{15}$$

4 Conclusion

The dynamic part of the pump stage model and main capacitor sizing for the cross-coupled charge pump architecture was presented in this paper. It was shown, that main particular parts of the charge pump design process determined by the static part of the MOSFET (threshold voltage, body effect, the full description of the CMOS

inverter transfer characteristics, *etc*). Strong inversion region of pump MOSFETs has proven to be sufficient for modelling real properties of the N-stages charge pump.

The implementation of the capacitive part into the original model eliminates its usability only for sufficiently large main capacity, making it credible for a wide range of parameters (main capacitors value, clock frequency). Of course, estimation of dynamic parameters such as rise time or energy efficiency is improved. Analytical description through the BSIM model equations for long channel process was used. Firstly, the dynamic model for estimation of the substrate capacitances in each pump stage was introduced. The principle is based on the transformation of the internal MOSFET capacitances into the input/output model terminals (5). Piece-wise Ward's capacitance model was implemented for description and partial $C_{ij}(V)$ characteristics, see Figs. 3, 4, were verified using the small signal MOSFET model.

Complex pump stage model provides concurrence of the characteristics with simulation results (Figs. 5, 10) despite a certain degree of simplification. Capacitive couplings (charge injections) between pump stages are not considered. However, the main difference between using the original static model and new complex model for low main capacitances values is obvious.

The main capacitor value in charge pump was found, so that the static efficiency (maximal voltage gain – low equivalent internal impedance at defined load current) and dynamic properties (rise time after connecting power supply voltage) were secured. Under given conditions, capacitor sizing is connected with the diode transistor sizing. Both the parameters W^{D} and C were found as intersection of time response characteristics in the first stage with zero initial condition and the last pump stage in steady state (7), so that the energy transport would be maximal in half of the period of CLK.

As a result of this setting, the load capacitor is discharged only in the passive interval. Therefore, the minimal load capacity value was derived from the peak value of the output ripple voltage (12). Determination of these parameters was shown in the practical example with simulation results in N-stage circuit topology. The solution was designed for the minimal number of stages, as it is evidenced in Tab. 2. But in general terms, this task is not unambiguous (N *vs* C, *etc*). If the nonlinear MOS capacitor is used, then the minimal capacity value (Fig. 11) should be respected (11).

The main issue of the article is using the design formulas and complex model for synthesis algorithm without long-time numerical optimization process. Future work includes the development of the design procedure through the state-space model and testing for a wide range of the input requirements and comparison the results with the simulation ones using the optimization algorithm.

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Jan Marek was born in Prague on April 8, 1990. He graduated from the Czech Technical University in Prague in 2014 and is currently studying towards PhD at the Department of Circuit Theory. His research interests deal with the design of current analog circuits, as well as their optimization.

Jiří Hospodka was born in 1967. He received his Masters and PhD degrees from the Czech Technical University in Prague in 1991 and 1995, respectively. Since 2007 he has been working as associate professor at the Department of Circuit Theory at the same university. Research interests: circuit theory, analog electronics, filter design, switched-capacitor, and switched current circuits.

Ondřej Šubrt was born in Hradec Králové on February 24, 1977. He works as Senior IC Designer engineer with ASI-Centrum Prague, a company of the Swatch Group. At present, he has also been appointed an Assoc Prof at the Faculty of Electrical Engineering, CTU Prague. His professional interests being integrated circuits design with emphasis to Non-volatile Memory design, compact models and Process Design Kit Development.