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# Analysis, design and simulation of digital controlled symmetrical seven levels inverter

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An analysis, design and simulation of digital controlled symmetrical seven levels inverter is presented in this paper. Against the contemporary use of two asymmetrical DC sources with two H-bridge cells to generate seven levels inverter two DC sources of equal voltage ratings are used through digital control strategy to realize seven levels output voltage. By utilizing limited number of active switching components and avoiding the usual complex PWM control techniques for multilevel inverters by way of digital control strategy, high efficiency multilevel inverter systems due to reduction in total harmonic distortion and switching losses is guaranteed. Owing to symmetry of the H-bridge cells, a simple and single programmed counter built around J-K flip is required irrespective of number of cascades. The analyzed and designed system has been simulated in MATLAB/SIMULINK environment. With an R-L load of 200 Ω and 200 mH, improved total harmonic distortions (THDs) for the inverter current and voltage are 7.59 % and 16.89 % respectively. The obtained results show that the control-circuit-based multilevel inverter topology is most suited for applications in solar powered inverter systems.

K e y w o r d s: seven level inverter, cascaded H-bridge, J-K flip-flop, transition table, digital control

## 1 Introduction

Cascade H-bridge multilevel inverter (CHBMI) structure has been attracting increasing interests in high power and medium voltage applications owing to its lower total harmonic distortion (THD), less switching losses, higher efficiency and lower voltage stress compared to two-or three-level inverters [1–4]. A cascaded multilevel inverter consists of a series of H-bridge inverters with each H-bridge unit having its own DC source [1] or a single DC source and capacitors-based DC sources [3] for all but the first source. For a cascaded H-bridge multilevel inverter the number of $m$ levels can be obtained from the relation $m = (2k + 1)$ while the number $n$ of active switches is $n = 2(m - 1)$ where $k$ is the number of H-bridge cells or DC sources. Going by the hypothesis, three H-bridge cells and twelve active switches are demanded for a seven level inverter [5, 6]. The seven levels however, can also be realized with only two H-bridge cells and two independent DC sources of different values popularly referred to as asymmetrical seven levels inverter [7–11]. Several attempts have been made in the recent past by researchers to synthesize the multilevel inverter (MLI) with few number of H-bridge cells or active switches, in order to circumvent the $2k + 1 = m$ levels hypothesis. In such attempts there are always the presence of one or more auxiliary switches and diodes with additional control circuits. In one of the attempts to accomplish the seven level output voltage using few active switches, a new seven level inverter topology having one H-bridge cell, four auxiliary switches and three DC sources was simulated [12]. There exists, however, at present a seven levels inverter with only five active MOSFET switches but with four symmetric DC sources [13]. The topology presents a less utilization of sources as one of the DC sources is not reflected at the output hence the maximum attainable output DC voltage is +3 V. The pulse pattern to trigger the switches were generated through carrier-based pulse width modulation (CBPWM) technique that requires $(n - 1)$ carriers, one sinusoidal reference signal, seven comparators and about 13 logic gates. In this scheme it is obvious that significant reduction in active switches is realized at the expense of less DC source utilization and complex control strategy.

It has not been reported in literature that a symmetrical seven levels inverter has been realized with two H-bridge cells and equal value DC sources. With equal value DC sources, the two H-bridge sources will obey the conventional theorem to generate a five level inverter output voltage. Asymmetric multilevel inverters differ from symmetric multilevel inverters only in the ratings of input DC voltages and control strategies. In some applications like in solar powered grid-connected inverter systems it is not economical to use DC sources having different values as it could lead to voltage imbalance among the different PV sources. Various control strategies aimed at reducing the THD of the CMLI have been proposed. Most of the control strategies involve modulations where sinusoidal reference signals are compared with triangular carrier waves to generate gating signals. This ultimately demands the designs and/or implementations of triangular carriers and sinusoidal signals generating circuits. In most cases, the number of carrier waves in CMLI PWM controls is one less than the required output voltage lev-

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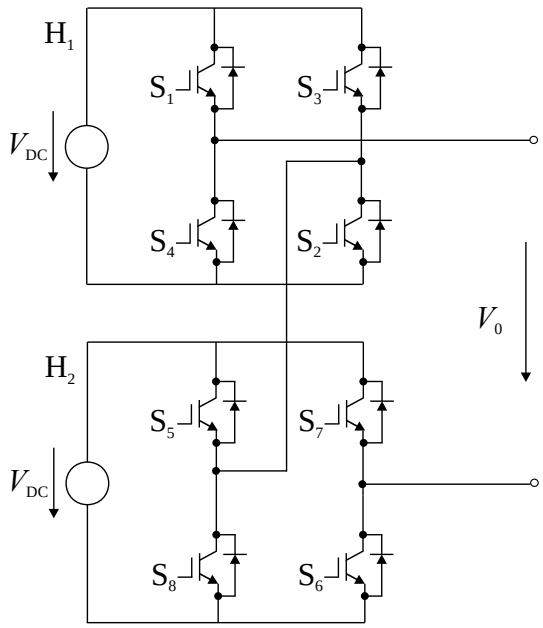


**Fig. 1.** Seven level cascaded h-bridge voltage source inverter (VSI)

**Table 1.** State transition table

| Present state | | Next state | | Required excitation for the next state | | | |
|---|---|---|---|---|---|---|---|
| $A$ | $B$ | $A^*$ | $B^*$ | $J_A$ | $K_A$ | $J_B$ | $K_B$ |
| 0 | 0 | 1 | 0 | 1 | x | 0 | x |
| 0 | 1 | 0 | 0 | 0 | x | x | 1 |
| 1 | 0 | 1 | 1 | x | 0 | 1 | x |
| 1 | 1 | 0 | 1 | x | 1 | x | 0 |

els. In some PWM techniques, rectified sinusoidal modulating/reference signals are compared with the triangular carrier. This also requires a rectifier circuit which is widely known to be a source of harmonics.

It is quite anticipated that a given level of MLI realized with few H-bridge cells through control circuit based design [15] will result in compact system with greater efficiency and reliability compared to realizing the same level of MLI with same number of H-bridge cells but with additional auxiliary power circuit components or achieving the same level of output voltage with greater number of H-bridge cells.

In this paper, two H-bridge cells with equal DC sources are utilized to obtain a seven level inverter output voltage through digital control strategy.

## 2 Proposed seven level inverter

The power circuit of the proposed single phase cascaded H-bridges seven levels inverter is shown in Fig. 1. It consists of two series connected H-bridge cells with two symmetrical DC sources and eight active switches. Going by the conventional cascaded H-bridge structure, PWM control of the symmetrical inverter is only capable of generating five level output voltage. With the digital control strategy the $m$ levels of the inverter output is related to the number $k$ of H-bridge cells or DC sources as

$$m = 2k + 3\,, \tag{1}$$

while the number n of active switches is

$$n = 2m - 3\,. \tag{2}$$

Equations (1) and (2) when compared with the conventional hypothesis provides for greater number of output levels and less number of active switches for same number of H-bridge cells or DC sources. The sum of the $H_1$ and $H_2$ DC sources defines the peak of the resulting staircase output voltage. The switching patterns for the eight switches are illustrated in details in the next section.

## 3 Digital control strategy

The genesis of this digital control strategy stems originally from the control of modified sine wave inverter which requires the specification of angle of zero voltage also referred to as dead spots between the positive and negative half-cycles of the output voltage [14]. And depending on the value of the angle of zero voltage, one cycle of the inverter output voltage is divided into segments with each segment equal to twice the angle of zero voltage. With the up-counting characteristics of the digital counter implemented using J–K flip-flops, a square wave

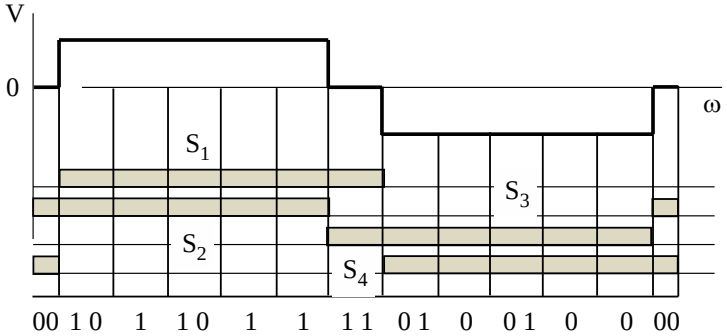


**Fig. 2.** Switching patterns for a squire wave inverter output voltage

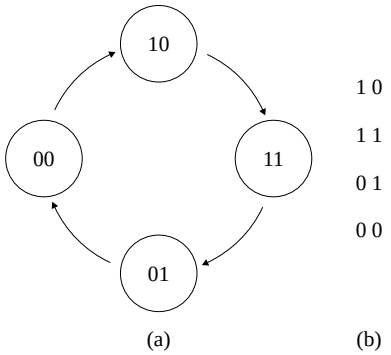


**Fig. 3.** Switching sequence for the single phase inverter (a) – flow graph (b) – state transition

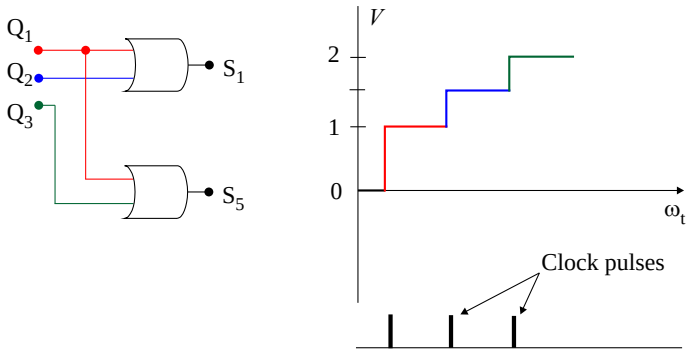


**Fig. 4.** Combinational logic signal sequences for switches $S_1$ and $S_5$ in a quarter of a cycle

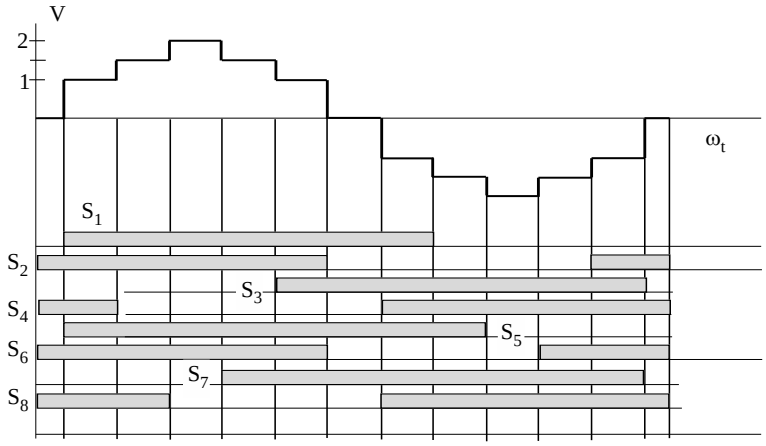


**Fig. 5.** Switching patterns for the seven levels inverter output voltage

inverter can easily be obtained as shown in Fig. 2. The peculiar advantage of this control strategy is that because of symmetry of the H-bridge cells in a cascaded structure, no additional counter design is required. The switch signals for the additional cells are obtained through logic combinations of the successive J–K flip-flop output signals. The number of flip-flop blocks in a designed counter depends on the number of repeated states corresponding to positive and negative half cycles of the voltage in Fig. 2. For the counter design of $H_1$ cell, the inverter top switches are assigned nomenclatures such that $S_1$, $S_3 = A\ B = 1\ 1$ while switching signals for the down switches are assigned nomenclatures such that $S_2$, $S_4 = \bar{A}\ \bar{B} = 0\ 0$. These switches are fired in the sequence $S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4$.

A delay angle of 15° is selected from which twelve segments of $\pi/6$ or 30° each for one switching cycle is obtained as shown in Fig. 2. As can be observed from Fig. 2, the states '0 0' and '1 1' corresponding to zero level voltages are not repeated while the states '1 0' and '0 1' corresponding to the positive and negative output pulses respectively are each repeated five times. With these switching states, the flow graph and state transition are obtained as shown in Fig. 3. The transition table showing the switching sequence is generated as displayed in Table 1. The resulting characteristic equation (obtained from the state transition table) is

$$J_A = \bar{A}\bar{B}\,, \quad K_A = AB\,, \quad J_B = A\bar{B}\,, \quad K_B = \bar{A}B\,. \quad (3)$$

Equation (3) is further simplified utilizing two variable Karnough map. In setting out the J–K flip flop based counter switching circuit, the number of repeated states and their location in the required excitation for the next state inside the state transition table, determine the number of blocks of the flip flop and the output terminals to which the inverter switches are connected.

The staircase inverter output voltage is realized when the switch signals are logic combinations of successive J–K flip-flop output signals. With this control strategy, the widths of voltage steps can be made equal to the segments. The more the number of segments per cycle, the more the likelihood of generating many levels of the inverter output voltage. For the seven levels inverter voltage, one cycle of the output voltage is divided into twelve segments with 15° angle of zero voltage. A squire wave inverter with angle of zero voltage is conventionally a three level inverter. For the seven levels inverter voltage that requires additional four levels (two levels per quarter cycle), the flip-flop output signal $Q_2$ is ORed with $Q_1$ to supply the switch $S_1$ of the $H_1$ cell while $Q_3$ is ORed with the flip-flop signal Q1 to supply the switch $S_5$ of the $H_2$ cell. In this instance, the OR-gates perform the sample and hold criterion of a digital control structure hence the staircase output voltage. Figure 4 displays the combinational logic signal sequences for switches $S_1$ and $S_5$ for a quarter of a cycle. The sample and hold actions

**Table 2.** Switching states and output voltage

| Segment | $S_8 = \bar{A} + \bar{B}_1 + \bar{B}_2$ | | | $S_7 = B_3 + B_4 + B_5$ | | | $S_6 = \bar{B}_3 + \bar{B}_4 + \bar{B}_5$ | | | $S_5 = A + B_1 + B_2$ | | | $S_4 = \bar{A} + \bar{B}_1$ | | $S_3 = B_4 + B_5$ | | $S_2 = \bar{B}_4 + \bar{B}_5$ | | $S_1 = A + B_1$ | | $V_0$ (V) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\bar{B}_2$ | $\bar{B}_1$ | $\bar{A}$ | $B_5$ | $B_4$ | $B_3$ | $\bar{B}_5$ | $\bar{B}_4$ | $\bar{B}_3$ | $B_2$ | $B_1$ | $A$ | $\bar{B}_1$ | $\bar{A}$ | $B_5$ | $B_4$ | $\bar{B}_5$ | $\bar{B}_4$ | $B_1$ | $A$ | |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 2 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1.5 |
| 3 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 2 |
| 4 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1.5 |
| 5 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 6 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 7 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 x | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | -1 |
| 8 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | -1.5 |
| 9 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | -2 |
| 10 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | -1.5 |
| 11 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | -1 |
| 12 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

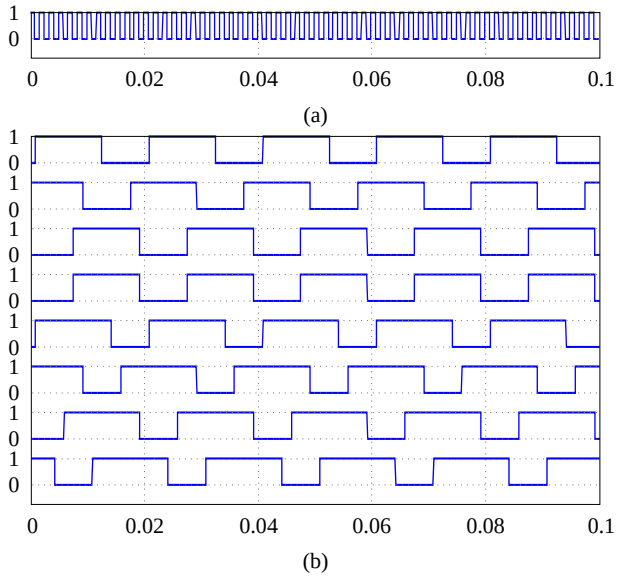


**Fig. 6.** Inverter switching signals (a) – clock signals (b) – switching signals for switches $S_1$ to $S_8$

of the two inputs OR-gates supplying the switches $S_1$ to $S_8$ cause the switching segments for switches $S_1$ to $S_4$ to appear to be seven or 210° and the segments for switches $S_5$ to $S_8$ to appear to be eight or 240° as indicated in Fig. 5. Table 2 displays the switching states and the corresponding seven level inverter output voltages for one switching cycle.

## 4 Simulation results

The designed digital controlled seven levels inverter has been simulated using MATLAB/SIMULINK to verify the uniqueness of the control strategy. Fig. 6 shows the inverter switching signals. Fig. 6(a) shows the counter clock signals while Fig. 6(b) displays the switch signals.

The inverter output voltage and current are shown in Fig. 7. The widths of the voltage steps correspond to the width of the segments in the design. The fast Fourier transform (FFT) of the inverter load current is displayed in Fig. 8 while the FFT of output voltage is shown Fig. 9. With an R–L load of 200 Ω and 200 mH, a THD of 7.6 % is obtained for the load current whereas it is 16.9 % for the output voltage.

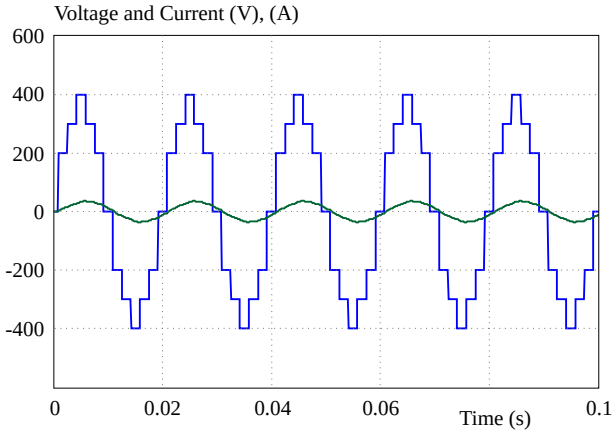


**Fig. 7.** Inverter output voltage and current

## 5 Comparison of topologies

As reported in literature, several research attempts have resulted in different topologies of seven levels inverter schemes with the primary interest of achieving reduced switches, low switching losses and improved THD. Table 3 shows comparisons of conventional cascaded multilevel structure (CMLS) [13], a topology having one H-bridge cell, four auxiliary switches and three

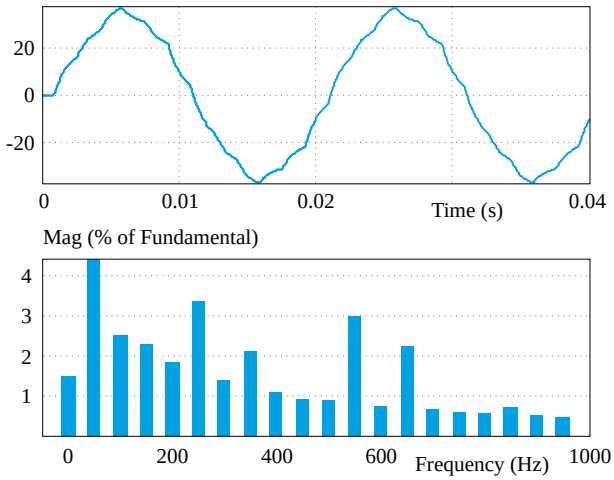


**Fig. 8.** FFT of the inverter load current

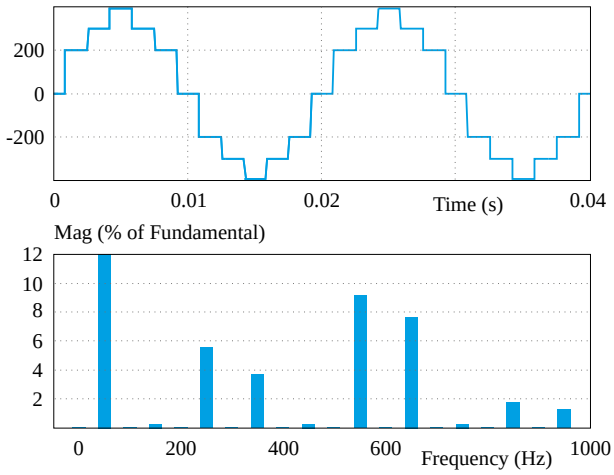


**Fig. 9.** FFT of the inverter output voltage

**Table 3.** Comparison of proposed seven levels inverter with other topologies

| Component count | Topology | | | |
|---|---|---|---|---|
| | Cascaded Multilevel Structure | 1 H-bridge cell, 4 auxiliary switches and 3 DC sources | 5 active switches and 4 DC sources | Proposed 2 H-bridge cells and 2 DC sources |
| No. of switches | 12 | 8 | 5 | 8 |
| No. of DC sources | 3 | 3 | 4 | 2 |
| No. of unutilized DC sources | – | – | 1 | – |
| %THD of output voltage | 23.13 | 14.62 | 16.12 | 16.89 |

DC sources [12], another topology with only five active MOSFET switches but with four symmetric DC sources [13] with the proposed structure in terms of number of switches, number of DC sources, number of utilized DC sources and percentage total harmonic distortion of the seven levels output voltage.

Table 3 clearly reveals the obvious reduction of switches in the three last topologies when compared to the CMLS with the topology in column 3 presenting the least number of switches. The topology in column three presents the highest number of DC sources with one redundant DC source while the proposed topology presents the least number of DC sources. The topology in column two presents the least THD. In comparison with the proposed topology, the topology in column two shares same number of switches but with improved THD at the expense of additional DC source. The proposed topology has a THD closer to the THD of the topology in column three but while the proposed topology has eight switches the topology in column three has only five switches at the expense of four DC sources with one DC source being redundant. The proposed topology, therefore, will find better application in a solar powered inverter system as it is more economical and practicable to deploy two photovoltaic (PV) systems as DC sources than involving four of such systems. In terms cost effectiveness the price of a single PV panel far much outweigh a good number of switch components as may be saved by employing the topology with five switches and four DC sources.

## 6 Conclusions

An analysis, design and simulation of digital controlled symmetrical seven levels inverter have been presented. Against the contemporary use of two asymmetrical DC sources with two H-bridge cells to generate seven levels inverter, two DC sources of equal voltage ratings are used through digital control strategy to realize seven levels output voltage. Utilizing the method of modified sine wave inverter control in which angle of zero voltage or dead spots between the positive and negative half-cycles of the output voltage is specified one cycle of the voltage is divided into segments with each segment equal to twice the angle of zero voltage. Owing to the symmetry of cascaded H-bridge cells, a simple but single counter built with J–K flip-flops supply the switch signals through logic combinations of the successive output signals. The control-circuit-based digital control strategy utilized only eight active switches and two symmetrical DC sources to guarantee high efficiency multilevel inverter system due to reduction in total harmonic distortion and switching losses. The analyzed and designed system has been simulated in MATLAB/SIMULINK environment. With an R–L load of 200 Ω and 200 mH, improved THDs for the inverter

current and voltage are 7.6 % and 16.9 % respectively. The obtained results show that in comparison with most recent topologies with reduced switching components the control-circuit-based multilevel inverter topology is most suited for application in solar powered inverter systems.

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