

ELECTRICAL PROPERTIES OF RECESSED AlGa_N/Ga_N SCHOTTKY DIODES UNDER OFF-STATE STRESS

Martin Florovič — Jaroslav Kováč — Peter Benko
— Aleš Chvála — Jaroslava Škriniarová — Peter Kordoš *

Electrical properties of recessed and non-recessed AlGa_N/Ga_N Schottky diodes under off-state stress were investigated. The samples were consecutively stressed by the stepped negative bias (–60 V). Before and after the stress I – V and C – V characteristics were evaluated to verify the device degradation process. Finally, the degradation mechanism and the influence of AlGa_N recessed layer thickness on the electrical properties of the Schottky diodes were analysed. It was found that the short time stress influence on I – V characteristics was most negligible for the non-recessed sample. Shallow and deep recessed samples exhibited initial trap filling and reverse current decrease. Generally it was found that the stress voltage near 60 V caused recoverable device degradation.

Keywords: AlGa_N/Ga_N Schottky diode, 2DEG, off-state stress, traps, recess

1 INTRODUCTION

AlGa_N/Ga_N devices are promising due to the presence of macroscopic spontaneous and piezoelectric polarization which induces two-dimensional electron gas (2DEG) at the AlGa_N/Ga_N interface. Superior carrier saturation velocity, high thermal conductivity and high breakdown of Ga_N-based materials are required for high temperature and high speed applications [1]. However, it is well known that Ga_N-based devices exhibit degradation of their performance, which was ascribed for example to the generation of defects through converse piezoelectric effect [2]. Additionally, it was indicated that reverse-bias degradation of Ga_N-based HEMTs and Schottky diodes could be time-dependent mechanism for a given Ga_N-based technology [3]. The Schottky gate contacts prepared on AlGa_N/Ga_N-based structure determine the basic properties of particular HEMT devices. Therefore it is necessary to understand the degradation process that occurs in proximity of the Schottky gate edge, in the region where the electric field and leakage current have their maxima [4].

In this work we report on electrical properties of AlGa_N/Ga_N structure Schottky diodes grown on SiC substrate. The top AlGa_N layer was recessed to achieve different AlGa_N layer thickness, which has an influence on the induced piezoelectric charge at the AlGa_N/Ga_N interface. Investigated samples have been off-state stressed by the negative bias (–60 V) for different time (30 min, 60 min) to observe the degradation processes. From the measured I – V and C – V characteristics the basic Schottky diode parameters are extracted and the influence of the stress time and voltage level on device degradation is analysed.

2 EXPERIMENTAL

Al_{0.26}Ga_{0.74}N/Ga_N structures were grown by low-pressure metal-organic vapour phase epitaxy (LP-MOVPE). The structure is grown on a SiC substrate and consists of an AlN nucleation layer followed by 1.5 μm thick Ga_N layer and 25 nm thick Al_{0.26}Ga_{0.74}N layer, both intentionally undoped. Ohmic contacts were formed by Nb/Ti/Al/Ni/Au (20/20/100/40/50 nm) evaporation followed by rapid thermal annealing (60 s, 850 °C). The wafers were etched in RIE mode in CCl₄/He based plasma in a ROTH & RAU MICROSYS 350 machine. During etching the flow of CCl₄/He was 13.6 sccm and the working pressure 0.8 Pa. Three types of samples were investigated: 1) sample (A) virgin surface no recess, 2) sample (B) with shallow recess (~ 4 nm) and 3) sample (C) with deep recess (~ 15 nm). Finally Ni/Au (40/130 nm) Schottky gate contacts were formed at the square area of 100 μm × 100 μm.

Investigated AlGa_N/Ga_N Schottky diodes were tested for static (I – V characteristics) and high frequency (C – V characteristics at 1 MHz) performance. The samples were consecutively off-stressed under high reverse voltage (–60 V) for different times (30 min, 60 min). I – V and C – V characteristics were measured before, during and after the stress.

From I – V measurements the basic Schottky diode parameters were extracted. After all measurements the degradation mechanism and the influence of AlGa_N recessed layer thickness on electrical properties of Schottky diodes were evaluated.

* Institute of Electronics and Photonics, Faculty of Electrical Engineering and Information Technology, Ilkovičova 3, 812 19 Bratislava, Slovakia, dr.martin.florovicail.com

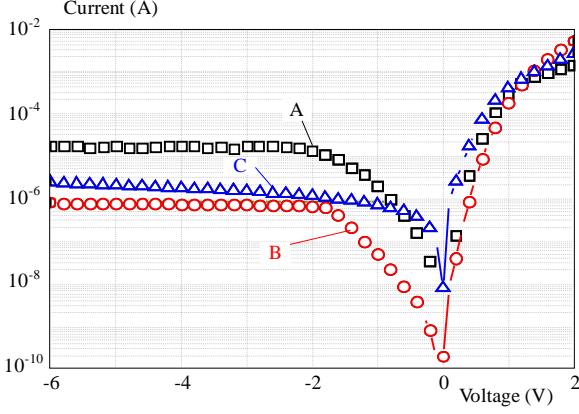


Fig. 1. I - V characteristics of virgin Schottky diodes

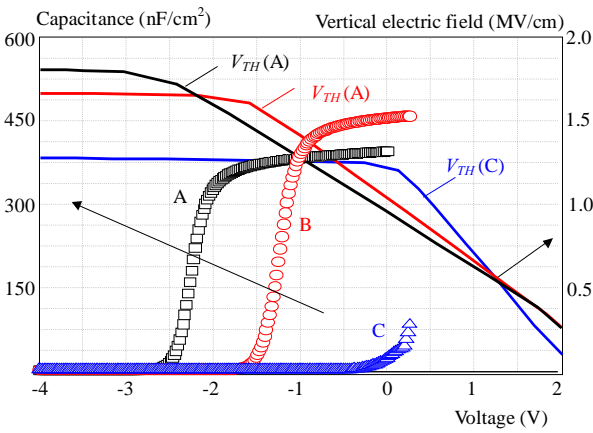


Fig. 2. G - V characteristics and simulated electric field in the middle of the Schottky diode in AlGaIn layer

3 RESULTS AND DISCUSSION

The measured I - V characteristics of non-stressed Schottky diodes are shown in Fig. 1. If the reverse voltage of the Schottky contact becomes more negative, the 2DEG charge density $\sigma_{2\text{DEG}}$ decreases because free electrons in the channel are attracted by the positive biased ohmic contact until $\sigma_{2\text{DEG}}$ becomes zero. At this point the absolute value of the electric field divergence under the Schottky contact decreases and electrons in the 2DEG leave the region under the Schottky contact. As a result the reverse current saturates and the capacitance sharply decreases as shown in Fig. 2. Technology CAD (TCAD) simulations of the vertical electric field in the middle under the Schottky contact in the top AlGaIn layer have verified this effect (Fig. 2, full lines) using the Schottky barrier height $\Phi_B \approx 1.4$ eV calculated from the measured forward I - V characteristics. A leakage path can be formed at the edge of the Schottky contact, where the lateral component of the electric field is high. For very high negative voltages additional trap states or defects near the Schottky contact (demonstrated later) can be created. When $\sigma_{2\text{DEG}}$ becomes zero along the channel, this indicates the threshold voltage (depicted in Fig. 2 for investigated samples) which can be expressed as

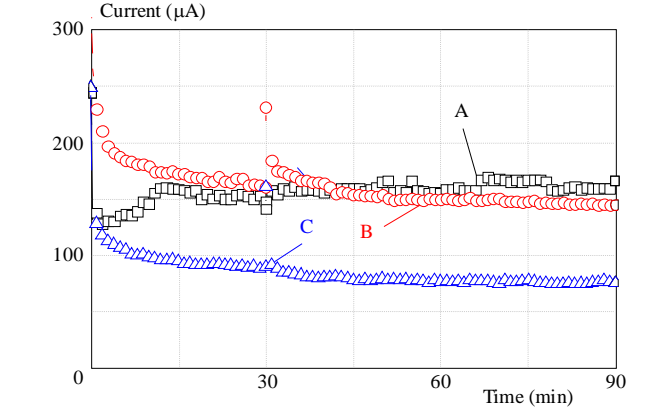


Fig. 3. Off-state reverse current *vs* stress time

$V_{\text{TH}} = (\Phi_B/q) - (\Delta E_C/q) - d(\epsilon_{\text{AlGaIn}})^{-1}(qN_Dd + \sigma(x))$. Here ΔE_C is the conduction band offset between AlGaIn and GaN, ϵ_{AlGaIn} is the dielectric constant, d is the thickness and N_D donor concentration in AlGaIn layer, $\sigma(x)$ is a polarization induced charge density in the $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ interface. Applying the gate voltage V , 2DEG concentration can be determined as $n_{2\text{DEG}} = \sigma_{2\text{DEG}}/q = \epsilon_{\text{AlGaIn}}(qd)^{-1}(V - V_{\text{TH}} - V_C - (E_F/q))$, where V_C is the potential along the channel, E_F is the Fermi level relative to the bottom of the conduction band. The Fermi level depends nonlinearly on $n_{2\text{DEG}}$, therefore it is necessary to solve the implicit function. The reverse current of sample C with the thinnest AlGaIn layer exhibits a stronger dependence on the negative voltage in comparison with samples A and B because of a relatively stronger vertical electric field in the proximity of the Schottky gate contact edge. In fact the reverse current flow through the structure depends on the presence of traps and leakage paths nearby the surface and through the AlGaIn layer. This is primarily given by the layer properties, and for GaN-based devices strongly depends on the deposition technology. When a positive voltage is applied to the Schottky contact, the space charge area is reduced and $n_{2\text{DEG}}$ increases. For a thinner AlGaIn layer (sample C) the forward current rises more rapidly. This is affected by recessed surface quality and for higher currents the serial resistance, structure defects and contact geometry uniformity play significant roles.

The reverse current *vs.* time behaviour of the investigated samples during the off-state stress for applied voltage -60 V is shown in Fig. 3. As a consequence of the negative voltage stress, device current has shown an initial decrease for samples B and C. This effect can be ascribed to the trapping of negative charge, since those traps initially empty will capture and thereby immobilize most of the injected carriers. The equilibrium trap occupancy results from a balance between the capture of electrons into the traps and their thermal emission into the conduction band.

Typically both deep and shallow traps are present in AlGaIn [6]. The immediate leakage current increase results from the electron escape from the shallow traps ex-

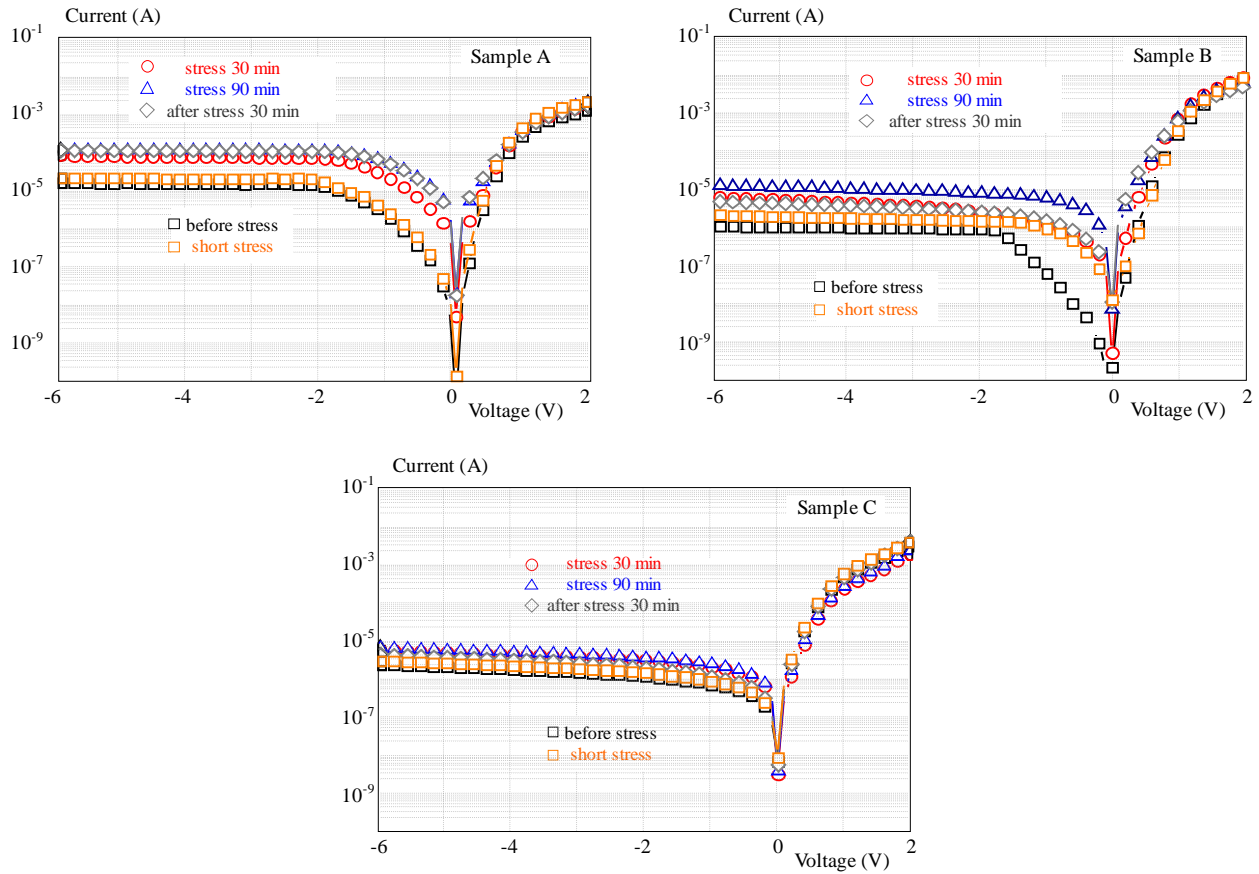


Fig. 4. I - V characteristics of stressed Schottky diodes

cept sample A, where deep traps with a longer capture time cause a slow increase of the reverse current.

The I - V characteristics measured during the stress break are compared in Fig. 4. The forward I - V characteristics measured between the off-state stresses were analysed and the Schottky barrier height changed by less than 10 %. Non-recessed sample A is the most resistant against the short time stress, which points at the deep traps presence with a long capture time. Though longer applied stress voltage fills deep traps with longer capture time and/or leakage paths are created by the stronger electric field and trap to trap hopping mechanism takes place. Electrons can be accumulated in the traps creating a virtual gate. The virtual gate formed on the surface depletes the 2DEG, on the other hand increases the vertical electric field, especially in the proximity of the Schottky contact edge, therefore the reverse current rises. In the case of structure C there is more than two-times stronger vertical electric field, therefore electric field contribution of filled traps with taking account on thin AlGa_N layer is lower in comparison to structure A, therefore off-state stress has a weaker influence on the I - V characteristics. In the case of structure B there is only a slightly stronger vertical electric field in comparison with structure A, in addition the contribution of escaped electrons from the shallow traps results in an immediate reverse current increase.

C - V characteristics measured during the stress break exhibited the same behaviour as shown in Fig. 5. The

virtual gate causes 2DEG depletion, free electrons are repelled from the Schottky gate and easier get to the positive biased ohmic contact. Therefore the threshold voltage increases. Assuming that the Schottky gate, AlGa_N layer (space charge area) and 2DEG could be presented as a capacitor with a tuneable capacitance C are in good correspondence with the well-known plan-parallel capacitor model $C = \epsilon_{\text{AlGa}_N} S_{2\text{DEG}} d^{-1}$, where $S_{2\text{DEG}}$ is the virtual area of 2DEG vertically opposite the Schottky gate electrode.

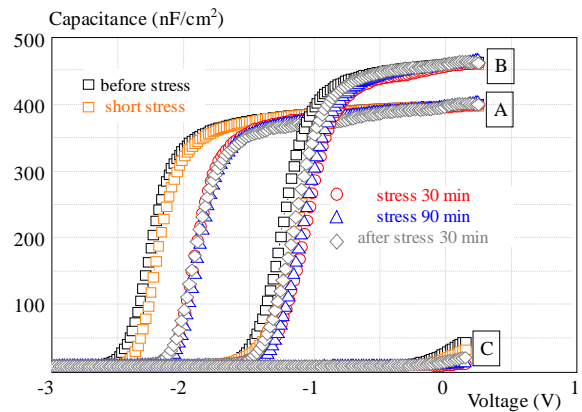


Fig. 5. C - V characteristics of stressed Schottky diodes

Capacitance maximum for the C structure was not acquired, since it has a threshold voltage near zero, where the parallel conductance rises and the space charge

area reduces under the AlGaIn layer thickness. A short stress time has an influence mainly on I - V and C - V characteristics of recessed structures. There are many traps with relatively short capture and escape times, therefore de-trapping is noticeable after the stress reverse current decreased. Non-recessed structure A exhibits only a small current resumption caused by traps with a longer escape time and leakage paths, this is caused by traps with longer escape time and leakage paths, such as crystallographic defects are partially formed and affect the device characteristics in a profound way.

4 CONCLUSION

This article deals with the I - V and C - V characteristics of recessed and non-recessed Al_{0.26}Ga_{0.74}In/GaN Schottky diodes investigated before, between and after the off-state stress for the applied voltage -60 V. Non-stressed samples show the threshold voltage of -2.2 V(A), -1 V(B) and 0 V(C) confirmed by TCAD simulations and analytical equations. The equilibrium trap occupancy results from a balance between the capture of electrons into the traps and their thermal emission (escape) into the conduction band. Shallow or deep recessed samples (B, C) are relatively less resistant against the short time stress caused by traps with longer capture and escape times. This results in slight current resumption, therefore a short stress time has an influence mainly on the I - V and C - V characteristics of recessed structures. During the off-state stress electrons can accumulate in traps creating a virtual gate resulting in a threshold voltage shift to more positive values. The maximum of the Schottky diode capacitance is in good correspondence with a plan-parallel capacitor model.

Acknowledgement

The authors would like to thank T. Lalinský and G. Vanko for sample preparation. This work was financially supported by the Scientific Grant Agency of the Ministry of Education of the Slovak Republic (grants 1/0866/11 and 1/0439/13).

This paper summarizes in brief the essential issues of a work presented at ADEPT-2014, Advances in Electronics and Photonic Technologies, an international conference held in Tatranska Lomnica, High Tatras, Slovakia, on 1-4 June 2014.

REFERENCES

- [1] AMBACHER, O.—SMART, J.—SHEALY, J. R.—WEIMANN, N. G.—CHU, K.—MURPHY, M.—SCHAFF, W. J.—EASTMAN, L. F.—DIMITROV, R.—WITTMER, L.—STUTZMANN, M.—RIEGER, W.—HILSENBECK, J.: Two-Dimensional Electron Gases Induced by Spontaneous and Piezoelectric Polarization Charges in N- and Ga-Face AlGaIn/GaN Heterostructures, *Journal of Appl. Phys.* **85** No. 6 (1999), 3222–3233.
- [2] ALAMO, J. A.—JOH, J.: GaN HEMT Reliability, *Microel. Rel.* **49** (2009), 1200–1206.
- [3] DOUGLAS, E. A.—CHANG, C. Y.—CHENEY, D. J.—GILA, B. P.—LO, C. F.—LIU, L.—HOLZWORTH, R.—WHITING, P.—JONES, K.—VIA, G. D.—KIM, J.—JANG, S.—REN, F.—PEARTON, S. J.: AlGaIn/GaN High Electron Mobility Transistor Degradation under On- and Off-State Stress, *Microel. Rel.* **51** (2011), 207–211.
- [4] KARBOYAN, S.—TARTARIN, J. G.—RZIN, M.—BRUNEL, L.—CURUTCHET, A.—MALBERT, N.—LABAT, N.—CARISSETTI, D.—LAMBERT, B.—MERMOUX, M.—ROMAINLATU, E.—THOMAS, F.—BOUEXIERE, C.—MOREAU, C.: Influence of Gate Leakage Current on AlGaIn/GaN HEMTs Evidenced by Low Frequency Noise and Pulsed Electrical Measurements, *Microel. Rel.* **53** (2013), 1491–1495.
- [5] ANWAR, A. F. M.—FARACLAS, E. W.: Schottky Barrier Height in GaN/AlGaIn Heterostructures, *Solid-State Electr.* **50** (2006), 1041–1045.
- [6] GOSWAMI, A.—TREW, R. J.—BILBRO, G. L.: Physics Based Modeling of Gate Leakage Current due to Traps in AlGaIn/GaN HFETs, *Solid-State Electr.* **80** (2013), 23–27.

Received 15 June 2014

Martin Florovič (Ing, PhD) was born in Bratislava, Slovakia, in 1978. He graduated from the FEI STU, Bratislava in 2003, then he has been working in the research of optoelectronic devices technology at the Department of Electronics and Photonics of FEI STU where he received a PhD degree in 2006 he is involved in electrical and optical characterization of III-V based electronic devices.

Jaroslav Kováč (Prof, Ing, PhD) was born in Tornala, Slovakia, in 1947, graduated from the Slovak University of Technology, Faculty of Electrical Engineering and Information Technology (FEI STU), Bratislava, in 1970. Since 1971 he has been with the Microelectronics Department of FEI STU. He received a PhD degree (1983), professor degree (2001) at STU Bratislava, since 1991 being the leader of the Optoelectronic group at the Institute of Electronics and Photonics.

Peter Benko (Ing, PhD) was born in Šurany, Slovakia, in 1981. He received the master's degree and the PhD degree in microelectronics from FEI STU, Bratislava, in 2005 and 2009, respectively. Currently is a Research Fellow with the Institute of Electronics and Photonics of FEI STU with research interests in electrical characterization of Si- and GaN-based electronic devices for high power and high-frequency applications and study of their reliability and long term stability.

Aleš Chvála (Ing, PhD) received the MSc and PhD degrees in electronics from the Slovak University of Technology, Bratislava, Slovakia, in 2005, and 2009. He has been a Researcher with the Institute of Electronics and Photonics, STU, since 2007 and research interests in the TCAD and SPICE electrothermal modelling of Si and GaN-based devices.

Peter Kordoš (Doc, Ing, DrSc) graduated from the FEI STU, Bratislava, in 1963. During his 29-year career at the Institute of Electrical Engineering, Slovak Academy of Sciences (IEE SAS), he worked in a wide variety of problems related to III-V technology and devices. From 1991 he was with Research Centre Jlich, Germany, dealing with microelectronic and optoelectronic devices and sensors. Since 2004 he is with FEI STU and IEE SAS, working on GaN-based devices.

Jaroslava Škriniarová (Ing, CSc) received her Ing (MSc) and CSc degree from the Slovak University of Technology (STU), Bratislava, in 1977 and 1986. In 1993 she joined the Microelectronics Department of STU, at present she is there engaged in the research of optoelectronic devices. Her interests include chemical processing of semiconductor materials, thin films and surfaces.