

CAPACITANCE ANALYSIS OF THE STRUCTURES WITH THE a-Si:H(i)/c-Si(p) HETEROJUNCTION FOR SOLAR-CELL APPLICATIONS

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In this paper we present the capacitance study of the intrinsic amorphous silicon/crystalline silicon heterostructure with the aim to gain insight on the heterointerface properties of a passivated silicon heterojunction solar cell. It is shown that due to the high density of defect states in the amorphous layer the structure has to be analyzed as a heterojunction. Using the analysis, the following values have been determined: conduction-band offset of 0.13 eV, electron affinity of 3.92 eV, and density of defect states in the intrinsic amorphous silicon being that of $4.14 \times 10^{21} \text{m}^{-3}$.

Key words: capacitance-voltage measurements, a-Si:H(i)/c-Si(p) heterojunction, Si heterojunction solar cells

1 INTRODUCTION

The concept of solar cells with amorphous and crystalline silicon (a-Si:H/c-Si) heterojunction was first time proposed by Fuhs *et al* in 1974 [1], and first time fabricated in the group of Hamakawa *et al* [2], in 1985. Since then a number of laboratories have been formed which were involved in the development of this solar-cells technology. The main research motivation is the potential of high efficiency volume cells and their low production costs, typical for the thin-film cells technology.

The absorption layer of such cells is a thin silicon substrate, making it possible to achieve high efficiency and stability during illumination. The emitter is prepared by deposition of amorphous silicon at temperatures around 200 °C resulting in cost savings in production. An important assumption for high efficiency of a solar cell with an a-Si:H/c-Si heterojunction is a good interface with a low concentration of surface states. For the purpose of reducing the surface states, a thin layer of intrinsic amorphous silicon (a-Si:H(i)) which acts as the passivation, is deposited on the interface. The potential of this technology has been best utilized by the SANYO company which, using their solar cell technology with the a-Si:H/c-Si heterojunction called HIT (Heterojunction with Intrinsic Thin layer), achieved record-breaking efficiency of 24.7% [3]. However, despite the commercialization of this solar-cells technology, the physical principle of the processes on the heterojunction is still insufficiently understood. It is therefore necessary to focus on the a-Si:H/c-Si heterojunction and learn to analyze it by diagnostic techniques. By introducing an intrinsic intermediate layer of amorphous silicon, an a-Si:H(n)/a-Si:H(i)/c-Si(p) structure is obtained. To understand the processes at the a-Si:H/c-Si heterojunction and their modelling, it is also necessary to

observe both the properties of the a-Si:H(i)/c-Si(p) interface as well as the properties of the intrinsic amorphous silicon of such a structure.

2 EXPERIMENTAL

In order to examine the a-Si:H(i)/c-Si(p) interface, a-Si:H(i)/c-Si(p) heterostructures have been prepared. Using the PECVD technique, a 950 nm thick layer of intrinsic amorphous silicon was deposited onto the crystalline silicon substrate of 525 μm thickness, with $\langle 111 \rangle$ orientation, p-type dotation and impurity concentration of $1.6 \times 10^{21} \text{m}^{-3}$ (measured by a four-point probe). Before depositing the amorphous silicon, the silicon substrate was cleansed in diluted hydrofluoric acid (HF). The amorphous silicon was prepared at the Laboratory of photovoltaic materials and devices, TU Delft – Dimes, Netherlands. A full-area aluminum contact of 120 nm thickness was evaporated on the back side of the crystalline silicon. The gates of the structures with $500 \times 500 \mu\text{m}$ dimensions were prepared using standard photolithography, followed by lift-off patterning of the evaporated 120 nm thick aluminum layer.

The $C - V$ diagnostics of the a-Si:H(i)/c-Si(p) heterostructure has been realized at room temperature in the dark by using the Agilent LCR Meter 4284A operated by the CV Measure service program. The current-voltage measurements have been made at room temperature in the dark by using the Keithley 237 equipment operated by the DCATS software.

2.1 Capacitance-voltage measurements

The studied Al/a-Si:H(i)/c-Si(p)/Al heterostructure with 950 nm thick intrinsic amorphous silicon is com-

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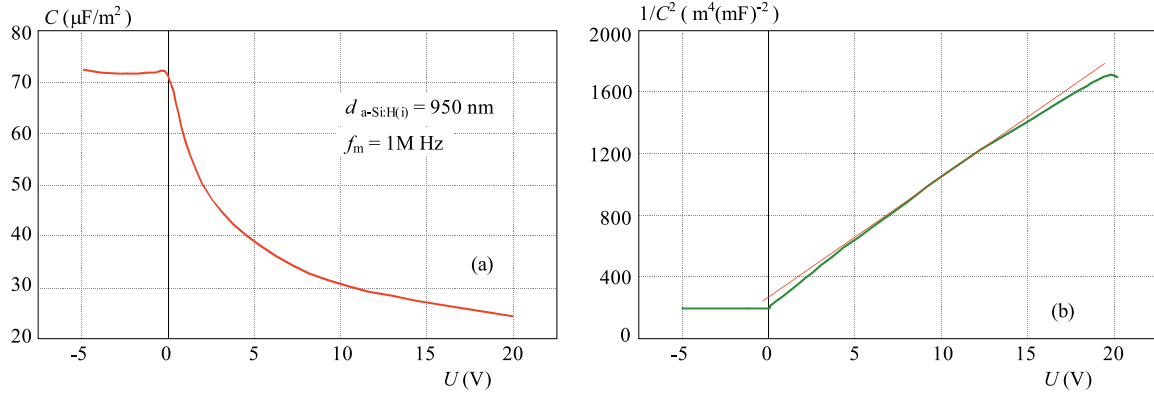


Fig. 1. (a) – typical measured C – V curve of the test a-Si:H(i)/c-Si(p) heterostructure, (b) – $1/C^2$ – V dependence of the a-Si:H(i)/c-Si(p) heterostructure. Abnormality of the C – V curve of the investigated MOS structure can be observed in both graphs

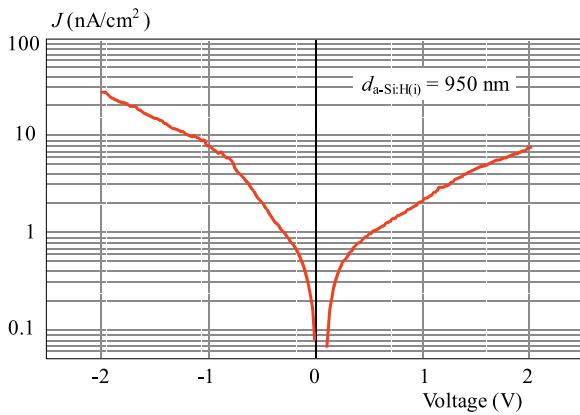


Fig. 2. Leakage currents measured on the a-Si:H(i)/c-Si(p) heterostructure. Due to high leakages it is not possible to investigate this structure as an MOS structure

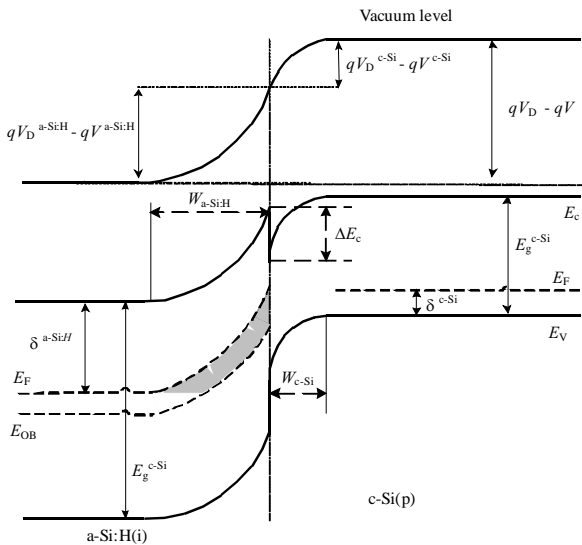


Fig. 3. Energy band diagram of the a-Si:H(i)/c-Si(p) heterostructure at reverse bias voltage. Grey colour indicates defect states located under the Fermi level which act as donor states

positionally close to an MOS structure with imperfect high- κ dielectric. Based on the resistance of the intrinsic amorphous silicon, which is of the order of $\rho_{a-Si:H} = 10^9 \Omega\text{cm}$, we get the dielectric relaxation time of $t_{\text{diel}} =$

$\rho_{a-Si:H} \epsilon_{a-Si:H} \epsilon_0 \sim 10^{-3} \text{ s}$, and the frequency defined by $1/2\pi t_{\text{diel}}$ equal to 160 Hz. Based on this we may consider the intrinsic amorphous silicon as a dielectric material for C – V measurements with the AC frequency of the measured signal greater than the given frequency. Therefore, we first considered the given structure as an MOS structure. Looking at the C – V curve of the testing heterostructure a-Si:H(i)/c-Si(p) sample measured by the AC signal with the frequency of 1 MHz (Fig. 1a), we observe deviations compared to the projected C – V dependence of an MOS structure with a gate dielectric. Firstly, it is an atypically sharp change of the C – V curve in its transition to the accumulation regime. Also, in the deep depletion regime we did not register any hysteresis, being a condition for the strong inversion regime. When this C – V curve is redrawn into the $1/C^2$ – V form, we observe its nonlinear behaviour what prevents us from analyzing it as an MOS structure (Fig. 1b). The reason for this atypical behaviour of the C – V curve is the presence of the intrinsic amorphous silicon acting as an oxide layer of such MOS structure, forming in this case an imperfect dielectric with a high density of defect states.

Moreover, the amorphous silicon used as a dielectric layer causes large leakage currents (Fig. 2). Amorphous silicon contains a significant amount of defect states which can be charged and discharged. Consequently, the space-charge region (SCR) spreads also into the amorphous silicon and the MOS structure in this case acts as a heterostructure.

In this regard it is more suitable to analyze the examined structure in terms of a heterostructure. In the case of a heterostructure it is assumed that when reverse bias voltage is applied, the SCR would spread into the crystalline and amorphous silicon. On the side of the crystalline silicon the space charge in the SCR is formed by negatively charged ionized acceptors with the concentration equal to that of the impurities. To meet the assumption that the structure will behave as an np heterostructure, it is necessary that the SCR on the side of the amorphous silicon is negatively charged. The origin of this charge may be explained by the existence of a large number of defect states in the forbidden gap of

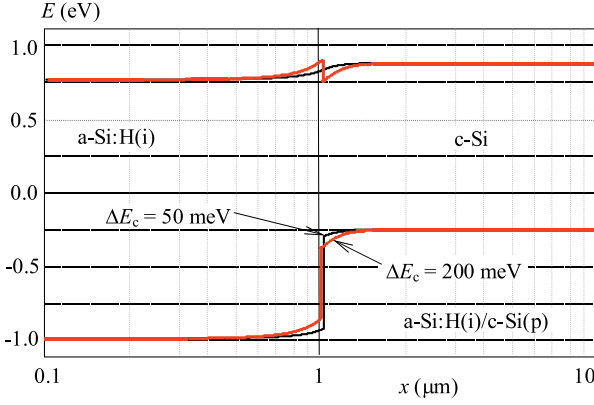


Fig. 4. Energy band diagram of the a-Si:H(i)/c-Si(p) heterojunction. Due to the presence of undoped amorphous silicon, the inversion layer at the interface is not created

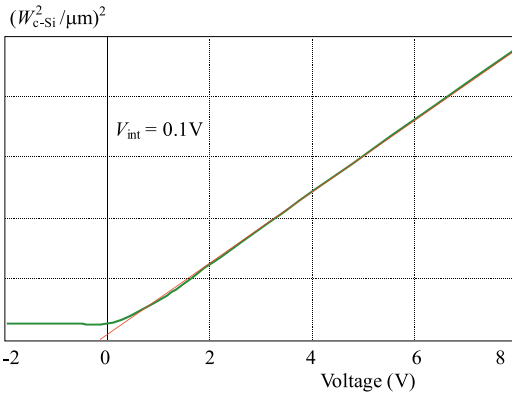


Fig. 5. Voltage dependence of the square of the width of the SCR on the side of the crystalline silicon of the investigated a-Si:H(i)/c-Si(p) heterostructure

the amorphous silicon. As can be seen in Fig. 4, in the bulk part of the amorphous silicon the traps located under the Fermi level are occupied by electrons. Applying reverse bias voltage on the structure results in the shift of the Fermi level followed with emission of these electrons. Energetical states above the energy level E_{OB} are those states with missing electrons. The energy E_{OB} is given by electron and hole emission rates from the defect states in the forbidden gap and is defined as [10]

$$E_{OB} = E_V + E_g^{a-Si:H} + \frac{kT}{2} \ln \frac{v_p}{v_n} \quad (1)$$

where $E_g^{a-Si:H}$ is the forbidden gap of the amorphous silicon, v_p and v_n are the frequencies of the emission and recombination for the electrons and holes, respectively.

Since the difference between the bulk part of the amorphous silicon and the fraction in the SCR is in the occupancy of the defect states by the electrons (indicated in Fig. 4 in gray colour), these states behave as positively charged, *ie*, as donor states. Let us denote their concentration as N_I . The mentioned states lay between the energy E_{OB} and the Fermi level situated in intrinsic amorphous silicon approximately in the middle of the

forbidden gap, and thus represent the density of states in the middle of the forbidden gap of intrinsic amorphous silicon.

Before analyzing the a-Si:H(i)/c-Si(p) structure as a heterostructure, it is first important to inspect the possible presence of the inversion layer at the heterointerface. As was shown by Gudovskikh *et al* [4], due to the presence of the inversion layer on the a-Si:H(n)/c-Si(p) heterostructure, it is not possible to determine the diffusion voltage from the $C-V$ measurement of such structure. Therefore, we carried out the simulation study using the ASA program to confirm or reject the presence of inversion layer in the studied samples. For simulation we have chosen parameters of the amorphous silicon taken from the literature [5]. The simulated band diagram of the a-Si:H(i)/c-Si(p) heterostructure is shown in Fig. 4. It can be observed that due to the intrinsic nature of the amorphous silicon, the inversion layer at the a-Si:H(i)/c-Si(p) interface is not created, and thus the $C-V$ measurements can be used for determination of certain parameters of the examined heterojunction.

3 RESULTS AND DISCUSSION

3.1 Determination of defect states density in the a-Si:H(i)

When analyzing the $C-V$ curves and considering the heterojunction character of a-Si:H(i)/c-Si(p) structures, it is necessary to come out from the Anderson's model for heterostructures [6], thanks to which one can determine (except the conduction band offset of the a-Si:H(i)/c-Si(p) heterojunction) also the density of defect states in the middle of the band gap of the intrinsic amorphous silicon, [7].

As shown in Fig. 1b, the $1/C^2$ -Voltage curve does not have a linear behaviour; that is why it is not possible to analyze it by the line approximation. For the needs of the $C-V$ measurement analysis, it is necessary first to express the width of the SCR as a function of voltage. For the SCR on the side of the crystalline silicon we may write

$$W_{c-Si} = \left[\frac{2\varepsilon_0\varepsilon_{c-Si}}{qN_A} (V_D^{c-Si} - V^{c-Si}) \right]^{1/2}, \quad (2)$$

and on the side of the amorphous silicon

$$W_{a-Si:H} = \left[\frac{2\varepsilon_0\varepsilon_{a-Si:H}}{qN_I} (V_D^{a-Si:H} - V^{a-Si:H}) \right]^{1/2}, \quad (3)$$

where V_D^{c-Si} and $V_D^{a-Si:H}$ are diffusion voltages in crystalline and amorphous silicon, while V^{c-Si} and $V^{a-Si:H}$ are drops of potential at the SCR on the side of the crystalline and amorphous silicon, respectively. At the same time it may be written

$$qN_A W_{c-Si} = qN_I W_{a-Si:H}. \quad (4)$$

The total measured capacitance of the structure is expressed by

$$\frac{1}{C} = \frac{1}{C^{c-Si}} + \frac{1}{C^{a-Si:H}}. \quad (5)$$

With respect to the dielectric relaxation time of the crystalline silicon being in the order of 10^{-12} s, the capacitance on the side of the crystalline silicon, C^{c-Si} , is expressed as

$$C^{c-Si} = \frac{\varepsilon_{c-Si}\varepsilon_0}{W_{c-Si}}. \quad (6)$$

Amorphous silicon can be considered as dielectric, so the capacitance on the side of the amorphous silicon may be expressed as

$$C^{a-Si:H} = \frac{\varepsilon_{a-Si:H}\varepsilon_0}{d_{a-Si:H}}, \quad (7)$$

where $d_{a-Si:H}$ is the thickness of the intrinsic amorphous silicon. From the Equations (2), (3) and (4) we may subsequently write

$$\frac{V_D^{c-Si} - V^{c-Si}}{V_D^{a-Si:H} - V^{a-Si:H}} = \frac{\varepsilon_{a-Si:H}\varepsilon_0 N_I}{\varepsilon_{c-Si}\varepsilon_0 N_A}, \quad (8)$$

and for the width of the SCR in the region of the crystalline silicon we may (using (2), (5), (6) and (8)) express the formula for the width of the depletion region on the side of the crystalline silicon

$$W_{c-Si}^2 = \left(\varepsilon_{c-Si}\varepsilon_0 \left(\frac{1}{C} - \frac{1}{C^{a-Si:H}} \right) \right)^2 = \frac{2\varepsilon_0^2 \varepsilon_{c-Si} \varepsilon_{a-Si:H}}{q N_A (N_A \varepsilon_0 \varepsilon_{c-Si} + N_I \varepsilon_0 \varepsilon_{a-Si:H})} (V_D - V), \quad (9)$$

where $V_D = V_D^{a-Si:H} + V_D^{c-Si}$ is the total diffusion voltage of the heterostructure and $V = V^{a-Si:H} + V^{c-Si}$ is the applied voltage. Using (9) for the measured C - V curve we may plot the dependence of the square of the width of the SCR on the side of the crystalline silicon on the applied voltage (see Fig. 5).

The dependence is of linear behaviour which enables us to estimate its slope

$$S = \frac{dW_{c-Si}^2}{dV} = \frac{2\varepsilon_0^2 \varepsilon_{c-Si} \varepsilon_{a-Si:H}}{q N_A (N_A \varepsilon_0 \varepsilon_{c-Si} + N_I \varepsilon_0 \varepsilon_{a-Si:H})} \quad (10)$$

and subsequently, after an arithmetical modification, we get the value of the density of defect states located in the middle of the forbidden gap of the intrinsic amorphous silicon, $N_I = 4.14 \times 10^{21} \text{ m}^{-3}$. This value is in good agreement with the value for the density of "dangling bonds" defect states located in the middle of the forbidden gap for the intrinsic amorphous silicon, $N_I = 5 \times 10^{21} \text{ m}^{-3}$ [5].

3.2 Determination of the conduction band offset at the a-Si:H(i)/c-Si(p) heterojunction

The C - V measurements enable us to estimate the value of the diffuse voltage, thanks to which one may find the band offset value of the heterojunction. In the case of

the investigated samples with the a-Si:H(i)/c-Si(p) heterojunction, the value of the diffuse voltage may be determined by using Equation 9 which represents a linear equation. The intersection of linear approximation of W_{c-Si}^2 - V curve with the x axis equals to the value of the diffusion voltage. The assumption in (9) is valid only under depletion approximation, which means that presence of the free charge carriers in the SCR may be neglected. In order to improve the precision of the conduction band offset determination it is necessary to consider also the presence of the electrons at the interface of the depleted and neutral region in the crystalline silicon [8]. However, in the case of a-Si:H(i)/c-Si(p) heterostructure due to intrinsic nature of amorphous silicon, the presence of the free carriers may be neglected, and thus the Equation 9 gets the following form

$$W_{c-Si}^2 = \left(\varepsilon_{c-Si}\varepsilon_0 \left(\frac{1}{C} - \frac{1}{C^{a-Si:H}} \right) \right)^2 = \frac{2\varepsilon_0^2 \varepsilon_{c-Si} \varepsilon_{a-Si:H}}{q N_A (N_A \varepsilon_0 \varepsilon_{c-Si} + N_I \varepsilon_0 \varepsilon_{a-Si:H})} \left(V_D - \frac{kT}{q} - V \right). \quad (11)$$

From Fig. 5 then we will get for the diffusion voltage the value of $qV_D = 0.13$ eV. Consequently, after considering the distance of the bottom edge of the conduction band level and the Fermi level in intrinsic amorphous silicon $\delta_{a-Si:H} = 0.87$ eV, and the width of the forbidden gap of crystalline silicon $E_{c-Si} = 1.12$ eV, and after substituting these values into

$$\Delta E_C = \delta_{a-Si:H} + \delta_{c-Si} + qV_D - E_g^{c-Si}, \quad (12)$$

we obtain the conduction band offset equal $\Delta E_C = 0.13$ eV. This value corresponds with the observations made by Matsuura *et al* [9] on related a-Si:H(i)/c-Si(p) heterostructures.

When we take into account the electron affinity of crystalline silicon $\chi_{c-Si} = 4.05$ eV, then following the relation coming out from Anderson's model for heterostructure

$$\Delta E_C = \chi_{c-Si} - \chi_{a-Si:H} \quad (13)$$

we obtain for the electron affinity of intrinsic amorphous silicon the value $\chi_{a-Si:H} = 3.92$ eV. The measured value of the electron affinity is close to the value $\chi_{a-Si:H} = 3.93$ eV, which was published in the work of Matsuura *et al* [9].

4 CONCLUSIONS

In this paper we have studied the a-Si:H(i)/c-Si(p) heterostructure with the aim to determine the band offset at the heterointerface and the defect states in the amorphous silicon layer. Due to the presence of a large concentration of defect states in a-Si:H(i), in such structures the SCR spreads also into the intrinsic amorphous silicon, which calls for analyzing the structure as a heterostructure. The intrinsic nature of the amorphous silicon, or the position of its Fermi level in the middle of the forbidden band,

keeps from creation of the inverse layer in the heterostructure and enables us to apply the C - V diagnostics. Analyzing the C - V curves by means of determining the width of the SCR on the side of the crystalline silicon as a function of voltage, allowed us to determine the density of states in the vicinity of the middle of the forbidden gap of the amorphous silicon as being that of $N_I = 4.14 \times 10^{21} \text{m}^{-3}$. From the intersection point of the linear approximation of the $W_{c-Si}^2 - V$ curve we have found out the diffusion voltage of the structure and subsequently determined the magnitude of the conduction band offset to be that of $\Delta E_C = 0.13 \text{ eV}$. Taking into account the electron affinity of the crystalline silicon $\chi_{c-Si} = 4.05 \text{ eV}$, we may estimate the electron affinity of the intrinsic amorphous silicon $\chi_{a-Si:H} = 3.92 \text{ eV}$. The obtained values enable better modelling of the processes at the a-Si:H(n)/a-Si:H(i)/c-Si(p) heterostructures for the solar applications.

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REFERENCES

- [1] FUHS, W.—NIEMANN, K.—STUKE, J.: Heterojunctions of Amorphous Silicon & Silicon Single Crystals, In: Intern. Conference, Tetrahedrally Bonded Amorphous Semiconductors, Yorktown Hts., NY, vol. 20, 1974, pp. 345–350.
- [2] HAMAKAWA, Y. *et al.*: New Types of High Efficiency Solar Cells based on a-Si, *Applied Physics Letters* **43** (1983), 644–646.
- [3] YANO, A.—TOHODA, S.—MATSUYAMA, K. *et al.*: 24.7% Record Efficiency HIT(r) Solar Cell on Thin Silicon Wafer, In: 28th European Photovoltaic Solar Energy Conference and Exhibition: Proceedings, Paris, France 30.9–4.10 2013, München: WIP, 2013.
- [4] GUDOVSKIKH, A. S.—IBRAHIM, J.—KLEIDER, J. *et al.*: Determination of Band Offsets in a-Si:H/c-Si Heterojunctions from Capacitance-Voltage Measurements: Capabilities and Limits, *Thin Solid Films* **515** No. 19 (2007), 7481–7485.
- [5] SCHROPP, R.—ZEMAN, M.: *Amorphous and Microcrystalline Silicon Solar Cells: Modeling, Materials and Device Technology*, Kluwer Academic Publishers, 1998.
- [6] ANDERSON, R.: Experiments on Ge-GaAs Heterojunctions, *Solid-State Electronics* **5** No. 5 (1962), 341–351.
- [7] MATSUURA, H.: Hydrogenated Amorphous-Silicon/Crystalline-Silicon Heterojunctions: Properties and Applications, *Electron Devices, IEEE Transactions on Electron Devices* **36** No. 12 (1989), 2908–2914.
- [8] SZE, S. M.—KWOK, K. N.: *Physics of Semiconductor Devices*, John Wiley & Sons, New Jersey, 2007.
- [9] MATSUURA, H.—OKUNO, T.—OKUSHI, H.—TANAKA, K.: Electrical Properties of n-Amorphous/p-Crystalline Silicon Heterojunctions, *Journal of Applied Physics* **55** No. 4 (1984), 1012–1019.
- [10] MATSUURA, H.: *Electrical Properties of Amorphous/Crystalline Semiconductor Heterojunctions and Determination of Gap-State Distributions in Amorphous Semiconductors*, Dissertation, Kyoto University, Japan 1994.

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