# ASSEMBLING A FORMULA FOR CURRENT TRANSFERRING BY USING A SUMMARY GRAPH AND TRANSFORMATION GRAPHS 

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#### Abstract

This paper deals with the symbolic solution of the switched current circuits. As is described, the full graph method of the solution can be used for finding relationships expressing current transfer, too. The summa MC-graph is constructed using two-graphs method in two-phase switching. By comparing the matrix form with results of the Mason's formula are derived relations for current transfers in all phases. There are discussed various options described transistor memory cells - with loss and lossless transistors and normal transistor current mirror. Evaluation of the graph is simplified if we consider the lossless transistors or if the $y_{21}$-parameter of one transistor is alpha multiple of second ones.


Keywords: switched current, two phases, two-graph, Mason's formula, relations for current transfer, summary MCgraph

## 1 INTRODUCTION

A switched-current (SI) system is defined as a system using analogue sampled-data circuits in which signals are represented by a current samples [1]. The basic building block of SI circuits is the current memory cell [2]. This can be described by the equation of time domain or by the $z$-transform of the operator $z$-domain. Current memory cell can be represented by graph, too.

Graph methods give results in a symbolic form [3, 4] which makes it can be used to finding general relations. One option is to find general relations for current transfer in switched current circuits in two-phase switching. General relations are used for the calculation method of matrix calculus of final solution. This method will be demonstrated in the example. The summa MC-graph is constructed using the transformation-graphs method [5], in two-phase switching, transformation-graphs method for switched capacitor circuits is described in [6] where the resulting relationship is in the shape of the matrix [7].

## 2 CALCULATION OF THE TRANSMISSIONS FROM THE SUMMARY GRAPH

A circuit with a switched current has got for example the schematic wiring diagram shown in Fig. 1, eg [1, 2]. This circuit consist of two capacitors $C$, and three field effect transistors $T_{1}, T_{2}$ and $T_{3}$, where $T_{1}$ is lossless transistor. Phases of the switching are marked as odd and even, not 1 and 2 , which could lead to confusion with the numbering of nodes and phases.

A solution of a circuit by the described method of a summary MC-graph [8] constructed on the transformation graphs [5] will be shown by solving a circuit with three field effect transistors and two capacitors, whose wiring diagram is shown in Fig. 1. The phases are marked as odd ( O ) and even ( E ) because numbered are the nodes.

The field effect transistor is described by the equation $I_{D}=y_{21} V_{G}+y_{22} V_{D}$, this equation can be rewritten in the following form $y_{22} V_{D}=-y_{21} V_{G}+I_{D}$, if $I_{D}=0$ then $y_{22} V_{D}=-y_{21} V_{G}$. The graph representation of this equation [9] is in Fig. 2: The left side of the equation $y_{22} V_{D S}$ represents the own loop of the node $D$ with the transfer $y_{22}$, the right side branch going from the node $G$ to the node $D$ has the transition $y_{21}$. The lossless FET is described by the equation $I_{D}=y_{21} V_{G}$, it means in the graph representation will be one branch going from the node $G$ to the node $D$ with the transfer $y_{21}$ only.

The circuit in Fig. 1 has four nodes, therefore the starting graph of the circuit in Fig. 3 has also four nodes. Full-graph solution is following:


Fig. 1. Schematic diagram of the SI circuit from the solution


Fig. 2. MC-graph of the equation $y_{22} V_{D}=-y_{21} V_{G}$

Drain $D$ of the transistor $T_{1}$ is connected to the node 1 , gate $G$ to the node 2 . Therefore, the transis-

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Fig. 3. Transformation graphs for EE, OO, EO and OE phases


Fig. 4. The summary extended MC-graph
tor $T_{1}$ is represented by the branch $-y_{21}^{(1 .)}$ from node 2 to node 1 and its inherent loop $y_{22}^{(1 .)}$ at the first node. Drain $D$ of the transistor $T_{2}$ is connected to the node 1, gate $G$ to the node 3 . Therefore, the transistor $T_{2}$ is represented by the branch $-y_{21}^{(2 .)}$ from node 3 to node 1 and its inherent loop $y_{22}^{(2 .)}$ at the first node.

The branch between the nodes 3 and 1 with the transfer $-y_{21}^{(2 .)}$ is transformed to the inherent loop with the transfer $y_{21}^{(2 .)}$, because in the relation $a_{I} \tilde{y} a_{V} \alpha=y$ now $\alpha=-1$, as the branch of the original graph converts to the inherent loop in the resulting transformed graph. The inherent loop with the transfer $y_{22}^{(1 .)}+y_{22}^{(2 .)}$ is transformed to the inherent loop, too. Because now $\alpha=1$, the transfer is $y_{22}^{(1 .)}+y_{22}^{(2 .)}$, too. Therefore, the resulting transfer of its inherent loop is $y_{22}^{(2 .)}+y_{21}^{(2 .)}$.

The summary MC-graph is obtained from the partial transformed graphs from the Fig. 3 and is shown in Fig. 4.

First, the results of the transformed graphs for EE and OO phases are plotted as nodes with the inherent loops with transfers $y_{22}^{(2 .)}+y_{21}^{(2 .)}, y_{22}^{(3 .)}, y_{22}^{(2 .)}+y_{21}^{(1 .)}$ and $y_{22}^{(3 .)}$ and one branch with transfer $-y_{21}^{(3 .)}$.

In the next step, the results of the transformed graph for the OE and EO phases multiplied by $\pm z^{-\frac{1}{2}}$ are then drawn between these nodes as branches, ie the branch with the transfer $z^{-\frac{1}{2}}\left(-y_{21}^{(3 .)}\right)$ between the nodes 1 E and 2 O , the branch with the transfer $-z^{-\frac{1}{2}} y_{21}^{(2 .)}$ between the nodes 1 E and 1 O , and the branch with the transfer $-z^{-\frac{1}{2}} y_{21}^{(1 .)}$ between the nodes 1 O and 2 E .

The current transfer $\frac{I_{4 E}}{I_{1 E}}$ will now be obtained from an extended graph, ie a graph must be extended to two
branches: the first branch from the input node IINP $\left(I_{I N P}=I_{1 E}\right)$ to the node 1 E with transfer 1 and the second branch from the node 2 E to the node $I_{\text {OUT }}$ $\left(I_{4 E}=I_{O U T}\right)$. The transfer is equal to the transmission of its own loop at the output node 2E, i.e. $y_{22}^{(3 .)}[6]$. The summary MC-graph is now evaluated by means of the Mason's rule [3], the current transfer $\frac{I_{4 E}}{I_{1 E}}$ is (1).

$$
\begin{align*}
\frac{I_{O U T}}{I_{I N P}}= & \frac{I_{4 E}}{I_{1 E}}=\frac{\sum p_{(i)} \Delta_{(i)}}{V-\sum S^{(K)} V^{(K)}}= \\
& 1\left(-y_{21}^{(3 .)}\right) y_{22}^{(3 .)}\left(y_{22}^{(2 .)}+y_{21}^{(1 .)}\right) y_{22}^{(3 .)} \times \\
& 1 /\left(\left(y_{22}^{(2 .)}+y_{21}^{(2 .)}\right) y_{22}^{(3 .)}\left(y_{22}^{(2 .)}+y_{21}^{(1 .)}\right) y_{22}^{(3 .)}\right. \\
& \left.-z^{-\frac{1}{2}} y_{21}^{(2 .)} z^{-\frac{1}{2}} y_{21}^{(1 .)} y_{22}^{(3 .)} y_{22}^{(3 .)}\right) \\
= & \frac{-y_{21}^{(3 .)}\left(y_{22}^{(2 .)}+y_{21}^{(1 .)}\right)}{\left(y_{22}^{(2 .)}+y_{21}^{(2 .)}\right)\left(y_{22}^{(2 .)}+y_{21}^{(1 .)}\right)-z^{-1} y_{21}^{(2 .)} y_{21}^{(1 .)}} \tag{1}
\end{align*}
$$

## 3 MATRIX DESCRIPTION

The linearized diagram of the circuit from the Fig. 1. is drawn in Fig. 5 and can be described by nodal admittance formulation by matrix (2).

$$
\begin{gather*}
V_{1 E}: \\
I_{1 E}:  \tag{2}\\
I_{2 E}: \\
I_{1 O}: \\
I_{2 O}:
\end{gather*}\left[\begin{array}{cc|cc}
y_{22}^{(2 .)}+y_{21}^{(2 .)} & 0 & V_{1 O}: & V_{2 O}: \\
y_{21}^{(3 .)} & y_{22}^{(3 .)} & 0 & 0 \\
\hline z^{-\frac{1}{2}} y_{21}^{(2 .)} & 0 & y_{21}^{(1 .)} & 0 \\
z^{-\frac{1}{2}} y_{21}^{(3 .)} & 0 & y_{22}^{(2 .)}+y_{21}^{(1 .)} & 0 \\
0 & y_{22}^{(3 .)}
\end{array}\right]
$$



Fig. 5. Linearized diagram of the circuit from the Fig. 1

In the next step, the elements occurring in the numerator and denominator of the relation (1) are written into the corresponding positions in which they are in the matrix (2). Because the nodes of Fig. 1 are renumbered in Fig. 5, when $4 \rightarrow 2$, transfers of the currents after renumbered are following: $\frac{I_{4 E}}{I_{1 E}} \rightarrow \frac{I_{2 E}}{I_{1 E}}, \frac{I_{4 O}}{I_{1 E}} \rightarrow$ $\frac{I_{2 O}}{I_{1 E}}, \frac{I_{4 O}}{I_{1 O}} \rightarrow \frac{I_{2 O}}{I_{1 O}}, \frac{I_{4 E}}{I_{1 O}} \rightarrow \frac{I_{2 E}}{I_{1 O}}$. So will for transfer $\frac{I_{2 E}}{I_{1 E}}$ $\frac{I_{2 E}}{I_{1 E}}=\frac{-y_{21}^{(3 .)}\left(y_{22}^{(2 .)}+y_{21}^{(1 .)}\right)}{\left(y_{22}^{(2 .)}+y_{21}^{(2 .)}\right)\left(y_{22}^{(2 .)}+y_{21}^{(1 .)}\right)-z^{-1} y_{21}^{(2 .)} y_{21}^{(1 .)}}=$

$$
\begin{align*}
& =\frac{\Delta_{1 E, 2 O: 2 E, 2 O}}{\Delta_{2 E, 2 O: 2 E, 2 O}} \tag{3}
\end{align*}
$$

By comparing with the matrix (2) it is now apparent that in the numerator there is an algebraic complement of this matrix (2) created out of this matrix by leaving out the rows $1 E$ and $2 O$ and the columns $2 E$ and $2 O$, symbolically written $\Delta_{1 E, 2 O: 2 E, 2 O}$. In the denominator, there is then the algebraic complement of the matrix (2) created out of this matrix by leaving out the rows $2 E$ and $2 O$ and the columns $2 E$ and $2 O$, symbolically written $\Delta_{2 E, 2 O: 2 E, 2 O}$.

According to the theory of multiple algebraic complements [3], the sign $(-1)$ in the numerator gives the number of omitted odd indices, in the numerator the row $1 E$ is omitted, which is the first (odd index) row in the matrix, while the remaining row $2 O$ is even in the row as well as the omitted column $2 E$, which is the second column in the matrix, and the column $2 O$, which is the fourth column in the matrix.

In the denominator the omitted rows $2 E$ and $2 O$ and columns $2 E$ and $2 O$ are the second and fourth rows and columns in the matrix, ie they always have even indices, which then corresponds to a positive sign.

## 6 CONCLUSIONS

A unified method in analyzing switched current circuits is presented. As can be seen, the description of different types of memory cells can be used for the assembling of the general relations. The advantages of this approach are in its uniformity in deriving results from graph. By comparing the results from the matrix and results obtained from the Mason's formula are derived general relations for current transfers. The described method can be used for solving and understanding of simple circuits.

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