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COMMUNICATIONS

ZVS FULL–BRIDGE BASED DC–DC CONVERTER WITH LINEAR VOLTAGE GAIN ACCORDING TO DUTY CYCLE

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This paper presents a zero-voltage-switching (ZVS) full-bridge based DC-DC converter with linear voltage gain according to duty cycle. The proposed converter is based on an asymmetrical pulse-width-modulation (APWM) full-bridge converter which has various advantages over other converters. However, it has some drawbacks such as limited maximum duty cycle to 0.5 and narrow input range. The proposed converter overcomes these problems. The duty cycle is not limited and input voltage range is wide. Also, the ZVS operation of all power switches is achieved. Therefore, switching losses are significantly reduced and high-efficiency is obtained. Steady-state analysis and experimental results for the proposed converter are presented to validate the feasibility and the performance of the proposed converter.

K e y w o r d s: full-bridge converter, asymmetrical PWM, ZVS, DC-DC converter

1 INTRODUCTION

Phase-shift full-bridge converters are widely used. They have several advantages such as low voltage stresses of the switching devices, a fixed switching frequency, and ZVS of power switches. However, they have some disadvantages. Their major disadvantage is their large circulating current without delivering energy to load during the time intervals of high-side switches' or low-side switches' common turn-on [1–5]. As a result, conduction losses are large and the effective duty cycle becomes smaller. These drawbacks can be overcome by utilizing the asymmetrical duty cycle control technique which was introduced in [6]. An asymmetrical full-bridge buck converter with this control technique has various advantages over resonant converters and phase-shift full-bridge converters such as zero switching loss, no conduction loss penalty, and fixed switching frequency. However, the asymmetrical full-bridge buck converter has some drawbacks. The maximum allowable duty cycle is limited to 0.5. Therefore, it is not suitable for the applications requiring a wide input voltage range.

In order to overcome the drawbacks of the asymmetrical full-bridge buck converter, a ZVS full-bridge based DC-DC converter with linear voltage gain according to duty cycle is proposed in this paper. The proposed converter witch is shown in Fig. 1 features clamped switch voltages, fixed switching frequency, soft-switching operations of all power switches, and no limitation in duty cycle. Therefore, the proposed converter shows high efficiency and it is suitable to a wide input voltage range application.

2 OPERATING PRINCIPLE

The circuit diagram of the proposed converter is shown in Fig. 1 and its theoretical waveforms are shown in Fig. 2. An auxiliary clamping capacitor C_c is inserted between two bridges in full-bridge circuit. The switches of S_1 and S_3 operate simultaneously at a duty cycle D, whereas

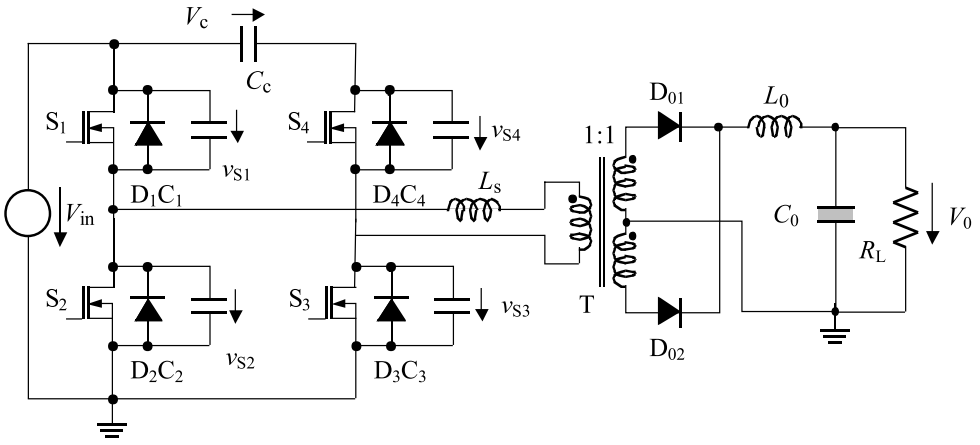

Fig. 1. Circuit diagram of the proposed converter

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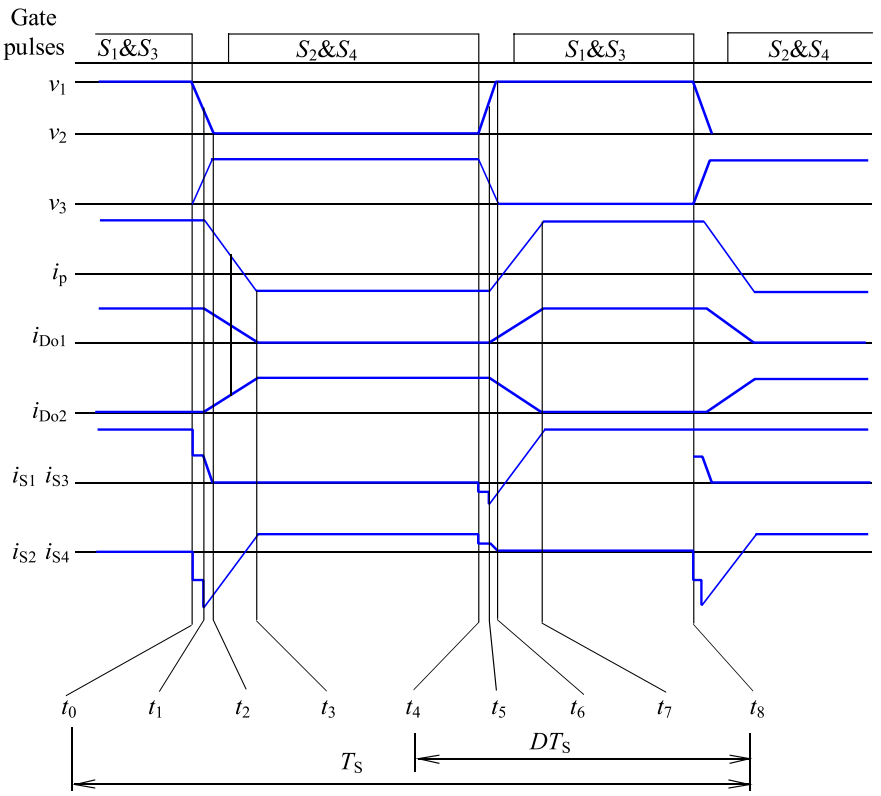

Fig. 2. Theoretical waveforms of the proposed converter

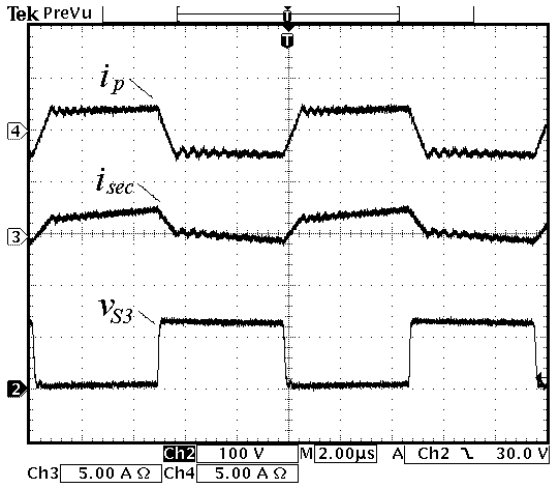

Fig. 3. Experimental waveforms of i_p, i_{sec}, and v_{S3}

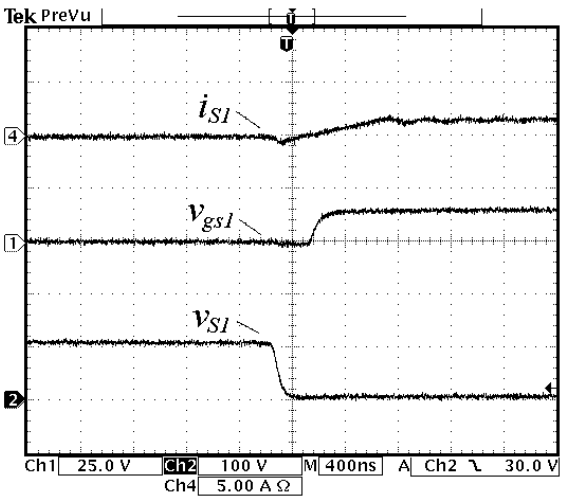

Fig. 4. Measured ZVS waveforms of S_1

the switches of S_2 and S_4 operate simultaneously at a duty cycle (1-D). The operation of the proposed converter during a switching period T_s is divided into eight modes. Before t_0, the switches S_1 and S_3 are conducting and the primary current flow through them. The output current I_o flows through D_{o1}.

Mode 1 $[t_0 \sim t_1]$. This mode starts with the turn-off of the switches S_1 and S_3. After that, constant primary current is diverted from S_1 and S_3 to C_1 through C_4. As a result, voltages v_1 and v_3 across C_1 and C_3 increase linearly, whereas voltages v2 and v4 across C_2 and C_4 decrease at the same rate. The load current I_o still flows through D_{o1}.

Mode 2 $[t_1 \sim t_2]$. At t_1, the output diodes D_{o2} begins to conduct. Since all output diodes are conducting, the transformer's secondary side is shorted and C_1 through C_4 and L_s form a series-resonant circuit. The voltage v_2 continues to decrease with a resonant manner, whereas the voltage v_3 continue to increase.

Mode 3 (t_2, t_3). When v_2 becomes zero, anti-parallel body diode D_2 begins to conduct. Then, gate signal is applied to S_2. Consequently, S_2 is turned on with ZVS.

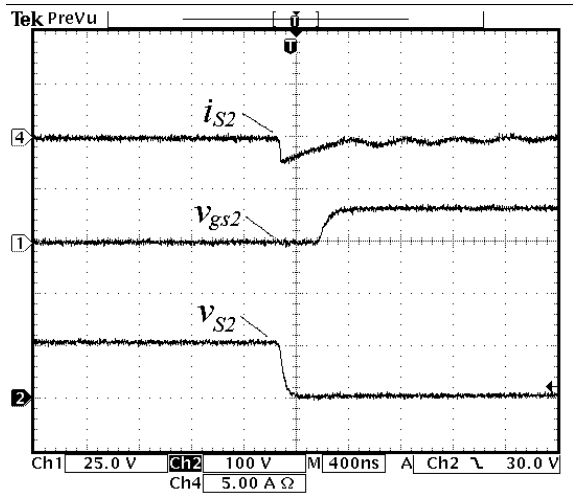

Fig. 5. Measured ZVS waveforms of S_2

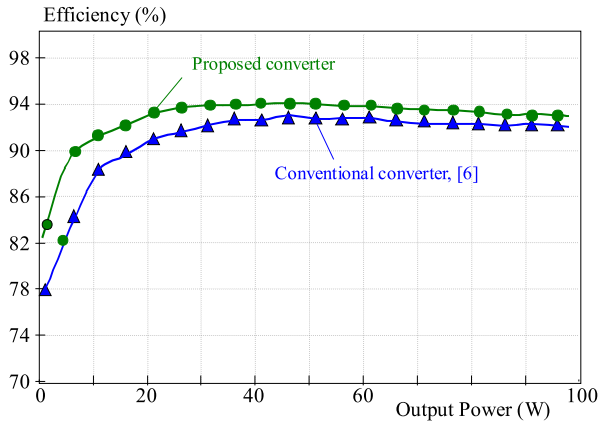

Fig. 6. Measured efficiency

Similarly, S_4 is turned on with ZVS. Since $-(V_{in}-V_c)$ is applied to L_s, the primary current i_p decreases linearly. As a result, the output diode current i_{Do1} decreases linearly, whereas i_{Do2} increases linearly.

Mode 4 (t_3, t_4). At t_3, i_{Do1} becomes zero and D_{o1} is turned off. The output current I_o flows only through D_{o2}.

Since modes 5 through 8 have similar operation to mode 1 through 4, the modal analysis is carried out only with mode 1 to 4. The output voltage V_o of the proposed converter is the average value of v_{rec}. Therefore, the output voltage V_o is obtained by

$$V_o = \frac{2DV_{in}}{n} - \frac{2L_oL_s}{n^2T_s} \approx \frac{2DV_{in}}{n}. \qquad (1)$$

From (1), it can be seen that the voltage gain has a linear relation with duty cycle. The duty cycle is not limited and input voltage range is wide.

3 EXPERIMENTAL RESULTS

To verify the performance of the proposed converter, a prototype has been built with the following specifications: $V_{in} = 85 \sim 120$ V, $V_o = 48$ V, $P_{o,\max} = 100$ W, and $f_s = 105$ kHz. The transformer turn ratio n is selected as 2. The serial inductance L_s is selected as 38 uH. The magnetizing inductance is selected as 600 uH and the capacitance of C_c is selected as 6.6 uF. The output filter consists of $L_o = 110$ uH and $C_o = 940$ uF. Figure 3 shows the measured key waveforms of the prototype. They agree with the theoretical analysis. Figures 4 and 5 show the soft-switching waveforms of the power switches. The voltages across the switches go to zero before the gate pulses are applied to the switches. Since the switch voltages are clamped as zero before the gate pulses are applied, the ZVS turn-on of the switches is achieved. Due to the softswitching operation, the switching losses are significantly reduce. Therefore, the efficiency of the system can be improved. The measured efficiency of the prototype is shown in Fig. 6. The maximum efficiency of the proposed converter is about 94 % at 50 W load.

4 CONCLUSIONS

A ZVS full-bridge based DC-DC converter with linear voltage gain according to duty cycle has been proposed in this paper. All power switches operate with ZVS and the switching losses are reduced. Also, it has linear voltage gain and its duty cycle is not limited. Therefore, the proposed converter can show high efficiency with wide input voltage range. Experimental results for the proposed converter were also presented. The feasibility of the proposed converter was confirmed with experimental results.

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