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THE IMPACT STUDY OF A STATCOM ON COMMUTATION FAILURES IN AN HVDC INVERTER FEEDING A WEAK AC SYSTEM

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The Static Synchronous Compensator (STATCOM) devices are pure power electronics devices that use voltage source, IGBT, IGCT or GTO based converters to generate reactive current. This paper illustrates the effect of STATCOM connected whit an HVDC inverter feeding a weak AC network, on the recovery from commutation failures following AC side disturbances. MATLAB/SIMULINK simulation results have demonstrated the robust performance of the proposed system based on the first CIGRÉ HVDC Benchmark model against commutation failures.

K e y w o r d s: HVDC inverter, Commutation failures, STATCOM

1 INTRODUCTION

The main shortcomings of line commutated converter (LCC) are large reactive power requirements (both during rectification and inversion), injection of low-order harmonic currents, risk of inverter commutation failures and their dependence on reasonably strong AC systems to provide the commutating voltages. The most outstanding contributions in the subject are included in [1]. In this reference, the weakness of an AC/DC node is classified using a relative term which is the short circuit ration (SCR), *ie*, the ratio of the AC system short circuit capacity to DC link power: weak systems are those having SCR between 3.0 and 2.0, whereas very weak systems have a value lower than 2.0.

Generally, it can be expected that the weaker the AC system at the inverter, the more likely an AC fault remote from the inverter will cause commutation failures, since it is more likely to result in a larger voltage reduction (or be manifested as a voltage phase shift for single phase faults) at the inverter.

An apparent anomaly can arise in some situations where the system strength is seemingly increased but the inverter's exposure to system faults and hence incidence of commutation failures is also increased. This does not imply that the inverter's performance is worse with the stronger system. One has to be careful in evaluating the relative causes and effects. An extreme example of this would be if an entirely separate system was connected to an inverter or it was already connected to an ac system by a new tie line. This new system would effectively increase the total system strength and actually improve the inverter performance for remote faults in the previously connected system. However, the inverter is now exposed to all the faults in the new system, and this has to be considered as well. A less obvious example could be a new line added to an existing system. The new line may increase the equivalent system strength and generally improve inverter performance, but it may also increase the inverter's effective exposure to faults in a network at the end of that line or, of course, on the line itself.

Another scenario could be postulated where a new system addition may increase the system strength but move the system, as seen at the inverter, closer to a harmonic resonance. Under certain faults or switching actions, this could inadvertently increase voltage distortions, increase incidence of commutation failures, and deteriorate the inverter performance.

A lot of works have been done to know the cause and consequence of the commutation failure [2, 3]. Earlier research in [4] shows effective control over fault current magnitudes as well as post-fault commutation problems. Reference [5] proposed a control strategy to obtain good DC system recovery from commutation failure. Reference [6] investigate whether a possible improvement to commutation failure prediction. However, another perspective on the problem is provided in [7] and [8] which deal with the coordination of HVDC and STATCOM, but have not been discussed in detail.

This work is related to the study of the impact of a STATCOM with two modes of control strategies at an HVDC inverter connected to a weak AC network. The first CIGR benchmark for HVDC [9] has been chosen for simulation in MATLAB/SIMULINK. The reason for the selection of this model is the presence of numerous system difficulties that may be encountered in a real system.

2 COMMUTATION FAILURES IN HVDC INVERTER

In line-commutated converter (Fig. 1), the thyristor module is very sensitive to voltage bias. When a commutation occurs, a second thyristor is fired and forces the first to get a negative bias, and thus get switched

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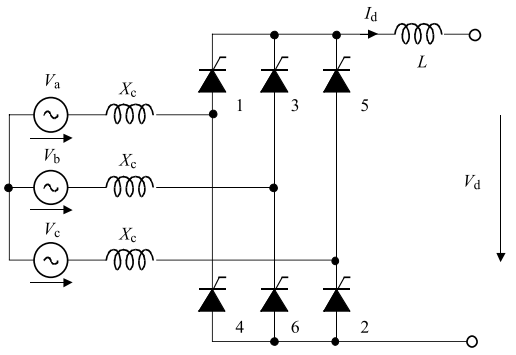

Fig. 1. Equivalent circuit for three-phase full-wave bridge converter

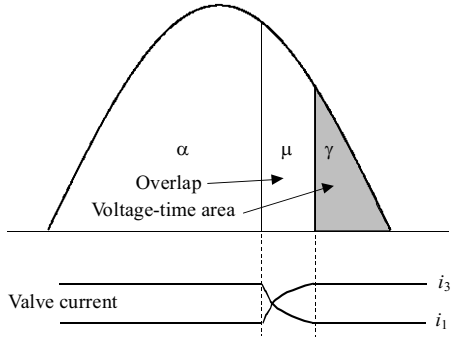

Fig. 2. Commutation process between valve 1 and valve 3

Table 1. CIGRÉ HVDC Benchmark system data

Parameters	Rectifier	Inverter
AC Voltage	345 kV	230 kV
DC Power	1000 kW	1000 kW
DC Voltage	500 kV	500 kV
DC Current	2 kA	2 kA
Frequency	50 Hz	50 Hz
Minimum angle	$\alpha = 15°$	$\gamma = 15°$
SCR	2.5	2.5

off. However, this negative bias has to remain for a certain time period (Fig. 2) for the thyristor to successfully extinguish in order to not cause a failure of the transmission. This time area is called the voltage-time area, and is very important, especially in the inverter of the HVDC station where the firing angle (α) is ideally held around 130–140°. Adding an overlap (μ) of 17– 20°, the remaining voltage area, expressed as the extinction angle (γ), becomes very limited. Note that

$$\gamma = 180° - \alpha - \mu\,. \tag{1}$$

The overlap angle μ is a function of the commutation voltage and the dc current. Hence, a decrease in commutation voltage or an increase in dc current can cause an increase in μ resulting in a decrease in γ. If $\gamma < \gamma_{\min}$, a commutation failure may result. In this case, the outgoing valve will continue to conduct current and when the incoming valve is fired in sequence, a short circuit of the bridge will occur.

During a commutation failure, the two valves in an arm of the bridge are conducting. Therefore, the AC current goes to zero while the DC current continues to flow. Thio [2] proposed the empirical equation for commutation failure as shown in equation (2) and (3). In the below equations, the possibility of commutation failure is expressed to ΔV which is the onset voltage of commutation failure. Equation (2) is for 3-phase fault case and equation (3) is for 1-phase fault case.

$$\Delta V = 1 - \frac{I'_d}{I_d}\frac{X_{cpu}}{X_{cpu} + \cos\gamma_0 - \cos\gamma}\,, \tag{2}$$

$$\Delta V = 1 - \frac{I'_d}{I_d}\frac{X_{cpu}}{X_{cpu} + \cos(\gamma_0 + \phi) - \cos\gamma}\,. \tag{3}$$

Where, I'_d is the larger DC current, X_{cpu} is an impedance of converter transformer expressed in per unit, γ_0 is the critical commutation margin angle corresponding to required thyristor extinction angle, γ is nominal commutation margin angle, ϕ is zero-crossing phase shift angle due to possible unsymmetrical voltage reduction.

Disturbances in the AC network can cause voltage drops and phase shifts in the voltages [10]. This in turn can cause the voltage-time area to be insufficient, and cause what is called a commutation failure. Keeping a large voltage-time area can be difficult hence it also means a lower voltage output as well as a higher current, which in turn increases the converter reactive power consumption. The desire to maintain an adequate voltage-time area while still keeping the reactive power supply requirement and voltage ratings down places tough constraints on the control system.

It has been shown that HVDC installations in combination with a weak AC grid have resulted in commutation failures to spread to other links in the area [11]. It is therefore preferable to improve the possibility to detect and react to disturbances that could lead to commutation failure caused by influence of other HVDC transmissions.

3 SYSTEM UNDER STUDY

Figure 3 shows the proposed hybrid HVDC system. It consists of a classic HVDC LCC link (based on first CIGRÉ HVDC benchmark model) and STATCOM device connected at the inverter side. The STATCOM provides both the necessary commutation voltage to the HVDC inverter and the reactive power compensation to the AC network during steady state and dynamic conditions. The first CIGRÉ HVDC benchmark system is developed in MATLAB/Simulink [12].

3.1 The first CIGRÉ HVDC benchmark model

The CIGRÉ HVDC system is a mono-polar 500 kV, 1000 MW HVDC link with 12-pulse converters on both rectifier and inverter sides, connected to weak AC systems (short circuit ratio (SCR) of 2.5 at a rated frequency of

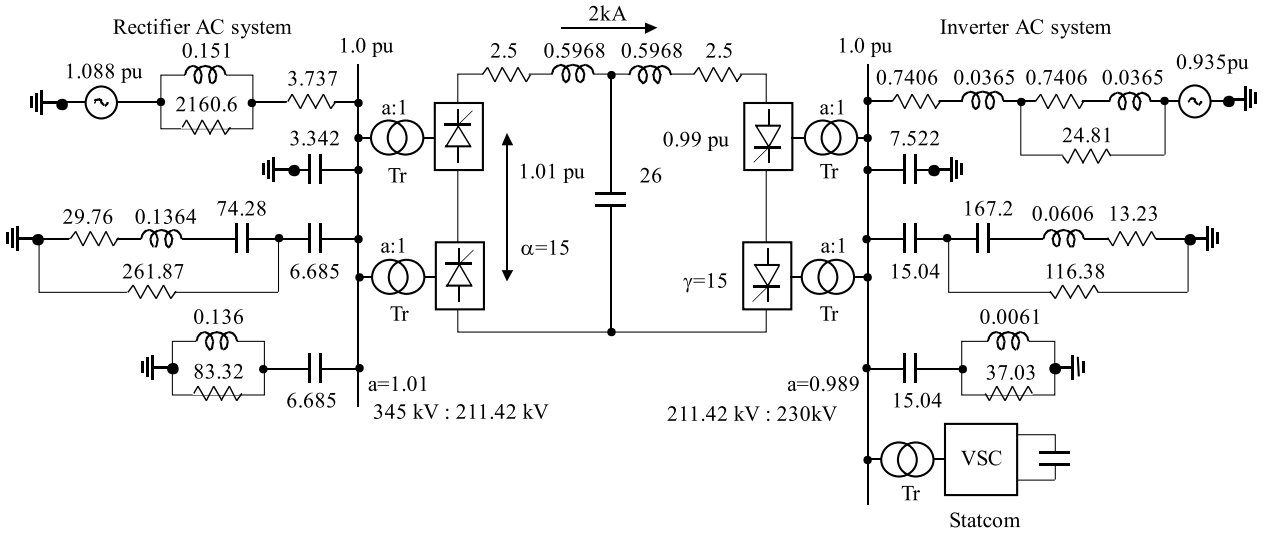

Fig. 3. Proposed HVDC-STATCOM System

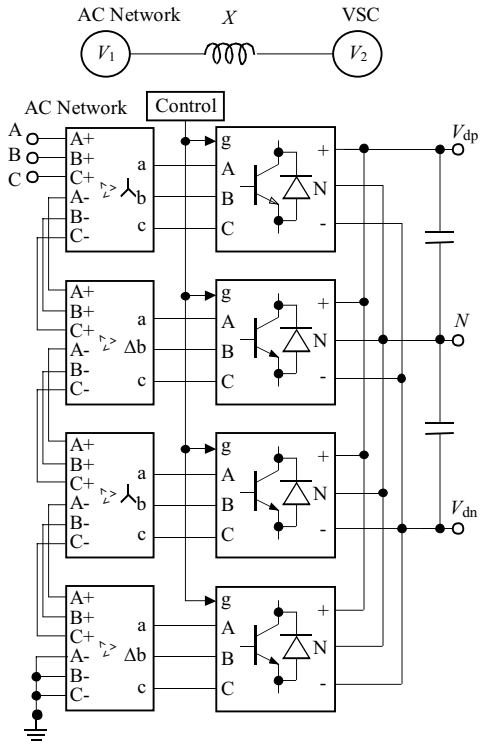

Fig. 4. 48-Pulse VSC based STATCOM

50 Hz) that provide a considerable degree of difficulty for dc controls. Damped filters and capacitive reactive compensation are also provided on both sides. The AC sides of the HVDC system consist of supply network, filters, and transformers on both sides of the converter. The AC supply network is represented by a Thévénin equivalent voltage source with equivalent source impedance. AC filters are added to absorb the harmonics generated by the converter as well as to supply reactive power to the converter. The DC side of the converter consists of smoothing reactors for both rectifier and the inverter side. The DC transmission line is represented by an equivalent T network, which can be tuned to fundamental frequency to provide a difficult resonant condition for the modeled system. Table 1 shows the CIGRÉ HVDC benchmark system data.

3.2 The STATCOM

In our model, the static synchronous compensator (STATCOM) is located at the inverter side of the HVDC link and has a rating of ±100 MVA. This STATCOM is a typical three-level PWM STATCOM. It consists of a three-level 48-pulse inverter and two series-connected 3000 F capacitors which act as a variable DC voltage source. Based on a voltage-sourced converter (VSC), the STATCOM regulates system voltage by absorbing or generating reactive power. Contrary to a thyristor- based static var compensator (SVC), STATCOM output current (inductive or capacitive) can be controlled independent of the AC system voltage.

Figure 4 shows the STATCOM used in our system. It consists of four 3-phase 3-level inverters coupled with four phase shifting transformers introducing phase shift of ±7.5 degrees. Except for the 23^{rd} and 25^{th} harmonics, this transformer arrangement neutralizes all odd harmonics up to the 45^{th} harmonic. Y and Δ transformer secondaries cancel harmonics $5+12n$ (5, 17, 29, 41, ...) and $7+12n$ (7, 19, 31, 43, ...). In addition, the 15° phase shift between the two groups of transformers (Tr1Y and Tr1? leading by 7.5°, Tr2Y and Tr2Δ lagging by 7.5°) allows cancellation of harmonics $11+24n$ (11, 35, ...) and $13+24n$ (13, 37, ...). Considering that all $3n$ harmonics are not transmitted by the transformers (Δ and ungrounded Y), the first harmonics that are not cancelled by the transformers are therefore the 23^{rd}, 25^{th}, 47^{th} and 49^{th} harmonics. By choosing the appropriate conduction angle for the three-level inverter (172.5), the 23^{rd} and 25^{th} harmonics can be minimized. The first significant harmonics generated by the inverter will then be

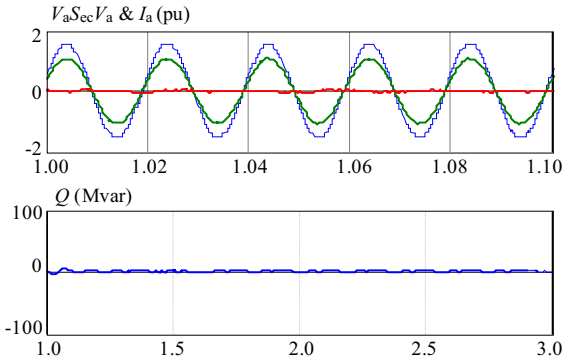

Fig. 5. STATCOM waveforms in VAR control mode, Qref = 0

47^{th} and 49^{th}. Using a bipolar DC voltage, the STATCOM thus generates a 48-step voltage approximating a sine wave.

The principle of operation of the STATCOM is explained below showing the active and reactive power transfer between a source V_1 and a source V_2.

$$P = \frac{V_1 V_2 \sin\delta}{X}\,, \tag{4}$$

$$Q = \frac{V_1(V_1 - V_2\cos\delta)}{X} \tag{5}$$

where V_1 is the line to line voltage of source, V_2 is the line to line voltage of STATCOM, X is the equivalent reactance between transformer and filters, δ is the angle of V_1 with respect to V_2. Since δ is very small, if we set $\delta = 0$:

$$P = 0\,, \tag{6}$$

$$Q = V_1\frac{V_1 - V_2}{X}\,. \tag{7}$$

If V_1 is greater than V_2, Q is flowing from V_1 to V_2 (*ie*, STATCOM is absorbing reactive power). On the reverse, if V_1 is less than V_2, Q is flowing from V_2 to V_1 (*ie*, STATCOM is generating reactive power) [13].

1) STATCOM control system

The control system task is to increase or decrease the capacitor DC voltage, so that the generated AC voltage has the correct amplitude for the required reactive power. The control system must also keep the AC generated voltage in phase with the system voltage at the STATCOM connection bus to generate or absorb reactive power only (except for small active power required by transformer and inverter losses).

The control system uses the following modules: PLL (phase locked loop) synchronizes IGBT pulses to the system voltage and provides a reference angle to the measurement system. Measurement System computes the positive-sequence components of the STATCOM voltage and current, using phase-to-dq transformation and a running-window averaging. Voltage regulation is performed by two PI regulators: from the measured voltage V_{meas} and the reference voltage V_{ref}, the Voltage Regulator block (outer loop) computes the reactive current reference $I_{q,ref}$ used by the Current Regulator block (inner loop). The output of the current regulator is the α angle which is the phase shift of the inverter voltage with respect to the system voltage. This angle stays very close to zero except during short periods of time, as explained below. Firing Pulses Generator generates pulses for the four inverters from the PLL output (ωt) and the current regulator output (α angle).

To explain the regulation principle, let us suppose that the system voltage V_{meas} becomes lower than the reference voltage V_{ref}. The voltage regulator will then ask for a higher reactive current output (positive I_q capacitive current). To generate more capacitive reactive power, the current regulator will then increase α phase lag of inverter voltage with respect to system voltage, so that an active power will temporarily flow from AC system to capacitors, thus increasing DC voltage and consequently generating a higher AC voltage. The STATCOM control system implements two mode of operation (voltage control mode & Var control mode). In Voltage control mode the primary voltage V_{abc} is controlled at V_{ref} within the droop setting. In Var control mode, either the reactive power output is kept constant at Q_{ref}. Figure 5 shows the STATCOM in Var control mode, where $Q_{ref} = 0$.

4 SIMULATION RESULTS

In this paper, comparative studies of the three systems of CIGRE model without STATCOM and with STATCOM (with two mode of control) were performed. The AC network parts of the study system and its DC controls are identical to those in the CIGRE benchmark model except for that STATCOM is added to AC busbar. For each system, two fault cases are simulated:

- Single phase to ground fault at the inverter side (remote fault according to the breaker resistance),
- Three phase to ground fault at the inverter side (remote fault according to the breaker resistance).

For each of the transient case considered above, plots of inverter AC voltage, DC current and DC voltage are given. Also the inverter valves current of two Graetz bridges connected in series (The bridges are connected to the AC system by means of converter transformers, one of YY winding structure and another $Y\Delta$ winding structure).

4.1 Single phase-to-ground fault at inverter side

A single phase-to-ground fault was applied to the A-phase of the inverter bus through resistance, and the duration of the fault was 5 cycles. Results of this study are shown in Table 2 where the resistance value varies between $0\,\Omega$ and $110\,\Omega$. Figure 6 represents the case where the resistance breaker value equal to $92\,\Omega$.

Table 2. Single phase-to-ground fault at inverter side according to breaker resistance

Single phase fault	Without STATCOM			With STATCOM (Voltage control mode)			With STATCOM (VAR control mode)		
Breaker resistance $R(\Omega)$	CFs during system fault	CFs After fault clearing	Recovery time (s)	CFs during system fault	CFs After fault clearing	Recovery time (s)	CFs during system fault	CFs After fault clearing	Recovery time (s)
0	CFs	CFs	0.2	CFs	CFs	0.2	CFs	CFs	0.2
50	CFs	No CFs	0.2	CFs	No CFs	0.2	CFs	No CFs	0.2
75	CFs	No CFs	0.2	CFs	No CFs	0.15	CFs	No CFs	0.15
80	CFs	No CFs	0.2	CFs	No CFs	0.15	CFs	No CFs	0.13
92	CFs	No CFs	0.15	CFs	No CFs	0.15	No CFs	No CFs	–
100	No CFs	CFs	0.15	No CFs	CFs	0.13	No CFs	No CFs	–
110	No CFs	No CFs	–	No CFs	No CFs	–	No CFs	No CFs	–

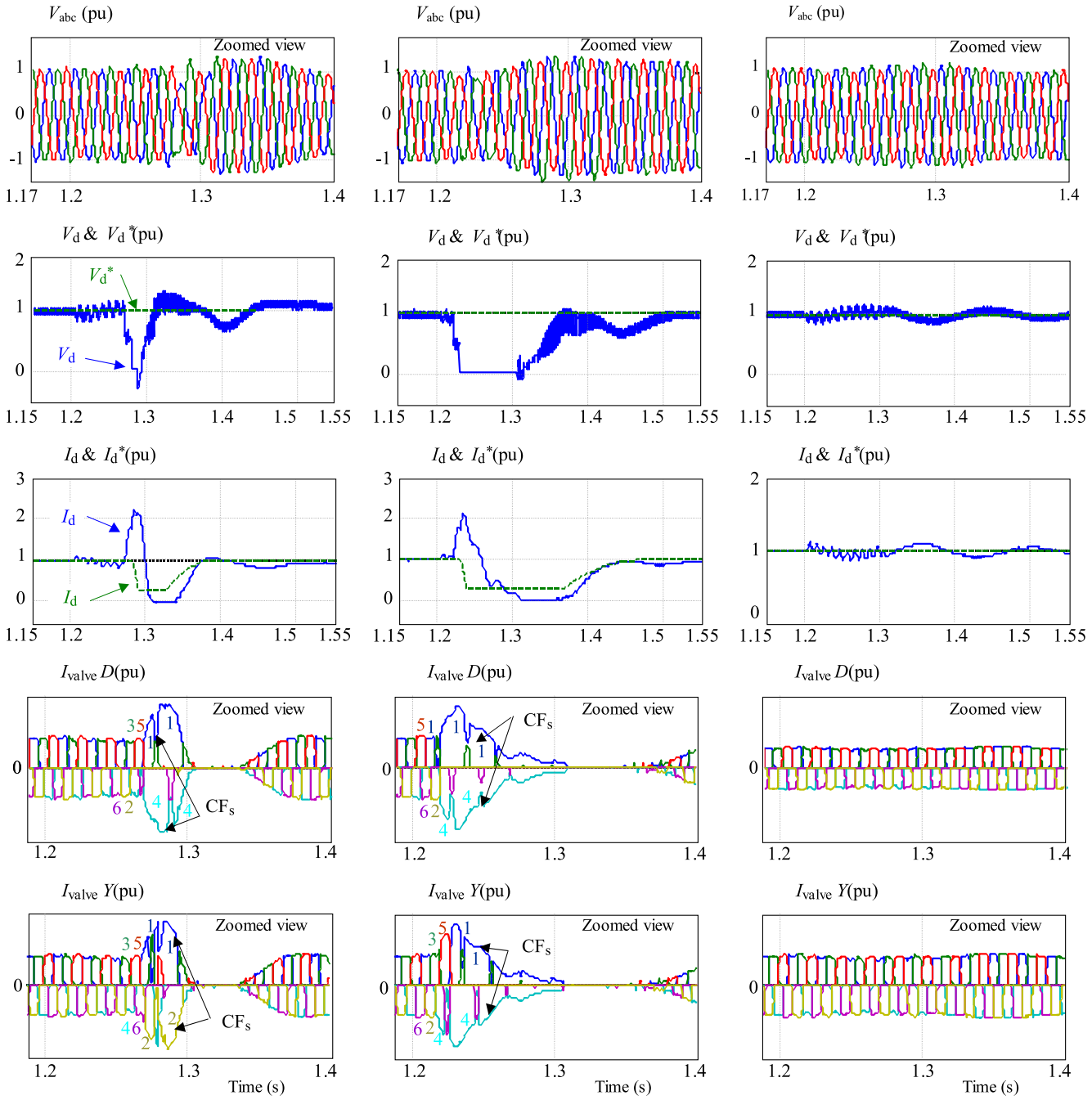

Fig. 6. Single phase-to-ground fault at inverter side ($R = 92\,\Omega$): left – With STATCOM, middle – Without STATCOM (Voltage control mode) right - With STATCOM (VAR control mode)

1) Operation without STATCOM

When this fault is applied at $t = 1.2$ s, due to a reduction in AC voltage of the inverter bus, the inverter DC voltage decreases. The DC current therefore shoots up. The rectifier current controller attempts to reduce the current by increasing its firing angle. The DC current decreases to a low average value as determined by VDCOL function (0.3 pu). This control named Voltage Dependent Current Order Limits (VDCOL) automatically reduces the reference current I_d^* set point when V_d decreases. Reducing the I_d reference currents also reduces the reactive power demand on AC network, helping to recover from fault [5]. The inverter valves current plots indicate a number of commutation failures of the corresponding valve groups (1 and 4), which translates by an increase in the DC current because the valves 1 and 4 in the $(Y\Delta)$ bridge are conducting current at the same time, and that the $(Y\Delta)$ graetz bridge is short-circuited on the DC side. Other commutation failures of the valves 1 and 2 will accrue during the fault in the second bridge (YY). Since the DC voltage is zero during a period following the commutation failures, no active power will be transmitted during this time. When the fault is cleared at $t = 1.3$ s, the system recovers in approximately 0.15 s after fault clearing.

2) Operation with STATCOM (Voltage control mode)

For the same fault, the waveforms resulting are displayed in Fig. 6. When this fault is applied at $t = 1.2$ s, commutation failures will accrue (valve 1 and 4 at the two bridge), and we can show that the valves 1 and 4 are conducting current at the same time, and that each graetz bridge $(YY/Y\Delta)$ is short-circuited on the DC side. The DC current therefore shoots up; the VDCOL operates and reduces the reference current to 0.3 pu. When the fault is cleared at $t = 1.3$ s, the DC voltage starts to increase, following commutations take place in a normal way, and normal operation is resumed. The system recovers in approximately 0.15 s after fault clearing.

3) Operation with STATCOM (VAR control mode)

Results of this transient study are shown in Fig. 6. The fault is applied at $t = 1.2$ s, and we can see that the nominal operation of the DC transmission is not affected by the fault.

4.2 three phase-to-ground fault at inverter side

A three-phase-ground was applied to the three phases of the inverter bus through resistance. The duration of the fault was 5 cycles. Results of this study are shown in Table 3. The resistance value varies between $0\,\Omega$ and $90\,\Omega$. Figure 7. represents the case where the resistance breaker value equal to $77\,\Omega$.

1) Operation without STATCOM

When the fault is applied, due to a sudden reduction in the inverter DC voltage there is overshooting in DC current of magnitude 2 pu. The rectifier current controller attempts to reduce the DC current by increasing the firing angle of the rectifier. The DC current reduces to a low average value as determined by the VDCOL. From Fig. 7, after the firing of valve 5 of the six-pulse bridge (YY), the disturbance at $t = 1.2$ s in the voltage occurs that reduces the remaining voltage-time area for valve 3. In such a way, that no forward blocking capability is obtained for valve 3. Consequently, the current through valve 3 starts to increase while the current through valve 5 reduces to zero again. The next commutation that will take place is from valve 4 to valve 6; however, this indicates that both valves 3 and 6 are conducting current at the same time and that the six-pulse bridge coupling with (YY) is short-circuited on the DC side. The same case for the second bridge coupling with $(Y\Delta)$. When the fault is cleared at $t = 1.3$ s, the VDCOL operates and rises the reference current to 1 pu. The system recovers in approximately 0.15 s after fault clearing.

2) Operation with STATCOM (Voltage control mode)

For the same fault, the waveforms resulting are displayed in Fig. 7. The beneficial impact of the STATCOM is evident.

3) Operation with STATCOM (VAR control mode)

The results show that the commutation failures were not observable in Fig. 7. Again the beneficial impact of the STATCOM is evident

4.3 Discussion of the results

Tables 2 and 3 show the occurrence of commutation failures during and after single or three phase to ground faults according to the breaker resistance and also according to the STATCOM control mode. Table 2 shows the result in the case of single phase to ground fault. With the STATCOM present, CFs are experienced for R varies from $0\,\Omega$ to $91\,\Omega$ (No CFs for $R = 92\,\Omega$). However, without the STATCOM, CFs occurs for R varies from $0\,\Omega$ to $99\,\Omega$. From the Table 3, it can be seen that with the STATCOM present, CFs are experienced for R varies from $0\,\Omega$ to $76\,\Omega$ (No CFs for $R = 77\,\Omega$). However, without the STATCOM, CFs occurs for R varies from $0\,\Omega$ to $89\,\Omega$. The beneficial impact of the STATCOM is evident. It should be noted that the VAR control mode of the STATCOM is beneficial in the case of asymmetric faults as compared with the voltage control mode. However, the system response due to a symmetrical fault is practically the same for both modes of control of the STATCOM.

Also, comparison of the results indicates that the AC voltage recovered with STATCOM is higher than one

Table 3. Three phase-to-ground fault at inverter side according to breaker resistance

Three phase fault	Without STATCOM			With STATCOM (Voltage control mode)			With STATCOM (VAR control mode)		
Breaker resistance $R(\Omega)$	CFs during system fault	CFs After fault clearing	Recovery time (s)	CFs during system fault	CFs After fault clearing	Recovery time (s)	CFs during system fault	CFs After fault clearing	Recovery time (s)
0	CFs	CFs	0.25	CFs	No CFs	0.2	CFs	No CFs	0.15
50	CFs	No CFs	0.15	CFs	No CFs	0.15	CFs	No CFs	0.15
75	CFs	No CFs	0.15	CFs	No CFs	0.15	No CFs	No CFs	–
77	CFs	No CFs	0.15	No CFs	No CFs	–	No CFs	No CFs	–
80	CFs	No CFs	0.15	No CFs	No CFs	–	No CFs	No CFs	–
85	CFs	No CFs	0.15	No CFs	No CFs	–	No CFs	No CFs	–
90	No CFs	No CFs	–	No CFs	No CFs	–	No CFs	No CFs	–

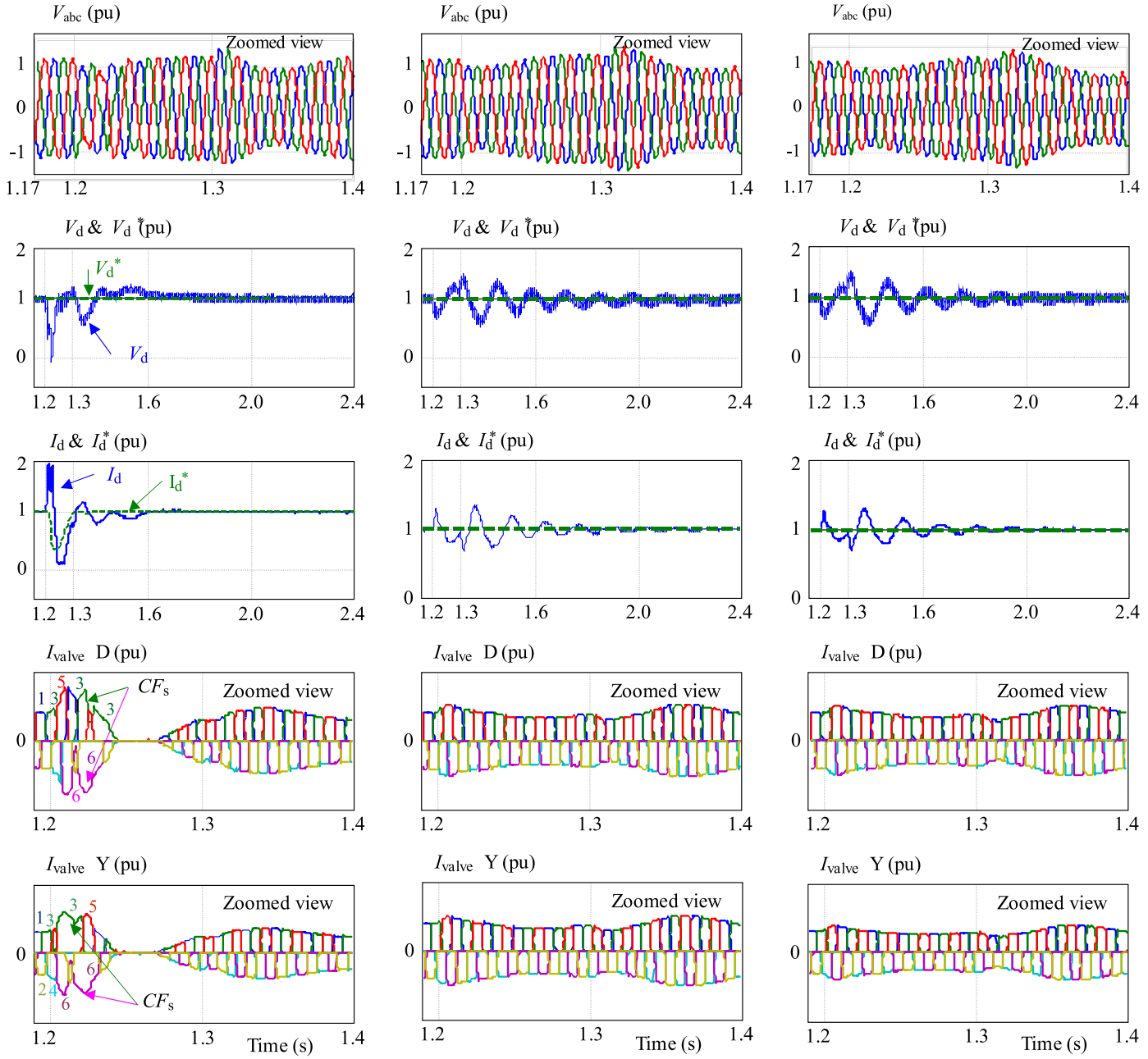

Fig. 7. Three phase-to-ground fault at inverter side ($R = 77\,\Omega$): left – Without STATCOM, middle – Without STATCOM (Voltage control mode) right - Without STATCOM (VAR control mode)

without STATCOM at the node connected with the DC–AC inverter after the single and three phase ground faults on the inverter AC network side.

5 CONCLUSIONS

In this paper, an evaluation of the coordination between STATCOM and HVDC classic link feeding a weak AC network is performed in order to mitigate commutation failures phenomena .The principle of the proposed system and the control strategy has been described, where two method of the STATCOM control are developed and compared. Dynamic performance during various single and three phase's faults at the inverter side have been demonstrated by the simulation results and they have shown satisfactory responses.

The main advantage of these approaches is that the probability of commutation failure can be reduced by increasing the VAR compensation required with the STATCOM device. The simulation results of the proposed scheme are very good and from the technical point of view provide a good solution for connecting weak AC networks.

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