

# ON MEASUREMENT UNCERTAINTY OF ADC NONLINEARITIES IN OSCILLATION-BASED TEST

Peter MRAK — Anton BIASIZZO — Franc NOVAK \*

Oscillation-based test (OBT) is one of the approaches for measuring static ADC parameters such as differential nonlinearity (DNL) and integral nonlinearity (INL) that can be implemented in a built-in self-test arrangement. When applying the OBT approach in practice we noticed an inherent measurement uncertainty related to the slope of the ADC input signal in OBT test mode. Experimental environment in Matlab has been set up to study the phenomenon. Experiments with varying values of slope were performed to demonstrate the margins of DNL measurement uncertainty.

**Key words:** oscillation-based test, analog-to-digital converter, differential nonlinearity

## 1 INTRODUCTION

Oscillation-based test (OBT) [1–3] is a low-cost analog and mixed-signal test technique primarily used for fault detection. In the test mode, the circuit is transformed into an oscillator and the frequency of oscillation is measured and compared to a reference value obtained on a known-good circuit operating in the same conditions. Assuming that most possible faults manifest in the discrepancy from the reference oscillation frequency, the technique offers an effective means of fault detection. It requires minimal re-configuration of the circuit-under-test and is thus suitable for built-in self-test. Oscillation based test has been applied to different kind of circuits including filters, A/D and D/A converters, PLLs, *etc* [1–8]. Extensive summary of the proposed solutions can be found in [9, 10].

In the development phase of the test procedure for the target unit-under-test, the impact of possible faults on the measured frequency must be analyzed. If some faulty components do not affect the frequency of oscillation, additional measurements of other parameters are required in order to achieve the required fault coverage. The acceptance/reject margins are determined on the basis of the required user specifications. For example, in our earlier industrial application of a go no-go test of a low-pass filter stage as a part of a communication unit produced by Hipot Hyb [11], the test system was first adjusted in reference to a golden filter stage. Reference filter stages with values corresponding to the acceptance ranges within  $\pm 0.1$  percent and  $\pm 0.3$  percent were measured in the test system in order to set up the test system acceptance margins. A pre-production series of 546 active adjusted filter stages were tested, and 95 % passed the go no-go test. The stages that passed the go no-go test were assembled in the final product. Functional test confirmed that all the circuits operated within the required tolerances.

Simulations can be performed to assess the impact of discrepancy from nominal values of individual compo-

nents of the unit-under-test on the oscillation frequency. Some work has been done to improve the sensitivity of OBT to parametric faults [12]. A so called “predictive oscillation based test” (POBT) proposed in [13, 14] can be used to define the acceptance region for an OBT implementation.

So far, most of the OBT related work has been directed either towards the problem of modification of given circuit-under-test into an oscillator, or towards analysis of detected faults (exploring ways to increase fault coverage or even trying to perform fault diagnosis). Little attention has been paid to the measurement accuracy of the developed OBT solutions. As stated in [15], for a simple arrangement consisting of a zero-crossing detector and a counter, the measurement accuracy is determined by the oversampling ratio ( $T_{osc}/T_s$ ) and depends of the phase shift, which is equivalent to one sampling period ( $T_s$ ) as maximum. While this is in general true for any OBT implementation, there exist another sources of inaccuracy associated with the OBT implementations adapted for the specific class of circuit-under-test. An example, related to OBT test of ADC is discussed in this paper.

## 2 OSCILLATION-BASED TEST OF ADC

OBT arrangement for testing an analog-to-digital converter (ADC) is shown in Fig. 1. It consists of a feedback loop, which forces the ADC to oscillate around a selected code [7]. The input stimulus of ADC is a triangle wave signal of symmetrical slope controlled by the OBT control logic. The measured frequency of the triangle wave signal can be used for a simple go no-go test or for determining static ADC parameters such as differential nonlinearity (DNL) and integral nonlinearity (INL). In this paper we focus on OBT measurements of DNL. For this purpose, some introductory remarks are given in the following.

An ADC generates a single output code for a range of input voltages. The voltage level where the ADC output

\* Computer Systems Department Jozef Stefan Institute, Ljubljana, Slovenia, peter.mrak@ijs.si, anton.biasizzo@ijs.si, franc.novak@ijs.si

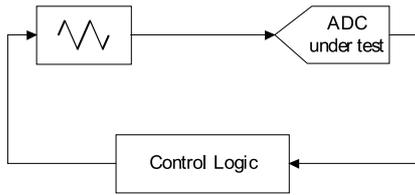


Fig. 1. Arrangement of oscillation-based test of ADC

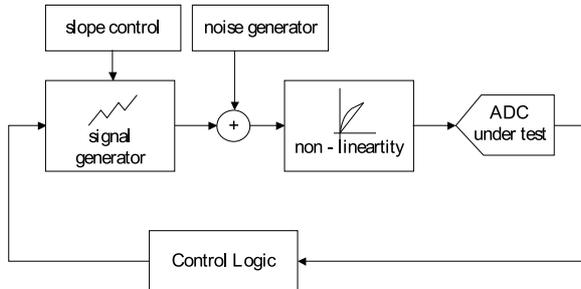


Fig. 2. The environment for analyzing measurement uncertainty of OBT of ADC

changes from code  $i - 1$  to code  $i$  is denoted as threshold voltage  $V_{TH}(i)$ , and where the ADC output changes from code  $i$  to code  $i + 1$  as threshold voltage  $V_{TH}(i + 1)$ , respectively. The difference between the threshold voltages  $V_{TH}(i)$  and  $V_{TH}(i + 1)$  is denoted as code width  $Q(i)$ . The code widths of an ideal  $n$ -bit ADC are equal. Their width is obtained by dividing the full scale range by the number of ADC codes. DNL measures the relative deviation of each code from the ideal value (1 LSB). The deviation is due to the fact that the actual threshold voltages differ from their nominal values. For a given code  $i$  DNL is defined as

$$DNL(i) = \frac{Q(i) - Q_N}{Q_N}, \quad (1)$$

where  $Q_N$  denotes the nominal code width.

### 3 OBT ENVIRONMENT

In order to analyze the influence of different measurement parameters on DNL estimation using OBT method a simulation environment using Matlab Simulink was developed. The environment (shown in Figure 2) allows us to perform calculations of DNL over the whole set of ADC codes with arbitrary number of oscillation periods at arbitrary code. Since the ADC block in the Matlab Simulink environment models an ideal ADC, an additional block with nonlinear transfer function was added in front of ADC to mimic the realistic non-linear behavior. Furthermore, a noise generator was included which allows us to introduce noise in the input signal.

The slope of the input signal is the most significant measurement parameter. Higher slope increases the oscillation frequency and shortens the measurement time, however it affects the measurement accuracy. To analyze the behavior of the testing method with different input

signal slopes, slope control was added to the input signal generator.

In the ideal case where the slope of the input signal is time invariant and without any noise, the oscillation period at given code is constant (because the duration of input signal rise and fall are constant). Hence the measurement of the half of the period is sufficient for the determination of the oscillation frequency. However, in the presence of noise the oscillation periods may vary. The influence of noise on oscillation frequency can be reduced by measuring and averaging over several periods. This, on the other hand, prolongs the DNL measurement time. The feedback loop control logic was adopted to perform arbitrary number of oscillations at given code which enables us to study all possible scenarios.

In order to measure the DNL of the ADC, the DNL of each code, with exception of the extreme codes, must be determined. To achieve this, while keeping the measurement time as low as possible, the feedback control logic is designed in such a way that DNL of successive codes are determined in their order starting with the code 1. The subsequence of the generated input signal with two oscillations per code is shown in Fig. 3.

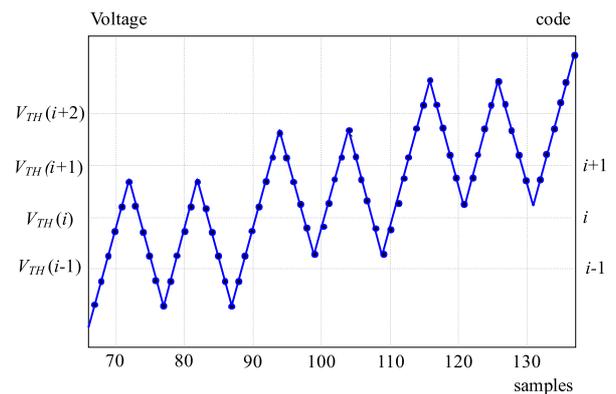


Fig. 3. Test procedure

### 4 MEASUREMENT UNCERTAINTY

As noted earlier, in the ideal case (*ie*, ideal ADC, input signal with constant slope and without noise) the oscillation period remains constant. The oscillation period is a multiple of the sampling period, because the slope alterations are performed only at sampling instances. Consequently, the oscillation period can be exactly determined. This comes with a price, notably an interval of slopes produce the same oscillation frequency which leads to measurement uncertainty.

In the case of coherent sampling, where the slope of input signal traverses the code width in multiple of sampling periods (denoted by  $k$ ), the oscillation period is constant irrespective of the phase shift  $\theta_i$  of the input signal as shown in Fig. 4. In coherent sampling  $\theta_i = \theta_{i+1}$ . In the case of non-coherent sampling, when the slope of the input signal traverses code width in non-whole number

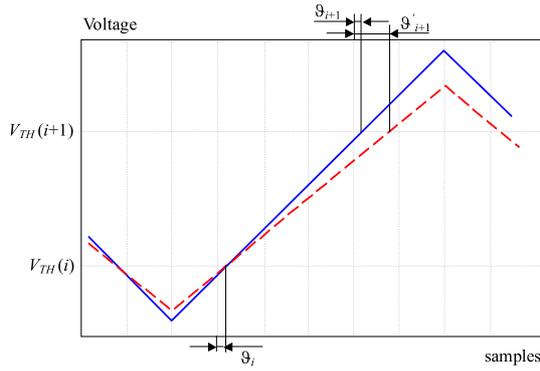


Fig. 4. Phase shift of the input signal

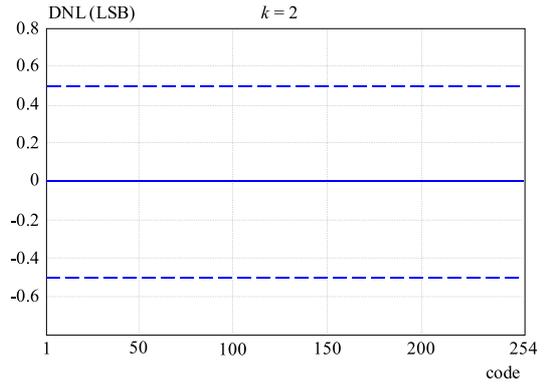


Fig. 5. DNL measurement of an ideal ADC using input slope with  $k = 2$

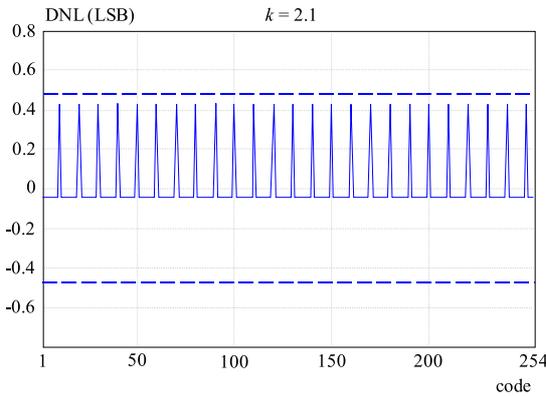


Fig. 6. DNL measurement of an ideal ADC using input slope with  $k = 2.1$

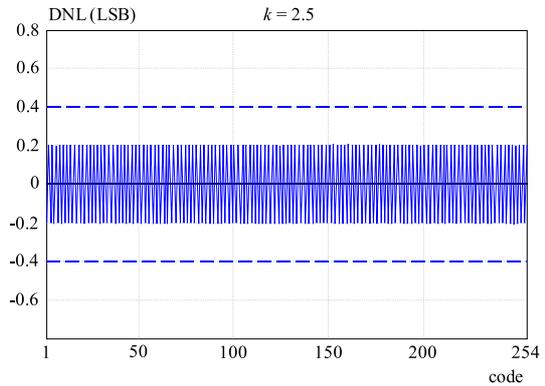


Fig. 7. DNL measurement of an ideal ADC using input slope with  $k = 2.5$

of sample periods ( $k \notin \mathbb{N}$ ), the phase shift  $\theta_{i+1}$  crossing the voltage threshold  $V_{i+1}$  differs from the phase shift  $\theta_i$  crossing the voltage threshold  $V_i$  (depicted by the dashed line in Fig. 4).

By investigating the phenomenon more closely, we noticed that by varying the phase shift  $\theta_i$  two distinct oscillation periods occur. It can be shown [16] that this results in the DNL measurement uncertainty  $\Delta$

$$\Delta = \pm \frac{1}{K} . \tag{2}$$

We demonstrate this uncertainty in the following examples.

### 5 EXPERIMENTAL RESULTS

Using the developed Matlab Simulink environment we performed numerous experiments measuring the DNL of an ideal 8-bit ADC with different input signal slopes. The DNL is measured for all non-extreme codes.

In Fig. 5 the DNL measurement in the case of coherent sampling (with  $k = 2$ ) is depicted. The upper bound of the measurement uncertainty is depicted by a dashed line. As expected, determined DNL of each code is exact and equals to 0.

Figures 6, 7, and 8, present DNL measurement using input slopes with  $k$  equal to 2.1, 2.5, and 2.9, respectively.

While the slope of the input signal remains the same during the experiment and the code widths are equal in the case of ideal ADC, the phase shifts for each code differ. This manifests in two different oscillation periods in the whole ADC range and consequently in two different DNL values. While the DNL for the ideal ADC is 0, the measured DNL deviates from the exact value. The dashed line represents the upper bound of the measurement uncertainty.

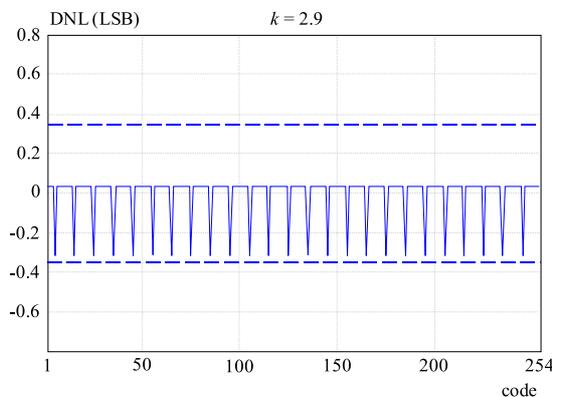


Fig. 8. DNL measurement of an ideal ADC using input slope with  $k = 2.9$

The dependency between the input signal slope expressed by  $k$  (number of samples required for traversing

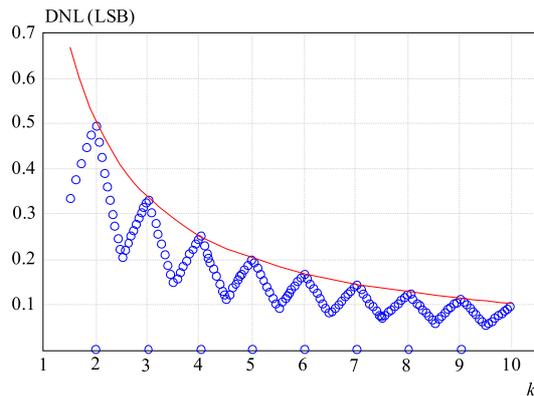


Fig. 9. Measured DNL of an ideal ADC using OB T with different input slopes

the code width) and measured DNL of an ideal ADC is depicted in Fig. 9. The DNL of the ADC is composed of maximum values of the DNLs of individual codes. The upper bound of the DNL measurement uncertainty is depicted by the solid line. Measured DNLs for the considered slopes are depicted by marks.

## 6 CONCLUSIONS

The measurement uncertainty of the classical OB T techniques is related to the uncertainty of the measurement of the oscillation period and is determined by oversampling ratio  $T_{osc}/T_s$ . In the case of ADC OB T, however, the measurement of oscillation period is precise, but due to the arbitrary input signal phase shift and non-coherent input signal two oscillation periods are possible. This in turn manifests itself as a measurement uncertainty as demonstrated in the paper. So far, the experiments were performed only assuming ideal ADC. The developed environment enables us to study the measurement conditions in more realistic circumstances. Theoretically, nonlinearities of ADC do not contribute to the measurement uncertainty. In this case, however, the coherent sampling is not possible. On the other hand, noise is expected to worsen measurement accuracy. Their impact in practice is currently being studied.

## REFERENCES

- [1] ARABI, K.—KAMINSKA, B.: Oscillation-Test Strategy for Analog and Mixed-Signal Circuits, Proc. VLSI Test Symposium yr1996, 476–482.
- [2] ARABI, K.—KAMINSKA, B.: Design for Testability of Integrated Operational Amplifiers Using Oscillation-Test Strategy, Proc. ICCD (1996), 40–45.
- [3] ARABI, K.—KAMINSKA, B.: Testing Analog and Mixed-Signal Integrated Circuits Using Oscillation-Test Method, IEEE Transactions on CAD **16** No. 7 (1997), 745–753.
- [4] HUERTAS, G.—VAZQUEZ, D.—RUEDA, A.—HUERTAS, J. L.: Effective Oscillation-Based Test for Application to a DTMF Filter Bank, Proc. IEEE ITC (1999), 549–555.
- [5] SANTO ZARNIK, M.—NOVAK, F.—MACEK, S.: Design of Oscillation-Based Test Structures for Active RC Filters, IEEE Proc.—Circuits Devices Syst. **147** No. 5 (2000), 297–302.

- [6] DIAS, P. M.—FRANCA, J. E.—PAULINO, N.: Oscillation Test Methodology for a Digitally-Programmable Switched-Current Biquad, Proc. IEEE Int'l Mixed Signal Testing Workshop, 1996, pp. 221–226.
- [7] ARABI, K.—KAMINSKA, B.: Oscillation Built-in Self Test (OBIST) Scheme for Functional and Structural Testing of Analog and Mixed-Signal Integrated Circuits, Proc. International Test Conference, 1997, pp. 786–795.
- [8] HUERTAS, G.—VAZQUEZ, D.—RUEDA, A.—HUERTAS, J. L.: Oscillation-Based Test in Bandpass Oversampled A/D Converters, Microelectronics Journal **34** No. 10 (2003), 927–936.
- [9] HUERTAS, J. L.: Test and Design-for-Testability in Mixed-Signal Integrated Circuits, Kluwer Academic Publishers, Dordrecht, 2004.
- [10] SANCHEZ, G. H.—DE LA VEGA, D. V. G.—RUEDA, A. R.—DIAZ, J. L. H.: Oscillation-Based Test in Mixed-Signal Circuits, Springer, Dordrecht, 2006.
- [11] SANTO ZARNIK, M.—NOVAK, F.—MACEK, S.: Efficient Go No-Go Test of Active RC Filters, Int. J. of Circuit Theory and Applications **26** No. 5 (1998), 523–529.
- [12] HUERTAS, G.—VAZQUEZ, D.—PERALIAS, E. J.—RUEDA, A.—HUERTAS, J. L.: Testing Mixed-Signal Cores: a Practical Oscillation-Based Test in an Analog Macrocell, IEEE Design & Test of Computers, **19** No. 6 (2002), 73–82.
- [13] RAGHUNATHAN, A.—SHIN, H. J.—ABRAHAM, J. A.—CHATTERJEE, A.: Prediction of Analog Performance Parameters Using Oscillation Based Test, 22<sup>nd</sup> IEEE VLSI Test Symposium (VTS), 2004, pp. 377–382.
- [14] RAGHUNATHAN, A.—CHUN, J. H. P.—ABRAHAM, J. A.—CHATTERJEE, A.: Quasi-Oscillation Based Test for Improved Prediction of Analog Performance Parameters, Proc. Int. Test Conference, 2004, pp. 252–261.
- [15] VAZQUEZ, D.—HUERTAS, G.—LEGER, G.—RUEDA, A.—HUERTAS, J. L.: Practical Solutions for the Application of the Oscillation-Based-Test: Start-Up and On-Chip Evaluation, Proc. 20<sup>th</sup> IEEE VLSI Test Symposium (VTS), 2002, pp. 433–438.
- [16] MRAK, P.—BIASSIZO, A.—NOVAK, F.: Measurement Accuracy of Oscillation Based Test of Analog-To-Digital Converters, ETRI Journal **32** No. 1 (2010), 154–156.

Received 28 May 2011

**Peter MRAK** gained his PhD degree at Jožef Stefan International Postgraduate School, Ljubljana. He is with Gorenje d.d. where he is a member of research and development Department of refrigeration appliances. His research interests include electronic test, system diagnosis, control of cooling systems and quality control.

**Anton BIASSIZO** has been a researcher at the Jožef Stefan Institute since 1991. He received a PhD degree from the University in Ljubljana in 1998. His research interests include efficient algorithms for sequential diagnosis, constraint logic programming, model-based diagnosis and automatic test-pattern generation.

**Franc NOVAK** gained BSc, MSc, and PhD degrees in electrical engineering from the University in Ljubljana in 1975, 1977, and 1988, respectively. Since 1975 he has been with the Joef Stefan Institute, where he is currently head of the Computer Systems Department. Since 2010 he is also full professor at the Faculty of Electrical Engineering and Computer Science, University of Maribor. His research interests are in the areas of electronic testing and diagnosis, and fault-tolerant computing. His most recent assignment has been on designs for the testability of analogue circuits.