

PERFORMANCE ENHANCEMENT OF EMBEDDED SYSTEM BASED MULTILEVEL INVERTER USING GENETIC ALGORITHM

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This paper presents an optimal solution for eliminating pre specified order of harmonics from a stepped waveform of a multilevel inverter topology with equal dc sources. The main challenge of solving the associated non linear equation which are transcendental in nature and therefore have multiple solutions is the convergence of the relevant algorithms and therefore an initial point selected considerably close to the exact solution is required. The paper describes an efficient genetic algorithm that reduces significantly the computational burden resulting in fast convergence. An objective function describing a measure of effectiveness of eliminating selected order of harmonics while controlling the fundamental component is derived. The performance of cascaded multilevel inverter is compared based on computation of switching angle using Genetic Algorithm as well as conventional Newton Raphson approach. A significant improvement in harmonic profile is achieved in the GA based approach. A nine level cascaded multi level inverter is simulated in MATLAB Simulink and a proto type model has been fabricated to validate the simulation results.

Key words: multi level inverter, selective harmonic elimination, genetic algorithm, total harmonic distortion

1 INTRODUCTION

Nowadays high quality power is needed for medical, research and industrial applications to bring into being good quality results and for accurate evaluation. In this paper, an attempt has been made to improve the quality of power. A single phase nine level cascaded multi level inverter with identical dc supply is designed to reduce the harmonic components of the output voltage. Multilevel inverters continue to receive more and more attention because of their high voltage operation capability, low switching losses, high efficiency and low output of electromagnetic interference (EMI). The preferred output of a multilevel inverter is synthesized by several sources of dc voltages. With an increasing number of dc voltage sources, the inverter voltage waveform approaches a nearly sinusoidal waveform while using a low switching frequency scheme. This results in low switching losses, and because several dc sources are used to synthesize the total output voltage, each experiences a lower dv/dt compared to a single level inverter. Consequently, the multilevel inverter technology is a promising technology for high power electric devices such as utility applications [1–4].

Various multilevel inverters structures are reported in the technical literature, such as: diode clamped multilevel inverters (neutral clamp), capacitor clamp multilevel inverter (flying capacitor), cascaded multilevel with separate dc sources and hybrid inverters that are derived from the above mentioned topologies with the aim to reduce the amount of semi conductor elements.

Multilevel voltage source inverter using cascaded inverters with separate dc sources (SDCSs), hereafter called a cascaded multilevel inverter appears to be superior to other multi level structures in term of its structure that is not only simple and modular but also requires the least number of output voltage levels without undue increase in power circuit complexity. In addition, extra clamping diodes or voltage balancing capacitors are not necessary. An important key in designing an effective and efficient cascaded H-bridge multilevel inverter is to ensure that the total harmonic distortion (THD) in the output voltage waveform is small enough [3]. It is worth noting that in most of the works reported in the technical literature, the level of the dc sources was assumed to be equal and constant, which is probably not to be case in application even if the sources are nominally equal [8].

Selective Harmonic Elimination Pulse Width Modulation (SHE-PWM) has been intensively studied in order to achieve low THD, [6]. The common characteristic of the SHE-PWM method is that the waveform analysis is performed using Fourier theory [14]. Sets of non-linear transcendental equations are then derived, and the solution is obtained using an iterative procedure, mostly by Newton-Raphson method [5]. This method is derivative dependent and may end in local optima; however, a judicious choice of the initial values alone guarantees convergence [6, 7, 13].

In this paper, a multilevel inverter based on the cascaded converter topology with equal dc sources is studied. The main objective of this paper is to introduce a minimization technique assisted with Genetic Algorithm

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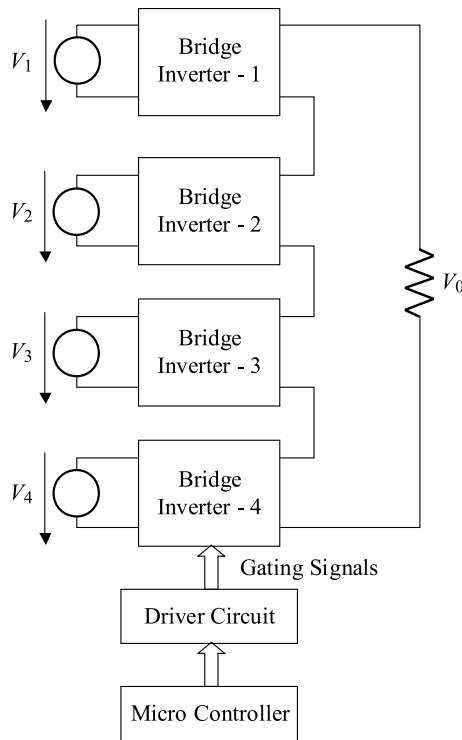


Fig. 1. Block diagram for cascaded multilevel inverter

(GA) [15] in order to reduce the computational burden associated with the solution of the nonlinear transcendental equations of the selective harmonic elimination method. An accurate solution is guaranteed even for a number of switching angles that is higher than other techniques would be able to calculate for a given computational effort. Hence it seems to be a promising method for applications when a high number of dc sources are sought in order to eliminate more low order harmonics to further reduce the THD, [9, 10, 12].

This paper is organized as follows. Section 2 describes the structure of a cascaded multilevel inverter and its switching pattern. Section 3 presents the formation of problem along with analysis for the generalized stepped voltage waveform. Section 4 describes the conventional Newton Raphson method and corresponding simulation results. The proposed genetic algorithm method along with the simulation and hardware results are presented in Section 5. Finally conclusions are summarized in Section 6.

2 CASCADED H-BRIDGE MULTILEVEL INVERTER

Among three types of topologies cascaded type multilevel inverter is considered for this work. In this configuration, four single phase H-bridges are serially connected for nine-level inverter. In general the number of bridges required for an m level inverter is $(m - 1)/2$. All

the switches in the inverter are turned on only at the fundamental frequency and the voltage stress across the switches is only the magnitude of dc source voltage. In the cascaded multilevel inverter all the voltage sources need to be isolated from one another. Thus for nine-level inverter four dc sources are needed. The switching stress can be reduced because of its better switch utilization. In the proposed system, identical dc source voltages are used for the four H-bridges of the multi-level inverter. The block diagram of single phase cascaded nine level inverter is shown in Fig. 1. Each bridge module comprises of four Metal Oxide Semi Conductor Field Effect Transistors (MOSFET). Each bridge is energized by separate sources. The cascaded multilevel inverter consists of a series of H-bridge (single phase, full bridge) inverter units. As mentioned, the general function of this multilevel inverter is to synthesize a desired voltage from several separate dc sources which may be obtained from batteries, fuel cells, solar cells or ultra capacitors.

2.1 Structure of Single Phase Cascaded Multilevel Inverter

Each separate dc sources is connected to a single-phase full-bridge inverter. Each inverter level can generate three different voltage outputs which are $+V_{dc}$, 0 , $-V_{dc}$. The ac output of each levels full bridge inverter is connected in series such that the synthesized voltage waveform is the sum of all of the individual inverter outputs. The number of output phase voltage level in a cascaded multilevel inverter is then $2s+1$, where s is the number of dc sources. With enough levels and appropriate switching algorithm the multilevel level results in an output voltage waveform which is almost sinusoidal.

Table 1. Output voltage levels and their switching states for nine-level inverter

Switches	Output Voltage (V_0)			
	V_1	$V_1 + V_2$	$V_1 + V_2 + V_3$	$V_1 + V_2 + V_3 + V_4$
M_{11}	1	1	1	1
M_{12}	1	1	1	1
M_{13}	0	0	0	0
M_{14}	0	0	0	0
M_{21}	0	1	1	1
M_{22}	1	1	1	1
M_{23}	0	0	0	0
M_{24}	0	0	0	0
M_{31}	0	0	1	1
M_{32}	1	1	1	1
M_{33}	0	0	0	0
M_{34}	0	0	0	0
M_{41}	0	0	0	1
M_{42}	1	1	1	1
M_{43}	0	0	0	0
M_{44}	0	0	0	0

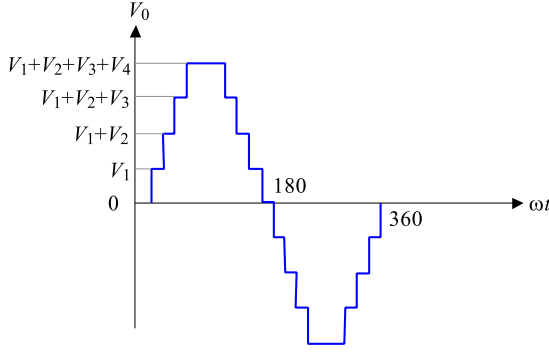


Fig. 2. Output voltage of single phase cascaded nine-level inverter

2.2 Principle of Working of Nine Level Inverter

The model output voltage waveform of nine-level cascaded multilevel inverter is shown in the figure 2.2. The maximum output phase voltage is given as $V_0 = V_1 + V_2 + V_3 + V_4$.

The steps to synthesize the nine-level voltage waveforms are as follows.

1. For an output voltage level $V_0 = 0$, no switch in the H-bridges are turned on.
2. For an output voltage level $V_0 = V_1$, turn on the switches M_{11} , M_{12} , M_{22} , M_{32} , M_{42} .
3. For an output voltage $V_0 = V_1 + V_2$, turn on all the switches as mentioned in step 2 and M_{21} .
4. For an output voltage level $V_0 = V_1 + V_2 + V_3$, turn on all the switches in the step 3 and M_{31} .
5. For an output voltage level $V_0 = V_1 + V_2 + V_3 + V_4$, turn on all the switches in the step 3 and M_{41} .

where M_{ij} is the switches in the individual bridge. i is the number of bridge and j switch number in the inverter.

Table 1 shows the voltage levels and their corresponding switch states in one quarter cycle of output voltage. State condition 1 means the switch is on and 0 means the switch is off. Each switch is turned on only once per cycle and therefore reduces switching losses.

3 HARMONIC MINIMIZATION PROBLEM IN MULTI LEVEL INVERTER

3.1 Switching States of inverter and Expression of output voltage

The output voltage waveform of cascaded multi level inverter has m levels. The problem under consideration is to find appropriate switching angles namely θ_1 , θ_2 , $\theta_3 \dots \theta_n$ so that the $n - 1$ non-triplen odd harmonics can be eliminated and control of the fundamental is also achieved. The Fourier series expansion of the SHE-PWM waveform is given by equation 1 assuming all the dc sources are equal value.

The Fourier expansion is used to find the expression for the output voltage of the multi level inverter. The output voltage of the single phase cascaded nine-level inverter is

shown in Fig. 2. There are five levels in the quarter wave of the output voltage waveform including the level zero. As per the Fourier theorem the periodic output voltage $V(\omega t)$ can be described by a constant term plus an infinite series of sine and cosine terms of frequency $n\omega$, where n is an integer.

Therefore $V(\omega t)$ in general, can be expressed as

$$V(\omega t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} (a_n \cos n\omega t + b_n \sin n\omega t). \quad (1)$$

Because of the output voltage of the multilevel inverter is quarter wave symmetry, the Fourier series constants a_0 , a_n become zero and only b_n is to be calculated. The value of b_n is found using the equations (2) and (3)

$$b_n = \frac{1}{\pi} \int_0^{2\pi} v_0(\omega t) \sin n\omega t d(\omega t), \quad (2)$$

$$b_n = \frac{1}{\pi} \left[\int_{\theta_1}^{\theta_2} v_1 \sin n\omega t d(\omega t) + \int_{\theta_2}^{\theta_3} (v_1 + v_2) \sin n\omega t d(\omega t) + \int_{\theta_3}^{\theta_4} (v_1 + v_2 + v_3) \sin n\omega t d(\omega t) + \int_{\theta_4}^{\frac{\pi}{2}} (v_1 + v_2 + v_3 + v_4) \sin n\omega t d(\omega t) \right]. \quad (3)$$

By finding the constants b_n , and substituting in equation (1) The Fourier expression for the output voltage of the single phase nine-level inverter is obtained as,

$$V(\omega t) = \sum_{n=1,3}^{\infty} \frac{4}{n\pi} (v_1 \cos n\theta_1 + \dots + v_s \cos n\theta_s) \sin \omega t \quad (4)$$

where s is the number of dc sources.

$$V(\omega t) = \sum_{n=1,3}^{\infty} \frac{4V_{dc}}{n\pi} (\cos n\theta_1 + \dots + \cos n\theta_s) \sin \omega t. \quad (5)$$

Assuming all sources are of equal value ($V_1 = V_2 = V_3 = V_4 = V_{dc}$).

3.2 Estimation of Switching Angles

Fourier series of the quarter-wave symmetric SH-bridge multilevel inverter output waveform is written as given in equation (6) in which θ_s are the optimized switching angles, which must satisfy the following condition

$$\theta_1 < \theta_2 < \dots < \theta_s < \pi/2.$$

The method to solve the optimized harmonic switching angles will be explained in this section. From equation (1), the harmonic components in the waveform can be described as follows:

1. The amplitude of dc component equals zero.

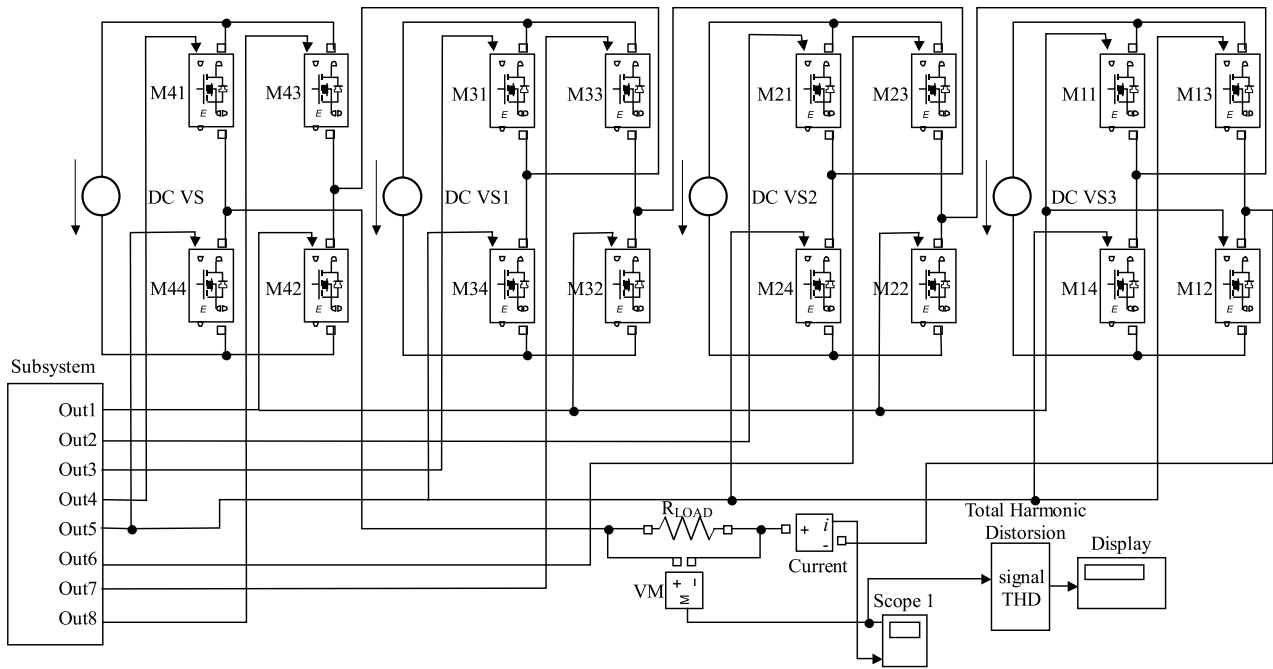


Fig. 3. Simulation circuit for nine level inverter using PWM technique

2. The amplitude of all odd harmonic components including fundamental one, are given by

$$h(n) = \frac{4V_{dc}}{n\pi} \sum_{k=1}^s \cos n\theta_k. \quad (6)$$

3. The amplitude of all even harmonics equal zero. Thus, only the odd harmonics in the quarter-wave symmetric multilevel waveform need to be eliminated.

The switching angles of the waveform will be adjusted to get the lowest THD in the output voltage

$$h(n) = \frac{4V_{dc}}{n\pi} [\cos \theta_1 + \cos \theta_2 + \cos \theta_3 + \cos \theta_4]. \quad (7)$$

If needed to control the peak value of the output voltage to be V_1 and eliminate the fifth and seventh order harmonics, the modulation index is given by $M = \frac{\pi V_1}{4V_{dc}}$, the resulting harmonic equations are

$$\frac{4V_{dc}}{\pi} [\cos \theta_1 + \cos \theta_2 + \cos \theta_3 + \cos \theta_4] = V_1, \quad (8)$$

$$\cos 5\theta_1 + \cos 5\theta_2 + \cos 5\theta_3 + \cos 5\theta_4 = 0, \quad (9)$$

$$\cos 7\theta_1 + \cos 7\theta_2 + \cos 7\theta_3 + \cos 7\theta_4 = 0, \quad (10)$$

Equation (8) is rewritten as

$$\cos \theta_1 + \cos \theta_2 + \cos \theta_3 + \cos \theta_4 = M. \quad (11)$$

Each H-bridge inverter unit has a conduction angle which is calculated to minimize the harmonic components. The conduction angles are the factors determining the amplitude of the harmonic components. This paper

deals with a four H-bridge cascaded inverter because its 9-level output voltage can be almost sinusoidal. In that case the conventional method can eliminate the 5th and 7th harmonics except for the fundamental wave. In nine level inverter four dc sources are needed so that the dc voltage levels are chosen so as not to generate the fifth and seventh order harmonics while achieving the desired fundamental voltage.

This is a system of three simultaneous equations with four unknowns $\theta_1, \theta_2, \theta_3$ and θ_4 . These values are found by solving the simultaneous equations (8–10).

4 CONVENTIONAL METHOD FOR HARMONIC REDUCTION

4.1 Newton Raphson Method

The conventional method has the merit of eliminating the required harmonic component but it has some problems. First it is difficult to solve simultaneous equations which are a set of nonlinear transcendental equations. These equations can be solved by an iterative method such as Newton–Raphson. If the number of simultaneous equations increases so does the time and the amount of calculations to obtain the conduction angles. Moreover the method is an approximate one depending on the iteration which leads to the inclusion of some errors. Secondly conducting angles are calculated through an off-line operation. Therefore they have to be arranged in the look-up table. It needs much data in order to implement switching angles with an accurate resolution. If the scale of the modulation index is divided in detail, the data of the conducting angles increases. In other words,

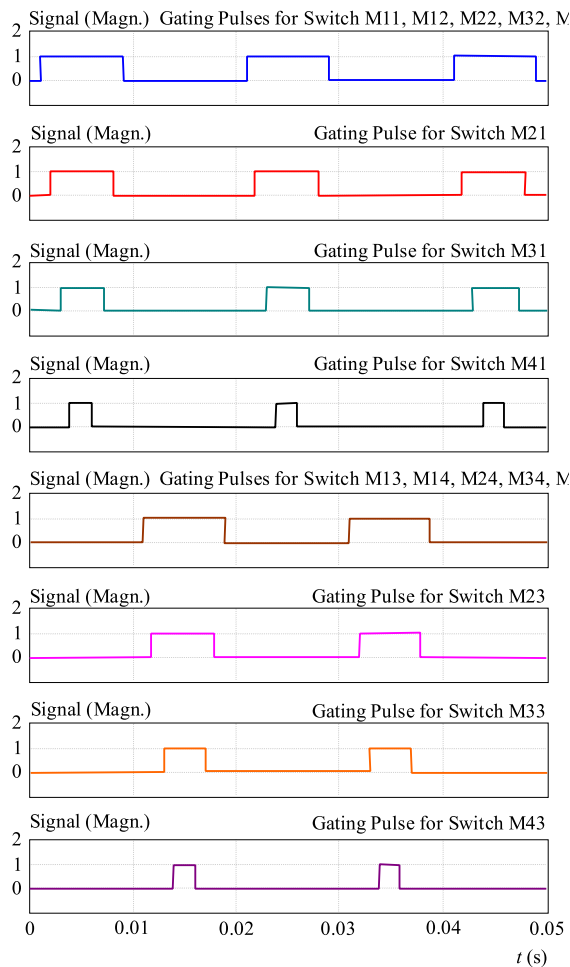


Fig. 4. Pattern of gating signals

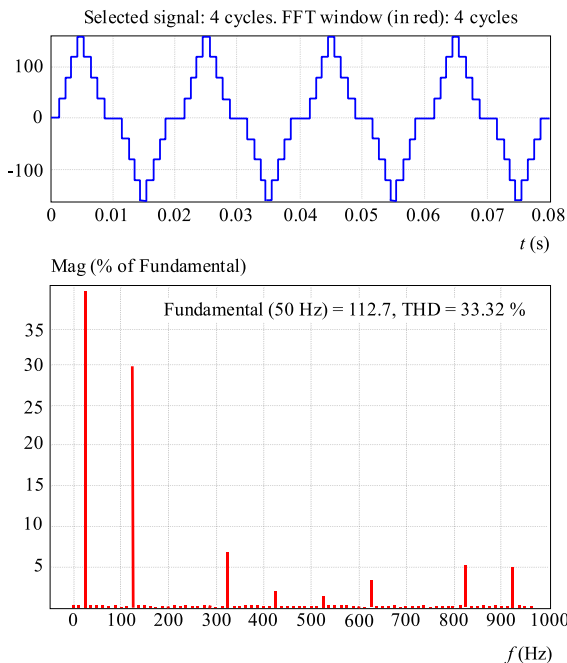


Fig. 5. FFT analysis for nine level inverter using Newton raphson method

method has a limitation in its application to an adjustable motor drive. The conventional method does not solve the set of non linear transcendental equations but calculates several trigonometric functions.

The objective is to choose the levels of the dc voltages so as to get the required fundamental voltages V_1 and specific higher order harmonics of $V(\omega t)$ equals to zero.

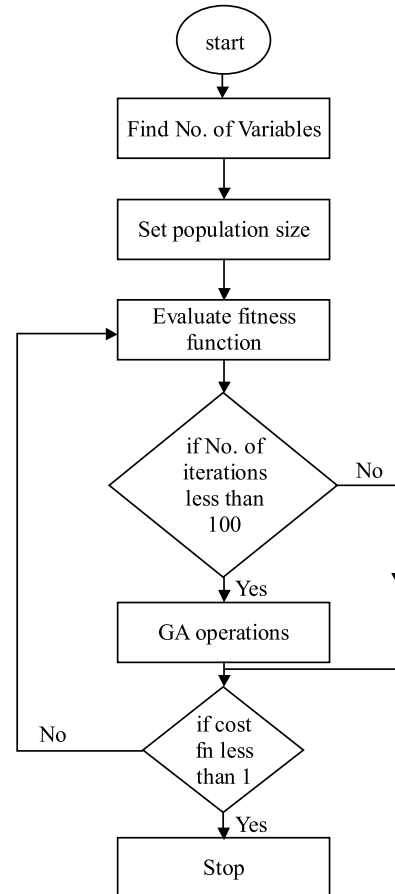


Fig. 6. Flow chart

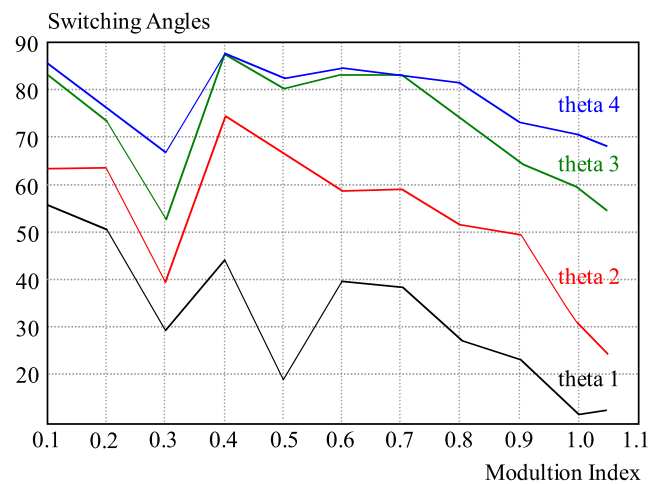


Fig. 7. Modulation indices vs Corresponding switching angles

the data of the conducting angles depends on the resolution of the modulation index. Therefore the conventional

The circuit shown in Fig. 3 is simulated and the results are presented in Fig. 4 and Fig. 5.

4.2 Simulation Circuit for Nine Level Inverter

The single phase cascaded nine level inverter using PWM technique and switching angle variation technique are simulated with the use of MATLAB R2007b. For nine level inverter three H-bridges are needed for simulation. MOSFET switches are used as power switches. Figure 3 shows the simulation circuit for nine level inverter using PWM technique.

4.3 Simulation Results

Figure 6 shows the circuit which is simulated in Matlab simulink package. The supply voltage in each H-bridge is 40 V and MOSFET is used as power switch. The load is considered as pure resistance $50\ \Omega$. The switching angles are obtained using GA approach in the off line.

Figure 4 shows the gating signals generated in simulink for the power circuit shown in Fig. 3.

Figure 5 shows output voltage waveform of the nine level inverter and the harmonic profile of the output voltage when the power circuit is simulated with switching angles calculated by Newton-Raphson method.

4.4 Limitations of Conventional Method

- The solution obtained depends on the initial guess and no guarantee to be optimum.
- It has computational burden and is time consuming.
- More than one solution is possible with different modulation indices.
- To obtain convergence with the numerical technique, the starting values must be selected considerably close to exact solution.
- It is difficult to presume the starting values. Divergence problem may occur.

5 PROPOSED TECHNIQUE FOR SWITCHING ANGLE GENERATION

5.1 Genetic Algorithm to calculate optimum switching Angles

The limitations of the Newton Raphson method is eliminated by using genetic algorithm based optimization technique. The switching angles are determined using GA. The steps for formulating a problem and applying a GA are as follows:

1. Select binary or floating point strings.
2. Find the number of variables specific to the problem; this number will be the number of genes in a chromosome. In this application the number of variables is the number of controllable switching angles which is the number of H-bridges in a cascaded multilevel inverter. A nine-level inverter requires four H-bridges; thus, each chromosome for this application will have four switching angles, *ie*, $(\theta_1, \theta_2, \theta_3, \theta_4)$.

3. Set a population size and initialize the population. Higher population might increase the rate of convergence but it also increases the execution time. The selection of an optimum-sized population requires some experience in GA.

The population in this paper has 20 chromosomes, each containing four switching angles. The population is initialized with random angles between 0 degree and 90 degree taking into consideration the quarter-wave symmetry of the output voltage waveform.

4. The most important item for the GA to evaluate the fitness of each chromosome is the cost function. The objective of this study is to minimize specified harmonics; therefore the cost function has to be related to these harmonics. In this work the fifth and seventh harmonics at the output of a nine-level inverter are to be minimized. Then the cost function (f) can be selected as the sum of these two harmonics normalized to the fundamental,

$$f(\theta_1, \theta_2, \theta_3, \theta_4) = 100 \frac{|V_5| + |V_7|}{V_1}. \quad (12)$$

For each chromosome a multilevel output voltage waveform is created using the switching angles in the chromosome and the required harmonic magnitudes are calculated using FFT techniques.

The fitness value (FV) is calculated for each chromosome inserting. In this case,

$$FV(\theta_1, \theta_2, \theta_3, \theta_4) = 100 \frac{|V_5| + |V_7|}{V_1}. \quad (13)$$

The switching angle set producing the maximum FV is the best solution of the first iteration.

5. The GA is usually set to run for a certain number of iterations (100 in this case) to find an answer. After the first iteration, FVs are used to determine new offspring. These go through crossover and mutation operations and a new population is created which goes through the same cycle starting from FV evaluation.

Sometimes, the GA can converge to a solution well before 100 iterations are completed. To save time, in this paper, the iterations have been stopped when the absolute value of the cost function goes below 1, in which case the sum of the fifth and the seventh harmonics is negligible compared to the fundamental. Note that after these iterations, the GA finds one solution; therefore, it has to be run as many times as the number of solutions required to cover the whole modulation index range. The algorithm to find the optimum switching angles is described through the flow chart shown in Fig. 6.

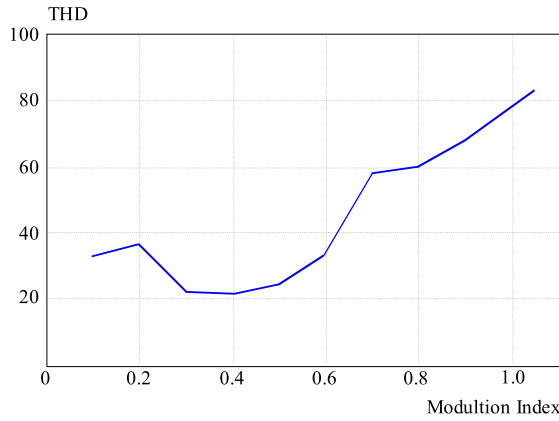


Fig. 8. Modulation indices vs THD

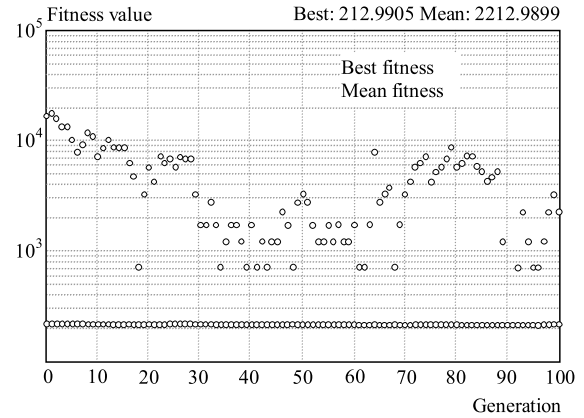


Fig. 9. GA result for fitness vs generations

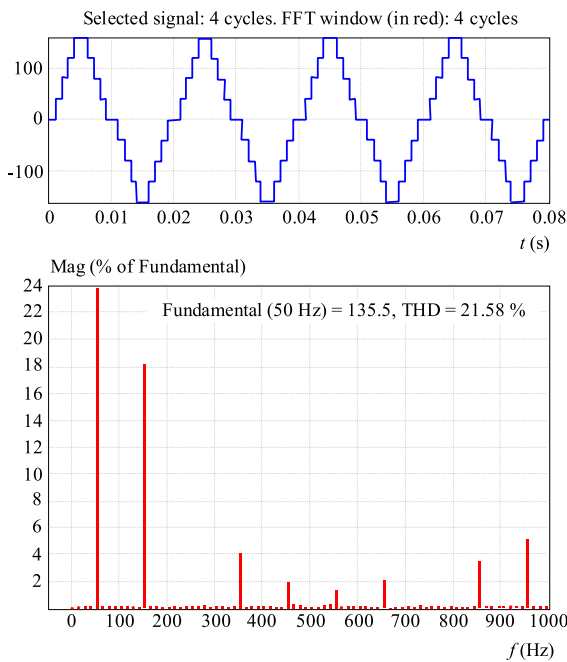


Fig. 10. FFT analysis for nine level inverter using GA

5.2 Simulation Results

For the nine level inverter, switching angles which minimize the fifth and seventh order harmonics are shown in Tab. 2. for various ranges of modulation indices using GA. The graph given in Fig. 7. Shows the variation of switching angle with respect to modulation indices. The graph shown in Fig. 8. gives the values of THD for the various ranges of modulation indices.

Figure 9 shows the fitness values for various generations.

The power circuit shown in Fig. 3 is simulated using the switching angles estimated from genetic algorithm. Figure 10 shows the output voltage waveform and its harmonic profile. From the spectrum analysis it is inferred that the THD in GA based is 21.58 % and that for Newton-Raphson is 33.32 %.

By comparing the two Figs. 5 and 10 it is clearly identified that the harmonics are reduced effectively by com-

puting the switching angles by GA compared to Newton Raphson method.

Table 2. Calculated switching angles for various modulation index

Modulation Index Level	Modulation Index	θ_1	θ_2	θ_3	θ_4	THD
High	1.05	12.5	23.8	54.3	67.8	83.3
	1.0	11.8	30.5	59.1	70.5	78.1
	0.90	23.1	49.3	64.5	73.1	67.8
Middle	0.8	27.4	51.6	73.9	81.4	59.7
	0.7	38.5	59	82.8	83.0	58.0
	0.6	39.5	58.6	83.1	84.5	33.3
	0.5	18.9	66.1	80.1	82.3	24.4
Low	0.4	44.1	74.3	87.4	87.6	21.5
	0.3	29.2	39.2	53.0	66.9	22.5
	0.2	50.9	63.3	73.1	76.2	36.2
	0.1	55	63.4	83.0	85.6	32.8

5.3 Hardware Results

A prototype model of nine level cascaded multilevel inverter has been fabricated and tested. The switching signals for the model are generated from 8051 microcontroller. The driver circuits are also used to give pulse for switches in the power circuit. MOSFET switches of rating IRF840, 600 V, 6 A are used in the power circuit. The input voltage $V_{dc} = 40$ V.

The power circuit is isolated by using opto-coupler circuit. Opto-couplers also known as opto isolators provide optical isolation and coupling between control circuit and power circuit, creating physical and electrical isolation signal coupling between them. Opto couplers which can be assembled using traditional semi conductor packages contain a light emitting diode and photo sensitive semiconductor devices (MCT2E) in the same housing.

The pulses for the H-bridge inverters generated from the 8051 micro controller are shown in Figs. 11, 12, 13 and 14 respectively. The inverter output voltage waveform is also shown in Fig. 15 and the corresponding frequency spectrum is shown in Fig. 16.

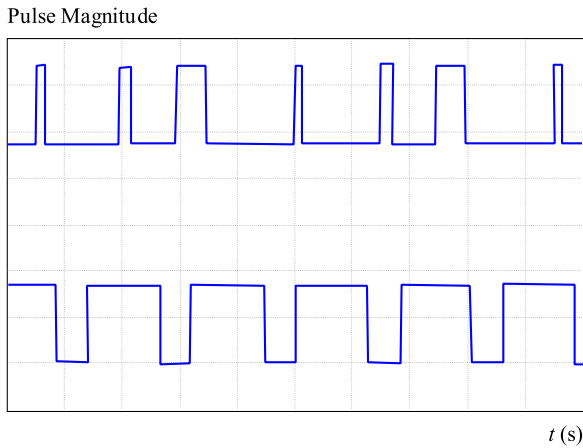


Fig. 11. Pulses for switches $M_{11}, M_{12}, M_{13}, M_{14}$

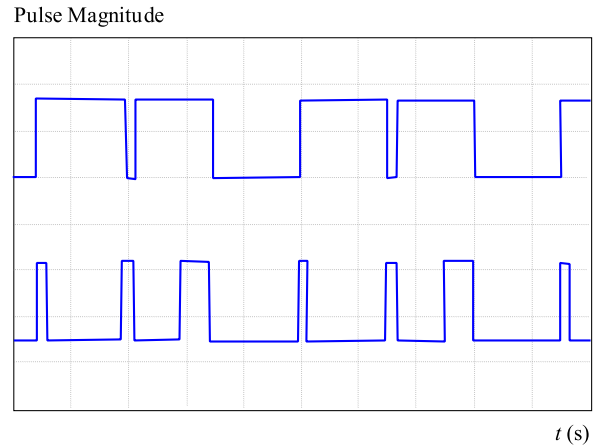


Fig. 12. Pulses for switches $M_{21}, M_{22}, M_{23}, M_{24}$

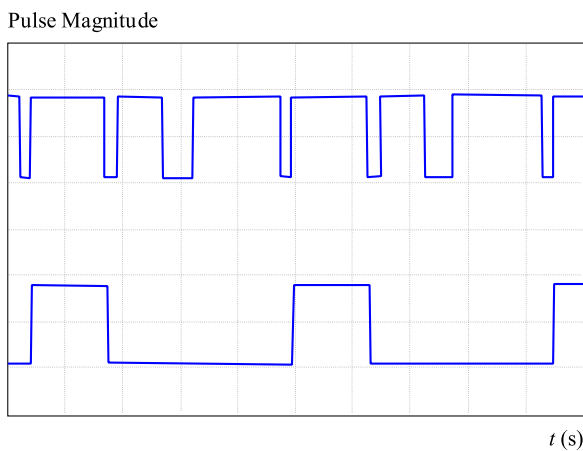


Fig. 13. Pulses for switches $M_{31}, M_{32}, M_{33}, M_{34}$

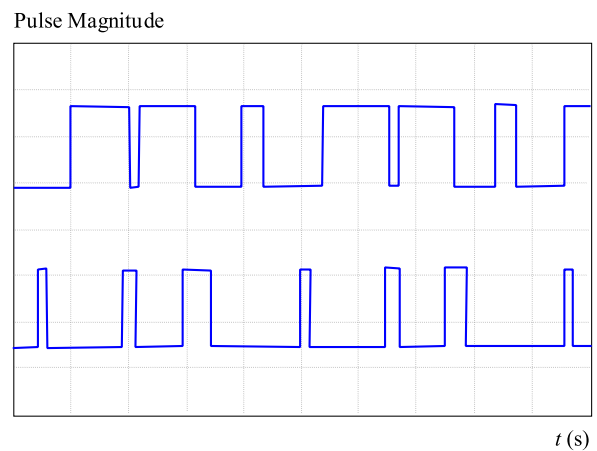


Fig. 14. Pulses for switches $M_{41}, M_{42}, M_{43}, M_{44}$

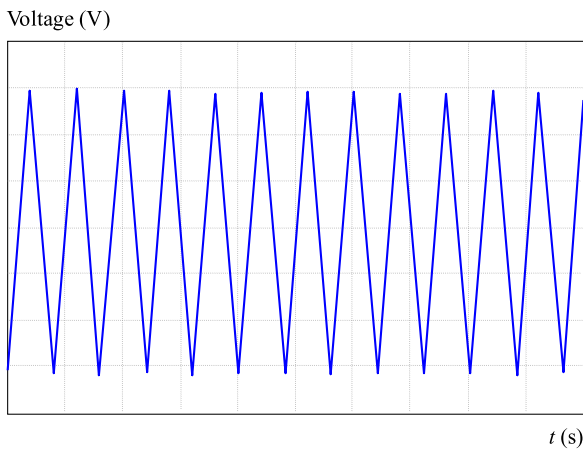


Fig. 15. Output voltage wave form for nine level inverter

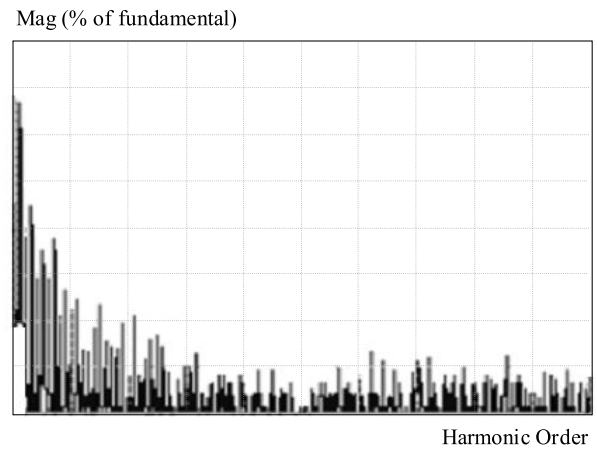


Fig. 16. FFT analysis for the nine level inverter

6 CONCLUSION

In this work genetic algorithm optimization technique is applied to find the switching angles of the cascaded inverter for the reduction of harmonics. The results obtained show that fifth and seventh order harmonics are reduced effectively. GA based solution of switching angles give minimum THD in the output voltage waveform compared with the conventional Newton Raphson method.

As in this approach, GA can be applied to any type of optimization problems. GA reduces the harmonic content more predominantly than any other conventional technique such as Newton Raphson method. This work can be extended by applying GA to reduce the harmonics in inverters with any number of levels. The hardware results are presented and it is found that these results agree with the simulation results.

REFERENCES

- [1] LAI, J. S.—PENG, F. Z.: Multilevel Converters - a New Breed of Power Converters, *IEEE Trans. Ind. Appl.* **32** No. 3 (May/Jun 1996), 509–517.
- [2] RODRÍGUEZ, J.—LAI, J.—PENG, F. Z.: Multilevel Inverters: a Survey of Topologies, Controls and Applications, *IEEE Trans. Ind. Electron.* **49** No. 4 (Aug 2002), 724–738.
- [3] DUFFEY, C. K.—STRATFORD, R. P.: Update of Harmonic Standard IEEE-519; IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems, *IEEE Trans. Ind. Appl.* **25** No. 6 (Nov/Dec 1989), 1025–1034.
- [4] WANG, J.—PENG, F. Z.: Unified Power Flow Controller using the Cascade Multilevel Inverter, *IEEE Trans. Power Electron.* **19** No. 4 (July 2004), 1077–1084.
- [5] ENJETI, P. N.—LINDSAY, J. F.: Solving Nonlinear Equation of Harmonic Elimination PWM in Power Control, *Electron. Lett* **23** No. 12 (June 1987), 656–657.
- [6] CHIASSON, J. N.—TOLBERT, L. M.—McKENZIE, K. J.—DU, Z.: Control of a Multilevel Converter using Resultant Theory, *IEEE Trans. Contr. Syst. Technol.* **11** No. 3 (May 2003), 345–354.
- [7] CHIASSON, J. N.—TOLBERT, L. M.—McKENZIE, K. J.—ZHONG, D.: Elimination of Harmonics in a Multilevel Converter using the Theory of Symmetric Polynomials and Resultants, *IEEE Trans. Contr. Syst. Technol* **13** No. 2 (Mar 2005), 216–223.
- [8] TOLBERT, L. M.—CHIASSON, J. N.—ZHONG, D.—McKENZIE, K. J.: Elimination of Harmonics in a Multilevel Converter with Non Equal dc Sources, *IEEE Trans. Ind. Appl.* **4** No. 1 (Jan-Feb 2005), 75–82.
- [9] SHI, K. L.—HUI LI: Optimized PWM Strategy Based on Genetic Algorithms, *IEEE Trans. Industrial Electronics* **52** No. 5 (Oct 2005), 1458–1461.
- [10] WELL, J. R.—GENG, X.—CHAPMAN, P. L.—KREIN, P. T.—NEE, B. T.: Modulation Based Harmonic Elimination, *IEEE Transactions on Power Electronics* **15** No. 4 (July 2000), 719–725.
- [11] AGELIDIS, V. G.—BALOUKTSIS, A. I.—DAHIDAH, M. S. A.: A Five Level Symmetrically Defined Selective Harmonic Elimination PWM Strategy: Analysis and Experimental Validation, *IEEE Transactions on Power Electronics* **23** No. 1 (Jan 2008), 19–26.
- [12] CHIASSON, J. N.—TOLBERT, L. M.—McKENZIE, K. J.—DU, Z.: A Complete Solution to the Harmonic Elimination Problems, *IEEE Trans. Power Electron* **22**, No. 1 (Jan 2007), 336–340.
- [13] TOLBERT, L. M.—PENG, F. Z.—HABETLER, T. G.: Multilevel PWM Methods at Low Modulation Indices, *IEEE Transactions on Power Electronics* **15** No. 4 (July 2000), 719–725.
- [14] MASWOOD, I.—WEI, S.—RAHMAN, M. A.: A Flexible Way to Generate PWM-SHE Switching Patterns using Genetic Algorithms, in *Proc. IEEE Applied Power Electronics Conf. Expo.*, 2001, pp. 1130–1134.
- [15] HOUCK, J. J.—KAY, M.: The Genetic Algorithm — Optimization Toolbox (GAOT) for MATLAB 7 (Online), <http://www.ie.ncsu.edu/mirage/GAToolBox/gaot>.

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