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MEASURING STATIC PARAMETERS OF EMBEDDED ADC CORE

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The paper presents the results of a feasibility study of measuring static parameters of ADC cores embedded in a System-on-Chip. Histogram based technique is employed because it is suitable for built-in self-test. While the theoretical background of the technique has been covered by numerous papers, less attention has been given to implementations in practice. Our goal was the implementation of histogram test in a IEEE Std 1500 wrapper. Two different solutions pursuing either minimal test time or minimal hardware overhead are described. The impact of MOS switches at ADC input on the performed measurements was considered.

K e y w o r d s: ADC static parameters, histogram based test, built-in self-test, system-on-chip

1 INTRODUCTION

Analog-to-digital converters (ADC) are used in a wide variety of applications including industrial control, consumer electronics and communication systems. ADC testing, which represents a considerable part of the product's cost, is a complex process. Testing is typically specification oriented. Parameters that are measured can be broadly divided into two categories:

- static parameters, related to the transfer function (*ie*, offset, gain, differential nonlinearity (DNL), integral nonlinearity (INL)),
- dynamic parameters which describe the deformation induced on the converted signal (*ie*, total harmonic distortion, signal-to-noise ratio).

Most test strategies today are based on DSP testing where a known stimulus is applied to the device input and its output is processed using, for example, fast Fourier transform techniques to extract dynamic characteristics [1–3]. ADC testing is performed by a specialized hardware such as mixed-signal automatic test equipment (ATE) or an IC tester. As test complexity increases with speed and resolution, and the cost of implementing measurements is becoming excessive, test strategy must be carefully elaborated.

The integration of ADCs in a system-on-chip (SoC) makes the problem of testing even more difficult due to the communication bottleneck in accessing deeply embedded cores from external ATE. Built-in self-test (BIST) of embedded cores has been identified as a potential solution. Simple BIST implementations primarily employ static parameters test. Determination of the dynamic parameters is viable only when a DSP core is available in the SoC and the solution is application dependent.

This paper presents the results of a case study of measuring static parameters of ADC cores embedded in a System- on-Chip (SoC) by histogram based technique. The described approach has been implemented in a IEEE Std 1500 wrapper. The purpose of this paper is to demonstrate the feasibility of the approach by providing implementation details and supporting measurement results.

2 PREVIOUS WORK

Histogram method [3–19] is an established approach for determining the static parameters. In histogram testing, ADC code transition levels are determined through statistical analysis of converter activity. For a known periodic input stimulus, the number of occurrences of each code is recorded over an integer number of input waveform periods. The static parameters of the ADC are determined by correlating the actual records with the theoretical values for the given signal. Sine-wave and triangle-wave are the most common types of the input stimuli because the theoretical values can easily be calculated. The corresponding output code histograms for sine-wave and triangle-wave input signal are depicted in Fig. 1.

Histogram based test of ADCs has been in use for more than two decades and different aspects of its application have been discussed by numerous authors. Earlier references [4–7] primarily concentrate on how the code density can be interpreted to compute the differential and integral nonlinearities, gain error and offset error, and estimate the achieved accuracy under different measurement conditions. More recently, the accuracy of ADC testing with sine- wave stimulus has been analyzed under the assumption of quasi coherent sampling and a bound on the variance of the transition level estimators have been derived in [8]. Error in the estimation of transition voltages in the presence of additive noise has been analyzed in [9]. As a continuation of this work, the error in the code bin widths has been studied, the error of the differential nonlinearity estimation has been analyzed and expressions for the amount of overdrive to minimize the error have been proposed in [10]. Another paper of the same authors [11] analyzes the precision of the estimates of ADC

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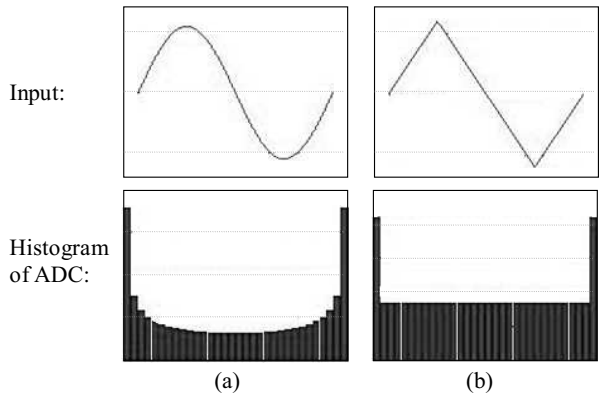

Fig. 1. Output code histograms for (a) sine-wave and (b) triangle-wave input signal

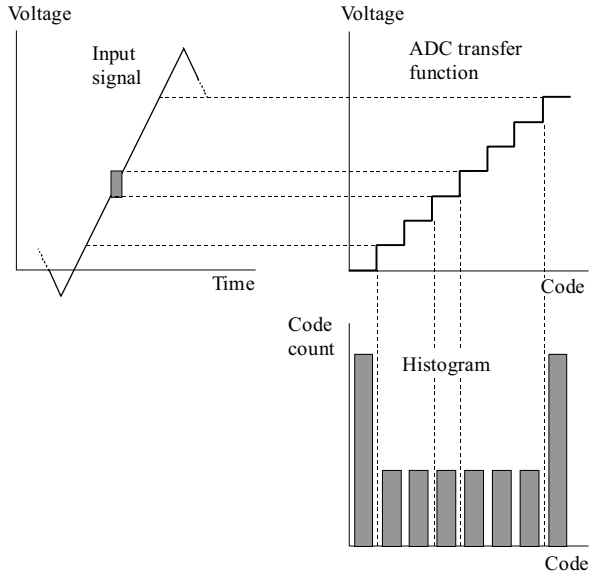

Fig. 2. The principle of histogram based test technique using triangle-wave input signal

gain and offset error that are obtained with the histogram method. An improved histogram based approach which reveals also dynamic performance, such as the effective number of bits, is proposed in [12]. Novel approach based on small-amplitude waves is proposed in [13] and further revised in [14].

Papers [15–17] focus on implementation of histogram based test of ADCs in a BIST arrangement. In general, a complete BIST scheme requires the definition of a reference analog input generator and digital output response analyzer. As on-chip generation of reference stimulus can be regarded as a classical problem with known solutions [18], the authors focus on defining the digital output response analyzer. They employ triangular input waveform and derive the procedures for computation of offset, gain, DNL and INL. The proposed BIST logic which implements the above procedures is verified with simulations for different lengths of ADCs. In [19] some improvements of the above BIST logic are proposed by performing DNL, INL, offset and gain error calculation procedures in parallel.

So far, most of the proposed solutions have been evaluated by simulations. Their application in SoC testing in practice is still an open issue. Paper [20] can be regarded as an attempt towards the implementation in a test wrapper conforming to IEEE Std 1500 [21]. However, the paper describes a general mixed-signal test wrapper design and does not provide any details of possible implementations of test techniques in practice. The lack of reported experimental evidence fostered our work on the design of histogram based test technique in a IEEE Std 1500 wrapper together with a thorough evaluation of the implemented test infrastructure on experimental case studies. We implemented two extreme versions of the histogram based BIST in a IEEE Std 1500 wrapper regarding test time/hardware overhead trade-off, both evaluated by laboratory measurements. In order to provide realistic measurement conditions we introduced external stimuli via analog boundary module of a IEEE Std 1149.4 compliant experimental test chip [22]. Reported work may be helpful in selecting the appropriate test resources for a histogram based test in a SoC.

3 DETERMINATION OF STATIC PARAMETERS OF ADC BY HISTOGRAM METHOD

The histogram test technique is based on a known amplitude distribution. The histogram represents the counts of each ADC code (*ie*, amplitude) for the applied input signal. For BIST implementations, a triangle-wave input signal is the most convenient for static parameter tests or linearity tests, because it can be characterized only by two values (count of extreme codes and count of other codes). The count of extreme codes is normally greater than the count of non-extreme codes due to the overflow of the input signal. The principle is shown in Fig. 2.

For practical reasons, coherent sampling must be provided. Coherent sampling refers to the relationship between the number of samples N, the number of input signal periods M, the sampling frequency f_s and the frequency of the input signal f_{in}. The condition for coherent sampling is given by

$$\frac{N}{M} = \frac{f_{in}}{f_s}\,. \tag{1}$$

In addition, the slope of the input signal is determined by the reference voltage V_{ref}, the number of ADC bits n and the number of input signal periods M. ADC static parameters: offset error, gain, differential nonlinearity (DNL), integral nonlinearity (INL) are calculated on the basis of the counts of ADC codes as shown below.

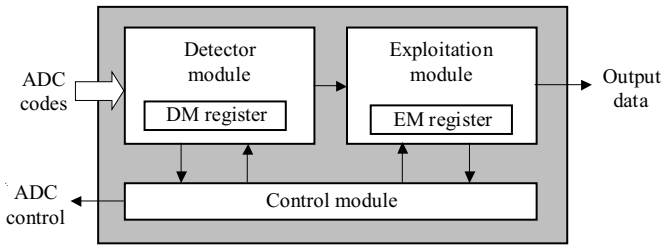

Fig. 3. Sequential BIST structure

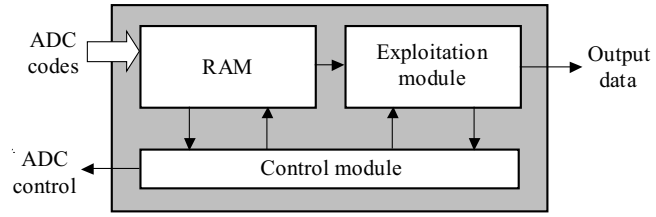

Fig. 4. RAM-based BIST structure

The offset error manifests itself as the deviation of the first actual code transition from 0,5 LSB. The offset error is calculated by

$$\text{Offset} = \frac{H(2^n - 1) - H(0)}{2H_{\text{ideal}}} . \tag{2}$$

In the above expression, $H(2^n - 1)$ is the number of occurrences of MSB code and $H(0)$ is the number of occurrences of LSB code. H_{ideal} represents the count of each code for the ideal ADC and the given stimulus waveform (a triangle-wave, in our case).

The gain error refers to the deviation of slope of the transfer curve. For an ideal ADC, the gain is equal to 1 and the code count for any non-extreme code is equal to H_{ideal}. For a non-ideal ADC, the ratio between the count of a code and the ideal count. H_{ideal} determines the actual ADC gain at that code. In practice, the code counts vary from code to code and the ADC gain is determined by averaging the measured values over m central codes of the range of the ADC

$$Gain^{-1} = \frac{\sum_{i=N_1}^{i=N_2} H(i)}{mH_{\text{ideal}}} . \tag{3}$$

Differential non-linearity (DNL) measures the relative deviation of each code width from the ideal value (1 LSB). In terms of histogram data, *DNL* is defined as the relative difference between the measured and the ideal code counts

$$DNL(i) = \frac{H(i) - H_{\text{ideal}}}{H_{\text{ideal}}} . \tag{4}$$

Integral nonlinearity (*INL*) refers to the deviation of the center of a generated code from the ideal straight center line. The *INL* of a given code i is computed from the cumulative sum of *DNL*s of the previous codes

$$INL(i) = \sum_{j=1}^{i} DNL(j) . \tag{5}$$

The above equations include arithmetic operations that are going be implemented in hardware. While addition and subtraction are quite simple, hardware implementation of division is more demanding. The problem can be avoided, if the denominator is the power of 2. In this case, the division can be performed simply by shifting of the decimal point. Therefore in order to simplify the division in our case, H_{ideal} and m should be the power of 2.

4 IMPLEMENTED BIST STRUCTURES

As mentioned before, we use triangle-wave input signal, which in an ideal case results in a constant code count for non-extreme codes and equal code count for extreme codes. The output of the ADC is processed by the test module, which runs in synchronization with ADC clock. Test module controls the operation of ADC, collects test responses, and computes the static parameters of ADC. For the purpose of possible implementation in a IEEE Std 1500 wrapper, we implemented two different BIST structures targeted either at low hardware overhead or at minimum test time. The first solution denoted as *sequential BIST* performs measurements and computations of static parameters in a sequence of individual steps. The ADC output data is acquired and processed separately for each ADC parameter. The other solution first collects the complete ADC test responses and stores them in a RAM. Next, the computation of static parameters is performed. This solution is denoted as *RAM-based BIST*.

4.1 Sequential BIST approach

The sequential BIST structure shown in Fig. 3 implements the concept proposed in [17] with some additional improvements in order to completely automate the evaluation of the DNL and INL parameters. The BIST structure is composed of three basic blocks: detector module, exploitation module and control module. The detector module monitors the codes generated by the ADC and signals when the code is equal to the preset value. The exploitation module receives the signals from the detector module and performs counting and complementing. The control module coordinates the processing of detector module and exploitation module and connects the BIST structure to the IEEE Std 1500 test infrastructure.

The detector module contains a counter and a comparator. The counter is used for setting the selected code which is then stored in the DM register. The contents of the DM register is compared with the ADC code. When

the ADC code equals the contents of the DM register, exploitation module is triggered. The exploitation module is an up/down counter with clear. Its contents represent the number of occurrences of the selected ADC code. In addition it is capable to calculate the complement of the current value. The temporary result is stored in the EM register. In the pseudo-code given below, the contents of the DM register, ADC code and the contents of the EM register are denoted by DM, ADC and EM, respectively.

Offset calculation. In reference to expression (2), the offset is determined as a difference of the number of occurrences of the two extreme codes divided by 2 H_{ideal}. This is achieved by first initializing the EM register to 0 and then increasing its contents when the ADC code is "11 ... 1 and decreasing it when the code is "00 ... 0. Assuming that $H_{\text{ideal}} = 2^p$ the division by 2 H_{ideal} is implemented as a $(P+1)$ shift operation. The procedure of the computation of offset is:

```
initialization: EM=0
for samples i=1 to N {
  if (ADC_LSB=1) {
    DM=11...1;
    if (ADC = DM) EM++
  }
  else {
    DM = 00...0
    if (ADC = DM) EM--
  }}
if (EM_MSB=1) complement EM
offset = EM ≫ (P+1) //division performed as shift
```

Gain calculation. The inverse of gain is determined as the ratio between the average count of m central codes and H_{ideal}. Again m is selected as a power of 2 ($m = 2^Z$) so that the division is performed as a shift operation. Let us denote the first of the m central codes by N_1 and the last by N_2 ($N_2 = N_1 + m - 1$). The procedure of the computation of the inverse of the gain is:

```
initialization: DM=N1, EM=0
while (DM ≤ N2 ){
  for samples i=1 to N{
    if (ADC = DM) EM++
    }
  DM++
}
gain = EM ≫ (P+Z) // division performed as shift
```

DNL calculation. This calculation is a bit different from the procedure proposed in [16] in order to reduce arithmetic operations. DNL is calculated for each ADC code (except for the two extreme codes). For the selected code, the contents of the EM register is first initialized to -2^P and then increased by the number of occurrences of the code. In this way, the subtraction in expression (4) is eliminated. The highest absolute value of EM register is taken and divided by H_{ideal}. (If the contents of EM register is negative, its complement is computed.) The procedure of the computation of *DNL* is:

```
initialization: DM=1, DNL=0
while (DM < 2n-1){
  EM = -2^P
  for samples i=1 to N {
    if (ADC = DM) EM++
  }
  if (EM_MSB=1) complement EM
    if (DNL < EM) DNL=EM
    DM++
}
DNL = DNL ≫ P // division performed as shift
```

INL calculation. For better understanding we rewrite expression (5) in the following way

$INL(0) = 0$
$INL(\text{i}) = INL(\text{i-1}) + DNL(\text{i}).$

At the beginning the counter is initialized to 0. After accumulating the number of hits of the current code, H_{ideal} is subtracted from the contents of the EM register. The highest absolute value of EM register is taken and divided by H_{ideal}. The procedure of *INL* computation is:

```
initialization: DM=1, EM=0, INL=0
while (DM < 2n-1){
  for samples i=1 to N {
    if (ADC = DM) EM++
  }
  EM -= 2^P
  if (EM_MSB=1){
    complement EM
    if (INL < EM) INL=EM
    complement EM
  }
  else if (INL < EM) INL=EM
  DM
++
}
INL = INL ≫ P // division performed as shift
```

The sequential BIST structure described above requires low hardware overhead but the test time may become excessive. The approach requires N samples for the calculation of offset, mN samples for the calculation of gain, $(2^n - 2)N$ samples for the calculation of *DNL* and $(2^n - 2)N$ samples for the calculation of *INL*. As an alternative, RAM-based BIST has been developed.

4.2 RAM-based BIST approach

As the name indicates, the RAM-based BIST test structure includes RAM module, in which the ADC code count of a complete histogram is stored. The remaining two modules play a similar role as their counterparts in sequential BIST: the computation module computes the ADC static characteristics from the values stored in RAM, while the control module coordinates the processing and connects the BIST structure to the IEEE Std 1500 test infrastructure.

RAM-based BIST is much faster than sequential BIST approach, only N samples are required for the computation of static parameters of ADC. The samples are first stored in RAM, then the static parameters are computed in accordance with the expressions (2–5). RAM is organized in such way that the ADC code actually presents the RAM address of its code count. In this way, data manipulation is simplified. The computation follows similar

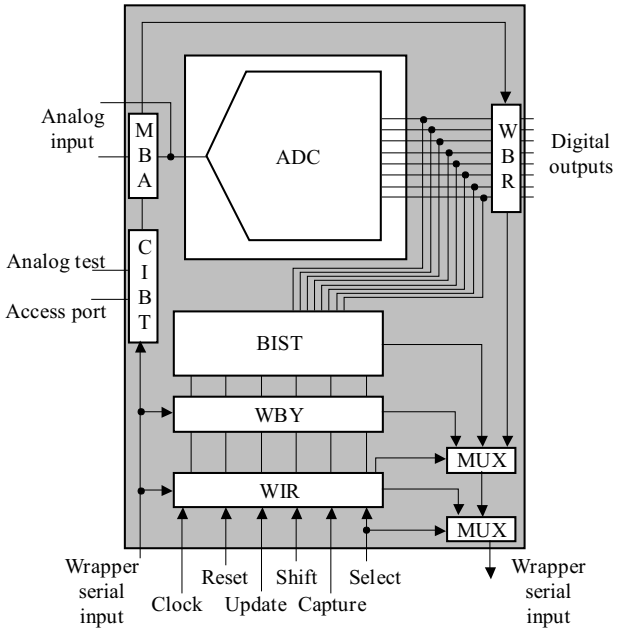

Fig. 5. Histogram based BIST structure in IEEE Std 1500 wrapper

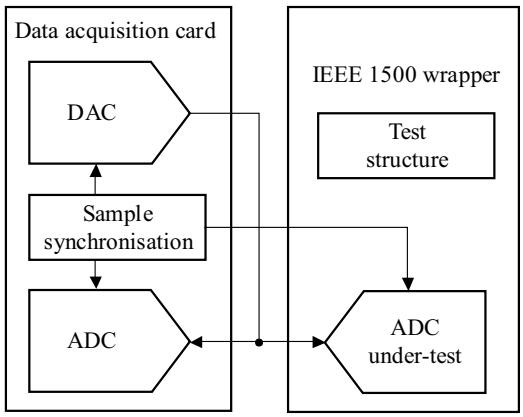

Fig. 6. Test and measurement configuration

principles as before, hence the description in a pseudo-code is omitted.

5 TEST WRAPPER DESIGN

The above test structure was implemented in IEEE Std 1500 test wrapper. The principal block scheme is shown in Fig. 5.

The shaded area presents the test wrapper logic. The lower part comprises Wrapper Serial Port (WSP), Wrapper Instruction Register (WIR) and Wrapper Bypass Register (WBR). Histogram test structure is included and denoted by BIST block. The outputs of ADC are connected to the Wrapper Boundary Register (WBR). On the other hand, ADC input is not included in the wrapper since IEEE Std 1500 is defined only for digital SoC. By analogy with IEEE Std 1149.1/IEEE Std 1149.4 we introduced an analog boundary module at the ADC input. For this purpose, our proprietary test chip [22] was employed. The analog boundary module (ABM) and its test bus interface circuit (TBIC) are added to the wrapper as shown in the figure. Since they are controlled by the 1500 wrapper control signals they could actually be regarded as an analog extension of IEEE Std 1500 infrastructure. In order to assess the impact of MOS switches of ABM on static parameter measurements, direct connection to the ADC input was optionally provided.

6 EXPERIMENTAL RESULTS

An experimental case study was performed with test and measurement configuration depicted in Fig. 6. ADC0808 was chosen as the unit-under-test. Test wrapper was implemented in Spartan3 XC3S200 FPGA. As mentioned above, analog boundary module (ABM) and its test bus interface circuit (TBIC) from our IEEE 1149.4 test chip were added to the wrapper (detail not shown in Fig. 6).

For input stimuli generation we used high resolution DAC from high-speed multifunction data-acquisition card from National Instruments (NI PCI-6251) with 16-bit accuracy The DAC resolution is 16 bit with DNL error ± 1 LSB. Triangle stimuli with amplitude of 3 V and sample rate 12.5 kS/s was generated.

To prevent sample leakage into the adjacent code bins, while constructing the histogram, coherent sampling is required. In order to achieve coherent sampling DAC and ADC-under-test are synchronized. In our case, DAC and ADC-under-test were simultaneously triggered.

Generated input stimulus was monitored by the high resolution ADC of the data acquisition card. The measured SNR of the generated triangle input signal was 62dB. Since the quantization error of an 8-bit ADC is 50 dB, the effect of SNR of the input signal is negligible.

Table 1 presents measured parameters for sequential BIST approach. In order to show the impact of MOS switches, the resulting static parameters obtained with stimulus supplied via ABM or directly to the ADC are presented. Similarly, measured parameters for RAM-based BIST approach are given in Table 2. The parameters are in conformance with the specifications provided by the manufacturer.

Shortened test time is achieved on the account of BIST resources. In order to assess the trade-off between the two approaches we synthesized the wrapper using Cadence RTL Compiler. The resulting designs are summarized in Table 4.

Table 1. Measured parameters for sequential BIST approach

H_{ideal}	Number of samples	Offset error [LSB] via ABM	Offset error [LSB] direct	Gain error [LSB] via ABM	Gain error [LSB] direct	DNL [LSB] via ABM	DNL [LSB] direct	INL [LSB] via ABM	INL [LSB] direct
4	537600	0.50	-0.32	0.70	0.00	0.50	0.50	0.94	0.25
8	1075200	0.25	-0.34	0.34	0.05	0.38	0.38	0.75	0.25
16	2150400	0.50	-0.29	0.52	0.12	0.31	0.31	0.53	0.19
32	4300800	0.78	-0.30	0.30	0.06	0.28	0.25	0.36	0.06
64	8601600	0.45	-0.28	0.22	0.12	0.25	0.23	0.67	0.14
128	17203200	0.71	-0.30	0.24	0.13	0.23	0.22	0.40	0.18
256	34406400	0.43	-0.27	0.22	0.15	0.39	0.21	0.48	0.23
512	68812800	0.22	-0.28	0.05	0.11	0.24	0.11	0.48	0.20

Table 2. Measured parameters for RAM-based BIST approach

H_{ideal}	Number of samples	Offset error [LSB] via ABM	Offset error [LSB] direct	Gain error [LSB] via ABM	Gain error [LSB] direct	DNL [LSB] via ABM	DNL [LSB] direct	INL [LSB] via ABM	INL [LSB] direct
4	1024	0.75	-0.38	0.50	0.05	0.50	0.50	0.58	0.25
8	2048	0.43	-0.44	0.28	0.03	0.38	0.38	0.29	0.23
16	4096	0.40	-0.41	0.34	0.10	0.27	0.19	0.36	0.15
32	8192	0.39	-0.36	0.26	0.13	0.22	0.20	0.57	0.21
64	16384	0.35	-0.38	0.32	0.08	0.23	0.21	0.34	0.15
128	32768	0.40	-0.39	0.29	0.14	0.24	0.15	0.44	0.17
256	65536	0.35	-0.36	0.29	0.11	0.22	0.20	0.52	0.20
512	131072	0.36	-0.35	0.24	0.10	0.23	0.18	0.33	0.19

Table 3. Measurement accuracy and overall test time of sequential and RAM-based BIST

H_{ideal}	Accuracy [LSB]	Test time (s) Sequential BIST	Test time (s) RAM-based BIST
4	0.250	44.0	0.8
8	0.125	87.3	1.0
16	0.063	174.0	1.2
32	0.031	347.3	1.5
64	0.016	694.0	2.4
128	0.008	1387.4	3.6
256	0.004	2774.1	6.1
512	0.002	5547.6	11.3

Table 4. BIST implementation

Sequential BIST	RAM-based BIST	
gates	1277	1199
flip-flops	381	277
RAM cells	–	2048

7 CONCLUSIONS

Presented implementation of histogram based test of ADC core in a IEEE Std 1500 test wrapper achieves the major goal of drastically reducing the amount of data transferred between the embedded ADC core and external test instrumentation. Comparison of test times and hardware overhead of sequential and RAM-based approach provides basis for selection of suitable strategy for BIST implementation of embedded ADC core. This issue has been further elaborated in [23].

In the described case study, triangle-wave generator was not included in the test wrapper because we presume that in most applications in practice the input stimuli will be either supplied by external signal generator or generated by another core (if available) in the SoC-under-test. In both cases, ADC sampling is triggered by the external signal source. The impact of MOS switches connecting the external source to the ADC core was simulated by introducing an ABM module of a IEEE Std 1149.4 compliant test chip. As IEEE Std 1500 covers only digital cores, similar solutions as the one used in our case study can be expected in practice.

Finally, it should be noted that the measured parameters are in good agreement with the values obtained by the conventional technique using laboratory measurement equipment which gives confidence to the described approach.

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