



ISSN 2255-9159 (online) ISSN 2255-9140 (print) 2018, vol. 14, no. 1, pp. 12–22 doi: 10.2478/ecce-2018-0002 https://www.degruyter.com/view/j/ecce

A Novel Hysteresis Power Point Optimizer for Distributed Solar Power Generation

Oleksandr Veligorskyi^{*} (Head of Department, Chernihiv National University of Technology, Chernihiv, Ukraine),
Oleksandr Husev (Associate Professor, Chernihiv National University of Technology, Chernihiv, Ukraine),
Viktor Shevchenko (Ph.D. student, Chernihiv National University of Technology, Chernihiv, Ukraine),
Kostiantyn Tytelmaier (Ph.D. student, Chernihiv National University of Technology, Chernihiv, Ukraine),
Roman Yershov (Senior Lecturer, Chernihiv National University of Technology, Chernihiv, Ukraine),
Roman Kosenko (Ph.D. student, Tallinn University of Technology, Tallinn, Estonia),
Dmitri Vinnikov (Head of the Power Electronics Group, Tallinn University of Technology, Tallinn, Estonia)

Abstract - This paper proposes a new photovoltaic panel maximum-power-point optimizer based on a buck converter. It can be connected to the DC-link distributed energy harvesting system that should perform the true maximum-power-point tracking algorithm based on maintaining a constant DC link voltage. The algorithm is based on the sensorless hysteresis control and ensures high efficiency. Three different realizations of proposed hysteresis optimizers have been analyzed in the paper, including operation principle and adjustment of hysteresis intervals. An experimental study has been performed for a portable low-power photovoltaic system in case of different loads and irradiance levels. The efficiency of maximum power point tracking has been calculated analytically for different hysteresis intervals and validated by experiment, which proved a 97-98 % efficiency of tracking for different PV panel temperatures. The proposed solution is recommended to be used in small- and medium-sized power systems where the price of the conventional maximum power point tracking converter is very high and is comparable to the cost of the individual panel.

Keywords – DC-DC power converters; Maximum power point tracker; Photovoltaic systems; Renewable energy sources.

I. INTRODUCTION

Renewable energy sources are increasingly important in today's conditions due to many practical issues. The European Commission has set up a target to increase the share of renewable energy to 20 % before 2020 [1], [2]. What is more, Denmark will have reached a 70 % share of energy production from renewable sources by 2020 and 100 % by 2050. The topic of power electronic converters for renewable applications is becoming extremely popular nowadays.

Despite the fact that the cost of renewable energy is decreasing, it is still higher than that of energy obtained from conventional sources. As a result, the main direction of the research is focused on the decreasing of the price. Considering wind turbine energy or photovoltaic (PV) energy, the power electronic interface converter is one of the key components whose price has to be optimized. As for the PV panel, the output power level depends on the output voltage. A maximum efficiency is achieved when the PV panel operates at a voltage that corresponds to the maximum power point (MPP). The MPP, in its turn, depends on the PV panel design, the irradiance level and the panel temperature. That is why it is so important to use power converters that ensure the functioning of the PV panel at the MPP or near it [1]–[6].

The disadvantage of such devices is the need for sensing the voltage and current of the PV panel and specialized integrated circuits (ICs) or microcontrollers to perform the complex control task, which significantly increases the cost [7]–[9].

There are many types of distributed PV generation systems, which can be classified by panel interconnection, presence of individual power converters (micro-converters; strings or central inverters) and the type of current flowing inside the system. In case of low power DC-DC application, the basic topologies with DC current interconnection are shown in Fig. 1. The simplest distributed system (Fig. 1a) consists of a buck, boost or buck-boost DC-DC converter and a single PV module.



Fig. 1. The main possible configurations of a DC-DC PV system.

In case of string configuration there are two possible basic solutions. The first one is based on the direct connection of the string PV module to the single DC-DC converter [10]–[15] (Fig. 1b). Strings of PV panels have a significantly reduced power output when an impedance mismatch between the panels occurs, as e.g. caused by partial shading by a cloud. In order to increase the efficiency of such a system, intermediate DC-DC converters can be used. This configuration is demonstrated in

* Corresponding author.

E-mail: oleksandr.veligorsky@inel.stu.cn.ua

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Fig. 1c [16]. With regard to DC-AC applications, the best efficiency will be exhibited by a system that has an optimizing DC-DC converter for each phase [17].

In case of using an intermediate DC-DC converter, depending on the ratio of V_{PV} to V_{DC} , conventional boost, forward or fly-back topologies are used [18]. The third group consists of the most accomplished power stage solutions, where flexibility is achieved by increasing the number of reactive components with SEPIC or Cuk topologies (which physically restrict their efficiency) [19] or by increasing the number of semiconductor switches with the switching-inductor and switching-capacitor topologies or the buck-boost topology.

When a high boost or buck ratio (more than 4) or extra-low voltage and current output ripples are reached simultaneously with unnecessary galvanic isolation, the good solution is to use the principle of coupled inductors, which is described in detail and implemented in [20], [21] and [22].

At the same time, the solution with DC-DC converters for each panel is the most expensive one because of using a control system along with voltage and current sensors for each converter.

An approved set of MPPT algorithms is described in [23] and [24]. Most of them are based on the flow consisting of continuous *V* and *I* measurements from resistive sensors and an iterative procedure of MPP calculation (sometimes the model of a certain PV cell is used) which results in tuning of the PWM duty cycle of the converter switches [25]–[27]. Advanced control methods are used for self-measuring, prediction and adaptation paradigms and require more complex calculations [26], [28], which are performed by using MCU [27], DSP or FPGA [29]. The newest methods with a wide control and adaptation range are based on AI concepts of neural networks and fuzzy logic and are described in [30]–[33]. It should be noted that regardless of the type of algorithms most of them need two or three voltage and current sensors.

There are several ways of cost reduction: a sensorless control approach (without a current sensor) [34], extreme power saving by simplification and reduction of the control part [35] by using a composition of existing hybrid control ICs. Such solutions allow the tracking optimization of a single PV cell with output power and operation voltage less than 1 W and 2 V. Also, both the sensor count and the calculation complexity can be reduced by using a sensorless hysteresis control methodology with a boost converter [29]. The main drawback of the proposed idea lies in continued switching of the transistor in a wide operation range. The objective of this paper is further improvement of the idea based on the buck topology.

II. PROPOSED OPTIMIZER STRUCTURE AND OPERATION PRINCIPLE

The main idea of a hysteresis power optimizer is to provide transmission of electrical energy to the load by portions during the time intervals when the voltage on the input capacitor is close to the maximum-power-point voltage of a solar cell. This ensures the operation of a solar cell close to its MPP, which guarantees it a high efficiency.

A basic functional diagram of the optimizer is shown in Fig. 2a. It consists of an input buffer capacitor ($C_{\rm IN}$), a

hysteresis element (HY), a transistor (Q), a freewheeling diode (D₁) and a low-pass filter (L_F-C_F). Three proposed realizations of the hysteresis element are shown in Figs. 2b–2d and are described in detail in Chapter III of the paper. A low threshold voltage level (V_{TL}) and a high threshold voltage level (V_{TH}) are selected according to the desired hysteresis bandwidth and the position relative to the PV panel's P = f(V) characteristic and MPP power, voltage and current (P_{MPP} , V_{MPP} and I_{MPP} , respectively).

For example, Fig. 3 shows the optimizer operation in a hysteresis band with the power derived from the panel less than $0.9P_{\text{MPPT}}$. In this case, the threshold level of output power is equal to $0.9P_{\text{MPPT}}$. By using *P*-*V* and *I*-*V* characteristic values of V_{TH} , V_{TL} can be found, the high and low threshold currents (I_{TH} , I_{TL}) of the PV can be found as well. If the load is constant optimizer can operate in three different modes depending on the relationship between the parameters of the load and the panel (Fig. 3): out-of-range, direct and hysteresis.

The *out-of-range mode (OR-mode)* is possible when the load current (optimizer output current) meets the condition $I_{\text{LOAD}} < I_{\text{TL}}$ (the load is high-resistance). In such case, the input buffer capacitor C_{IN} is never discharged to V_{TL} , so Q is never switched off and the PV panel works near its open-circuit mode (OC) with a low efficiency (Fig. 3a). This is a common drawback of buck-only MPPT converters [16].

The *direct mode (DIR-mode)* is possible when the load current meets the condition $I_{TL} < I_{LOAD} < I_{TH}$, the input buffer capacitor (C_{IN}) is never discharged to V_{TL} (as the PV panel current is equal to the load current and does not exceed the hysteresis band limits), so Q is never switched off and the PV panel is directly connected to the load (Fig. 3b). In this mode, the system efficiency is the highest due to the absence of switching loses and the panel's operation is close to the MPP. The proposed optimizer in the direct and out-of-range modes is not tracking the MPP, and the operation (output voltage and current) depends on the load.

The main mode of the proposed optimizer, which provides a high efficiency of MPP tracking, is the *hysteresis mode (HYS-mode)*.

In case of a low-resistance load, when the load current meets the condition $I_{\text{LOAD}} > I_{\text{TH}}$, the optimizer operates as a buck DC-DC converter with the control function determined by the hysteresis band, the PV panel and the load parameters (Fig. 3c). The circuit's operation in this mode is shown in detail in Fig. 4a.



Fig. 2. Proposed optimizer functional diagram (a), different realization of hysteresis element HY (b)–(d).



Fig. 3. Optimizer operation modes: out-of-range mode (OR-mode) (a), direct mode (DIR-mode) (b), hysteresis mode (HYS-mode) (c).



Fig. 4. Optimizer time diagram: variant A Fig. 2a (a), variant B Fig. 2b and variant C Fig. 2c (b).

The circuit's operation in the switching mode can be divided into the following stages:

- t_0 the input voltage of HY rises above V_{TH} , HY toggles and transistor Q starts conducting;
- t₀-t₁ the energy is transferred to the load (C_{IN} is discharging through the load);
- t_1 the input voltage of HY falls below V_{TL} , HY toggles, transistor Q is not conducting;
- $t_1-t_2 C_{IN}$ is charging from the panel;
- t_2-t_3 the process repeats.

The above is correct at the condition that $I_{OUT} > I_{SC} (I_{SC} - \text{the} open-circuit current of the PV panel) so C_{IN} does not charge while Q is open. If <math>I_{OUT} < I_{SC}$ then Q is always open, so the output current and voltage are determined only by the load parameters.

The output voltage of the optimizer has the form of high-frequency pulses (Q is open only for the time period T_{on}) and must hence be filtered by a low-pass filter.

III. CONTROL SYSTEM DESCRIPTION

Different hysteresis techniques can be realized as a control circuit HY in the proposed optimizer (Fig. 2 b–d). Some examples of control, limitations, advantages and drawbacks are described below.

A. Proposed Optimizer Circuit Variant A

A power optimizer circuit diagram (shown in Fig. 2b) is the simplest way to perform hysteresis control.

New elements R₁, R₂, C₁ perform a function of a proportional-integral chain that limits the switching frequency and determines the hysteresis band. The R₁, R₂ division factor (transfer ratio) is selected so that when $V_{IN} = V_{TH}$ then $V_1 = V_{GSth}$, where V_{GSth} is the gate-source threshold voltage of MOSFET Q. To provide a proper switching frequency, the time constant of the gate circuit should be lower compared with that of the input charge circuit. This is possible when the capacitance of C₁ meets the condition $C_{IN} \gg C_1$.

The circuit operates as follows. Initially, C_{IN} and C_1 are discharged, and MOSFET Q is not conducting. The process of charging of C_{IN} and C_1 starts after the surface of the PV panel is irradiated. When the voltage on C_{IN} reaches V_{TH} , voltage V_1 reaches V_{GSth} (the gate-to-source threshold voltage of transistor Q). It means that Q opens; the process of energy transfer from C_{IN} to the load is accompanied by the discharge of C_{IN} and C_1 . When C_1 discharges below V_{GSth} , MOSFET Q stops conducting and the process repeats.

The advantages of such a hysteresis circuit should be underlined. First of all, the circuit includes a number of passive elements and only one active (Q) element and can operate in the DIR-mode without switching losses (Fig. 3b) in case of a certain load that allows obtaining a high efficiency. The proposed circuit has no current sensors; and the hysteresis band position could be easily adjusted by tuning resistors' R_1 and R_2 values.

At the same time, some drawbacks of the proposed hysteresis circuit should be noted:

- only the hysteresis band position can be tuned in this circuit, whereas the width of the hysteresis band is fully determined by the transistor's parameters and cannot be changed;
- the hysteresis band width is mainly below 1 V and will vary noticeably from one transistor to another even in the same batch.
- in case of a certain load $(I_{\text{LOAD}} < I_{\text{TL}})$ the circuit operates in the OR-mode with low PV panel performance (Fig. 3a).

B. Proposed Optimizer Circuit Variant B

A modified hysteresis element HY circuit diagram of the proposed power optimizer is shown in Fig. 2c. Such a version is a modification of the above-described circuit, shown in Fig. 2b. The main change consists in the two additional diodes D_F and D_R that provide an adjustable hysteresis band width.

For the sake of simplicity, several assumptions have been made: the forward voltage drop V_{DF} of diode D_F satisfies the condition $V_{\text{DF}} < (V_{\text{TH}} - V_{\text{DR}})$. If this condition is not satisfied, the circuit operates in the same way except that D_F is open and C₁ starts charging somewhere in the interval t_0-t_1 ; C₁ is relatively low so C₁ it charges almost instantly; gate resistance R_{QG} is infinite; $I_{\text{OUT}} > I_{\text{IN}}$, so C_{IN} does not charge while Q is open.

The circuit's operation (Fig. 4b) can be divided into the following stages:

- $t_0-t_1 D_F$ is conducting, D_R and Q not, C_1 is charging;
- t₁ C₁ is charged to V_{GSth} + V_{DF}, C_{IN} is charged to V_{TH}, Q is conducting;
- t₁-t₂ D_F has a reverse bias, C_{IN} is discharging through the load, C₁ keeps transistor Q in the conducting mode;
- t_2 voltage V_1 falls below $V_{\text{GSth}} V_{\text{DR}}$, C_{IN} is charged to V_{TH} , D_{R} is conducting, C_1 discharges through R_2 to a voltage lower than V_{TH} , Q is closing, C_{IN} begins charging from the solar panel and then the process repeats.

The main advantage of the proposed solution lies in that the width of the hysteresis band can be easily adjusted by selecting appropriate "forward" and "reverse" diodes (D_F and D_R), or by

series connection of several diodes. At the same time, the hysteresis band width is still hard to precise and independently tunes in both directions, because of only one voltage divider being used and because of the limited diversity of diodes the forward voltage drops. Also, the circuit can operate in the OR-mode with a low PV panel performance at a certain load (Fig. 3a).

To determine the circuit parameters, firstly, we need to write down expressions for the C₁ voltages for two states of the optimizer: "switched on" ($V_{IN} = V_{TH}$) and "switched off" ($V_{IN} = V_{TL}$). To switch on Q when $V_{IN} > V_{TH}$, the following expression must be valid:

$$\varphi_1 = V_{\rm IN} \frac{R_2}{R_1 + R_2} \ge V_{\rm TH} \frac{R_2}{R_1 + R_2} = (V_{\rm GSth} + V_{\rm DF}).$$
(1)

Transistor Q will switch off when $V_{IN} < V_{TL}$:

$$\varphi_1 = V_{\text{IN}} \frac{R_2}{R_1 + R_2} \ge V_{\text{TL}} \frac{R_2}{R_1 + R_2} = (V_{\text{GSth}} - V_{\text{DR}}).$$
 (2)

The voltage divider ratio must be set in such a way that when the circuit is supplied by V_{MPP} , the voltage over R_2 is equal to transistor threshold voltage V_{GSth} :

$$\frac{R_2}{R_1 + R_2} = \frac{V_{\text{GSth}}}{V_{\text{MPP}}}.$$
(3)

Expressing V_{DF} and V_{DR} from (1)–(3), we obtain the following equations:

$$V_{\rm DF} = V_{\rm TH} \frac{V_{\rm GSth}}{V_{\rm MPP}} - V_{\rm GSth}; V_{\rm DR} = V_{\rm GSth} - V_{\rm TL} \frac{V_{\rm GSth}}{V_{\rm MPP}}.$$
 (4)

For example, let us calculate the voltage drop over the diodes for the following typical case: $V_{\text{GSth}} = 3 \text{ V}$, $V_{\text{TH}} = 41 \text{ V}$, $V_{\text{MPP}} = 39 \text{ V}$, $V_{\text{TL}} = 34 \text{ V}$; by using (3) $V_{\text{GSth}} / V_{\text{MPP}} = 3 / 39 = 0.077$, and finally by using (4) $V_{\text{DF}} = 0.23 \text{ V}$ and $V_{\text{DR}} = 0.61 \text{ V}$. As can be seen, V_{DF} is a typical voltage drop of a Schottky barrier diode while V_{DR} is typical for a Si rectifier diodes.

C. Proposed Optimizer Circuit Variant C

Among the drawbacks of the previous schematic is the limited tuning capability because of the limited diversity of diodes' forward voltage drop and the tight bond between V_{TH} and V_{TL} because of the use of only one voltage divider. The schematic shown in Fig. 2d solves this problem by utilizing the second voltage divider R₃, R₄. The use of two dividers provides the ability to tune V_{TH} and V_{TL} independently in a wide range. It should be noted that the proposed variant C optimizer as well as other circuits can also operate in the OR-mode with low PV panel performance at a certain load (Fig. 3a) and this is a common drawback of the proposed hysteresis power optimizer.

The math expressions for the variant C circuit diagram are almost the same as for circuit B:

$$V_{\text{TH}} \frac{R_2}{R_1 + R_2} = (V_{\text{GSth}} + V_{\text{DF}});$$
 (5)

$$V_{\rm TL} \frac{\bar{R}_4}{R_2 + R_4} = (V_{\rm GSth} - V_{\rm DR}).$$
(6)

Since this circuit diagram has two independent voltage dividers, threshold voltages V_{TH} and V_{TL} can be easily adjusted by varying the dividers' ratio without finding diodes with the exact voltage drop (it is recommended to use two identical low-drop Schottky rectifier diodes to ease calculations and minimize the power losses).

IV. ESTIMATION OF OPTIMAL HYSTERESIS WINDOW AND THE PROPOSED OPTIMIZER

As has already been mentioned, the panel MPP depends on the irradiance level and the temperature, so a hysteresis window calculated for certain conditions may be ineffective at others. It means that the full range of PV module irradiance and temperatures should be taken into account for the calculation of a hysteresis window.

The recommended methodology for choosing the optimal hysteresis window is shown in the example below. The following results are obtained in the mathematical modelling software for the portable low-power PV system, including series connection of 12 semi-flexible Si PV modules with the following characteristics (for one PV module): $P_{\text{MAX}} = 1$ W, $V_{\text{MPP}} = 1.5$ V, $I_{\text{MPP}} = 0.66$ A, $I_{\text{SC}} = 0.85$ A, $V_{\text{OC}} = 2.0$ V.

To estimate the optimizer efficiency, a simplified mathematical model has been built (Fig. 6a). The calculations have been performed for the following circuit elements: $C_{\rm IN} = 1 \cdot 10^{-3}$ F, $R_{\rm L} = 16 \Omega$, $R_{\rm IN} = 28.23 \Omega$, $R_{\rm Qon} = 0 \Omega$; $R_{\rm Qoff} = \infty$, PV panel parameters as stated above.

To simplify the input current calculation, the following assumptions have been used: the simplified model does not include a low-pass filter as its impact on the input voltage and current is negligible; a load resistance is constant; during a half-period of the optimizer's operation, the PV panel is represented by a constant voltage source E_{PV} ($E_{PV} = V_{TL}$ while Q is conducting and $E_{PV} = V_{TH}$ while Q is not conducting); $R_{IN} = V_{OC} / I_{SC}$ and represents a current limiter for the PV panel.

With all those assumptions, the circuit operation is divided into two periods: the first one in the case if Q is not conducting (the circuit is represented by Fig. 6b), the second one - if Q is conducting (Fig. 6c).

The circuit equation for the closed Q is shown below:

$$R_{\rm IN}C_{\rm IN}\frac{{\rm d}V_{\rm CIN}^{(1)}}{{\rm d}t} + V_{\rm CIN}^{(1)} = V_{\rm TH}.$$
(7)

Taking into account initial condition $V_{\text{CIN}}(0) = V_{\text{TL}}$, the voltage on V_{CIN} changes as follows:

$$V_{\rm CIN}^{(1)} = V_{\rm TH} + (V_{\rm TL} - V_{\rm TH}) e^{-\frac{t}{R_{\rm IN}C_{\rm IN}}}.$$
(8)

Voltage $V_{\text{CIN}}^{(1)}$ is the voltage on the PV panel, so the equation of the classic equivalent circuit of the PV module [8] can be used to find current I_{IN} :

$$I_{\rm IN}^{(1)} = I_{\rm SC} - I_0 \left(e^{\frac{V_{\rm TH} + (V_{\rm TL} - V_{\rm TH})e^{-\frac{t}{R_{\rm IN}C_{\rm IN}}}}{\varphi T}} - 1 \right).$$
(9)

The second equivalent circuit starts when $V_{\text{CIN}} = V_{\text{TH}}$ and can be described by the following equation:

$$R_{\rm IN}C_{\rm IN}\frac{dV_{\rm CIN}^{(2)}}{dt} + \left(1 + \frac{R_1}{R_{\rm H}}\right)V_{\rm CIN}^{(2)} = V_{\rm TL}.$$
 (10)

Solving equation (10) in accordance with the initial conditions mentioned above and by using the equivalent circuit of the PV, the following expressions have been obtained:

$$V_{\rm CIN}^{(2)} = \frac{R_{\rm L}V_{\rm TH}}{R_{\rm L} + R_{\rm IN}} + \left(V_{\rm TH} - \frac{R_{\rm L}V_{\rm TL}}{R_{\rm L} + R_{\rm IN}}\right) e^{-\frac{(R_{\rm L} + R_{\rm IN})}{R_{\rm IN}R_{\rm L}C_{\rm IN}}t}.$$
 (11)

$$I_{\rm IN}^{(2)} = I_{\rm SC} - I_0 \left(e^{\frac{R_{\rm L}V_{\rm TH}}{R_{\rm L} + R_{\rm IN}} + \left(V_{\rm TH} - \frac{R_{\rm L}V_{\rm TL}}{R_{\rm L} + R_{\rm IN}}\right)e^{-\frac{\left(R_{\rm L} + R_{\rm IN}\right)}{R_{\rm IN}R_{\rm L}c_{\rm IN}}t}}{\phi^T} - 1 \right).$$

The average output power harvested from the panel during one period of a steady process is calculated as follows:

$$P_{\rm avg} = \frac{\int_0^{T_1} V_{\rm CIN}^{(1)} I_{\rm IN}^{(1)} dt + \int_0^{T_2} V_{\rm CIN}^{(2)} I_{\rm IN}^{(2)} dt}{T},$$
(12)

where T is the period of a steady process (Fig. 4b).



Fig. 5. MPP trajectory for changing the irradiance and temperature of the PV module.



Fig. 6. Optimizer equivalent circuits at different transient intervals for analytical calculations: (a) generalized circuit; (b) transistor Q is closed; (c) transistor Q is open.

The steady process of period T is calculated approximately based on the equivalent circuit time constants for the on transistor (Fig. 6b) and the off transistor (Fig. 6c):

$$T = 3(\tau_{(1)} + \tau_{(2)}) = 3\left(R_{\rm IN}C_{\rm IN} + \frac{R_{\rm IN}C_{\rm IN}R_{\rm L}}{R_{\rm IN}+R_{\rm L}}\right).$$
 (13)

As a result, the expression for the average output power during the period of operation as a function of PV parameters – load resistance, panel temperature, illumination and threshold voltages V_{TH} and V_{TL} – has been obtained. Such parameters as *T*, *S*, *R*_L, *V*_{OC}, *I*_{SC}, *C*_{IN} are used as constants, whereas *V*_{TL} and *V*_{TH} – as variables, so the final expression of the average power harvested from the PV modules is a function of two variables: $P_{\text{avg}} = f(V_{\text{TL}}, V_{\text{TH}})$. The resulting expression is beyond the scope of this paper and too complex to be shown here.

The maximum power P_{MPP} and the corresponding voltage V_{MPP} of the analysed PV system (12 series-connected PV modules) can be found analytically by using the equation of the classic equivalent circuit of a PV module. For the above V_{OC} , I_{SC} , $S = 1000 \text{ W/m}^2$, the calculated values are shown in Table I. MPP $P_{\text{MPP}} = 15.1 \text{ W}$ for T = 25 °C is close to $P_{\text{MAX}} = 15 \text{ W}$, mentioned in the documentation for the modules used.

The efficiency *Eff* of the proposed optimizer can be found for different temperatures by using (12):

$$Eff = \frac{P_{\text{avg}}(V_{\text{TL}}; V_{\text{TH}})}{P_{\text{MPP}}}.$$
 (14)

It is clear that the efficiency of the proposed power optimizer depends on the threshold voltages V_{TL} and V_{TH} . For proper operation the optimizer's $V_{TL} < V_{MPP}$ and $V_{TH} > V_{MPP}$ and they should be close to the maximum power point. Let the hysteresis interval be $\Delta V = V_{TH} - V_{TL} = \Delta V^+ + \Delta V^-$, $\Delta V^+ = V_{TH} - V_{mdl}$, $\Delta V^- = V_{mdl} - V_{TL}$, where V_{mdl} is the "middle" of the hysteresis interval (it should be noted that this "middle" is not a mean or average voltage for the ΔV interval). $V_{mdl} = [19.5; 19.0; 18.5;$ 18.0; 17.5] V has been used to calculate the efficiency.

Two types of hysteresis intervals have been analysed. The first case considered in the paper, the so-called "symmetrical" one, corresponds to $\Delta V^+ = \Delta V^-$. The second case – the "unsymmetrical" one – is based on an unsymmetrical shape of the *P-V* curve for a PV module. It is well known that the right-side slope of the *P-V* curve is always more steep compared with the left-side one. In our case, the voltage difference for points P = 0 W and $P = P_{\text{MPP}}$ for the left-side slope is equal to $V_{\text{MPP}} = 19.5$ V, whereas for the right-side slope $V_{\text{OC}} - V_{\text{MPP}} = 24.0$ V – 19.5 V = 4.5 V. So, we can set ΔV^+ and ΔV^- in accordance with the ratio 4.5 : 1.0.

The results of efficiency calculation for different temperatures and symmetrical/unsymmetrical hysteresis intervals obtained from (14) are shown in Fig. 7. Curve 1 corresponds to $V_{mdl} = V_{MPP} = 19.5$ V, whereas curves 2, 3, 4 and 5 – to $V_{mdl} = 19.0$ V, 18.5 V, 18.0 V and 17.5 V, respectively.

TABLE I MAXIMUM POWER POINT PV SYSTEM FOR $S = 1000 \text{ W/m}^2$

<i>T</i> , °C	$V_{\rm OC}, { m V}$	$P_{\rm MPP}, { m W}$	$V_{\rm MPP},{ m V}$
0	26.4	17.3	21.9
25	24.0	15.1	19.5
50	21.6	13.0	17.1

An analysis of the data from Fig. 7a shows that an efficiency of more than 0.95 is provided for a wide range of ΔV of the hysteresis band in the case if T = 25 °C for the symmetrical hysteresis intervals as well as for the unsymmetrical ones. It should be noted that the efficiency for the "symmetrical" case is lower as compared to the "unsymmetrical" hysteresis because the power drop after the MPP is significantly higher. So, for example, $V_{mdl} = 19.5$ V (curve 1) and $\Delta V > 5$ V leads to a fast decrease of the efficiency down to 0.7 because V_{TH} in this case is close to V_{OC} , where P = 0 W.

The temperature variation leads to significant shifting of the maximum power point, as shown in Fig. 5, so the efficiency of the proposed optimizer is lower compared with the optimizer tuned to $V_{\text{MPP}} = 19.5$ V and T = 25 °C.

The analysis of the data allows choosing the interval and the "middle" position of the hysteresis, providing the best efficiency for different temperatures. An efficiency higher than 0.9 is possible for the "unsymmetrical interval" with $\Delta V = 2$ V and $V_{mdl} = 19.0$ V ($V_{TH} = 17.25$ V, $V_{TL} = 19.25$ V), marked as "optimal" in Fig. 7.

V. EXPERIMENTAL STUDY

A. Experimental Setup Description

The experimental setup of the three proposed power optimizers has been created to prove their ability of tracking MPP at different levels of solar irradiance and temperatures. The list of equipment for the experimental setup is shown in Table II. It should be noted that a PV simulator has been used instead of real PV modules to ensure repeatability of data for various experiments.

The developed prototype can implement all of the three above-considered power optimizers by using jumpers and potentiometers, adjusting the boundary positions of hysteresis V_{TL} and V_{TH} . The component list for the buck converter, which acts as a power converter for the proposed optimizer, is described in Table III.

TABLE II Equipment List for Test Setup

No.	Type	Name of the equipment
1	Oscilloscope	Tektronix MDO4034B-3
2	Power analyzer	Tektronix PA1000
3	Thermal camera	Fluke Til10
4	PV-simulator	Keysight E4360A

 TABLE III

 COMPONENT LIST FOR EXPERIMENTAL OPTIMIZER

Pos.	Туре	Name and parameters of the component
Q	MOSFET	IR IRL3803 ($V_{\rm DS} = 30$ V, $R_{\rm DS(on)} = 6.0 \text{ m}\Omega$, $I_{\rm D} = 140$ A)
\mathbf{D}_1	Diode	ON Semiconductor SS24 ($I_F = 2 \text{ A}$, $V_{RRM} = 40 \text{ V}$, $V_{F@2A} = 0.5 \text{ V}$)
L _F	Inductor	68 μH ($R_{\rm DC}$ = 0.3 Ω)
C _{IN}	Input filter capacitor	68 μF
C _F	Output filter capacitor	470 μF



Fig. 7. Efficiency of the optimizer for different V_{mdl} : 1 – 19.5 V, 2 – 19.0 V, 3 – 18.5 V, 4 – 18.0 V, 5 – 17.5 V: T = 0 °C (a), T = 25 °C (b), T = 50 °C (c).

Instead of the passive hysteresis circuit based on diodes (Fig. 2b–d), hysteresis control element HY has been built on discrete logic elements, such as J-K Type Flip-Flop CD4027, Schmitt trigger MC14584 and functional gate (inverter) MC14572. Driver TC4427A has been used for switching MOSFET transistor Q.

The experimental prototype of the power optimizer is shown in Fig. 8a. The printed circuit board consists of two parts: the hysteresis control and buck DC-DC converter and two connectors (the input for the connection of PV modules and the output for the load, marked with arrows).

B. Experimental Verification of the Proposed Optimizer

The efficiency of the proposed power optimizer has been analysed for different loads and irradiance level $S = 1000 \text{ W/m}^2$ and temperatures T = 25 °C, 35 °C and 50 °C by using a PV simulator as an energy source. V_{OC} and I_{SC} have been set on the PV simulator in accordance with the technical data for the PV modules used (see Chapter IV). A thermal photograph for $R_L = 5 \Omega$ and $P_{IN} = 11.76 \text{ W}$ is shown in Fig. 8b. As can be clearly seen, the main source of losses is concentrated in diode D_1 . Optimizing the design of that component can diminish the total losses and improve the efficiency of the proposed power optimizer.

The efficiency of MPP tracking plots for the proposed optimizer under the conditions $V_{mdl} = 18.5 \text{ V}$, $V_{TL} = 16.5 \text{ V}$, $V_{TH} = 18.7 \text{ V}$, $S = 1000 \text{ W/m}^2$, changing active load in the range 4 Ω to 15 Ω , for cases T = 25 °C, 35 °C and 50 °C (curves 1, 2,

3, respectively) is depicted in Fig. 8c. Points 4 and 5 show MPP tracking efficiency, calculated analytically in Chapter IV for the same parameters V_{mdl} , V_{TL} and V_{TH} (point 4 corresponds to T = 25 °C whereas point 5 – to T = 50 °C). A comparison of the position of points 4 and 5 with plots 1 and 3 proves the proposed tracking principle.

Obviously, the proposed analytical model of the power optimizer, considered in Chapter IV, corresponds to the experimentally verified data: the power optimizer tuned to T = 25 °C is more efficient compared with T = 50 °C operation. It should be noted that the proposed analytical model of the power optimizer considers only MPP tracking and does not take into account losses in the buck power converter elements (MOSFET, diode, inductor, etc.). The efficiency of the buck converter is shown in Fig. 8c, curves 6–8. As can be seen, the efficiency of the power converter is higher for a higher load resistance.

This can be explained by that fact that the higher-loadresistance power optimizer operates in the direct mode, without MOSFET switching, so the main source of losses consists in conductance losses. A lower efficiency in the case of the lowresistance load is explained by a higher deviation of current $I_{\rm IN}$ (see Fig. 8d) and operation in hysteresis mode, where losses consist of conductance and dynamic parts (caused by on-/off-MOSFET losses, inductor losses etc.). The second reason why the experimental data show a small difference from the analytically-calculated ones is the following.



Fig. 8. Experimental prototype of power optimizer (a), thermal image for $S = 1000 \text{ W/m}^2$, $R_L = 5 \Omega$, T = 25 °C (b), efficiency plots for $V_{mdl} = 18.5 \text{ V}$, $V_{TL} = 16.5 \text{ V}$, $V_{TH} = 18.7 \text{ V}$, where 1-3 – experimental efficiency of MPP tracking, 4-5 – calculations of MPP tracking, 6-8 – experimental efficiency of buck converter for cases: 1, 4, 6 - T = 25 °C, 2, 7 - T = 35 °C, 3, 5, 8 - T = 50 °C (c), experimental time diagram for $R_L = 5 \Omega$ and $R_L = 26 \Omega$ (d).

The analytical model of the PV modules considered in Chapter IV is simplified, thus, the position of MPP for the analytical solution and the experimental verification can be different, so it also leads to a difference in the data but does not violate the calculations and the circuit operation for the proposed power optimizer.

Time diagrams of the operation of the experimental prototype of the power optimizer for two load resistances are shown in Fig. 8d. It is obvious that in case of lower R_L the circuit operates in the hysteresis mode (depicted in Fig. 3c); a signal on the MOSFET gate pin switches on and off the buck DC-DC convertor. Higher load ($R_L = 26 \Omega$) transfers the circuit to the direct mode (depicted in Fig. 3b), when the MOSFET is almost constantly open and energy flows to the output without modulation in the converter. In case of the load resistance increasing further, the circuit operates in the out-of-range mode (Fig. 3a), which is not shown on the experimental time diagrams. In this case the MOSFET is conducting all the time as well.

VI. CONCLUSION

A new PV panel optimizer MPPT algorithm has been proposed. The proposed circuit diagram is a very robust and cheap solution, yet capable of maintaining PV panel operation close to MPP.

The proposed optimizer can be connected to the DC-link distributed energy harvesting system, which should perform a true MPPT algorithm based on maintaining constant DC-link voltage.

The proposed optimizer can be used with a partially shaded PV-cell string. To increase the general efficiency, the optimizer may be used for a low-cell-count string, a parallel cell assembly or as a cell-level optimizer. A cell-level MPPT is almost never used in real-world applications because of the complexity and cost of converters, yet with the proposed optimizer it is possible, as it consists only of a few elements and all of them can be integrated into the PV cell without sensors and without a control system.

The proposed solution is recommended to be used in smalland medium-sized power systems, where the price of a conventional MPPT converter is high and comparable to the cost of the individual PV panel.

ACKNOWLEDGEMENT

The current study was supported by the Ministry of Education and Science of Ukraine (projects 0116U004695 and 0116U006960). The Estonian partner's research work was supported by the Estonian Centre of Excellence in Zero Energy and Resource Efficient Smart Buildings and Districts, ZEBE, grant 2014-2020.4.01.15-0016 funded by the European Regional Development Fund.

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Oleksandr Veligorskyi received the B. sc. and M. sc. degrees in electronic systems from Chernihiv State University of Technology, Chernihiv, Ukraine, in 2001 and 2002, respectively. He received his doctoral degree in semiconductor power converters from the National Academy of Sciences, Institute of Electrodynamics, Kiev, Ukraine, in 2007.

He is currently Head of the Biomedical Radioelectronic Apparatus and Systems Department, Chernihiv National University of Technology. He has authored more than 30 published papers on power converters and is the

holder of several utility models. His research interests include semiconductor power converters, photovoltaics, biomedical electronics, industrial automation and control.

Address: Chernihiv National University of Technology, Biomedical Radioelectronic Apparatus and Systems Department. Shevchenko Str. 95, 14035, Chernihiv, Ukraine.

E-mail: oleksandr.veligorsky@inel.stu.cn.ua

ORCID iD: https://orcid.org/0000-0002-8256-7339



Oleksandr Husev (S'10–M'12) received the B. sc. and M. sc. degrees in industrial electronics from Chernihiv State Technological University, Chernihiv, Ukraine, in 2007 and 2008, respectively. He defended his Ph. D. thesis at the Institute of Electrodynamics of the National Academy of Science of Ukraine in 2012.

He is a Senior Researcher of the Department of Electrical Engineering, Tallinn University of Technology, and an Associate Professor at the Department of Biomedical Radioelectronics Apparatus and Systems, Chernihiv National University of Technology. He has over 100

publications and is the holder of several patents. His research interests include power electronics systems, design of novel topologies, control systems based on a wide range of algorithms, including modelling, design, and simulation; applied design of power converters and control systems and application, stability investigation.

Address: Chernihiv National University of Technology, Biomedical Radioelectronic Apparatus and Systems Department. Shevchenko Str. 95, 14035, Chernihiv, Ukraine.

E-mail: oleksandr.husev@ieee.org

ORCID iD: https://orcid.org/0000-0001-7810-457X



Viktor Shevchenko received the B. sc. and M. sc. degrees in industrial electronics from Chernihiv National University of Technology, Chernihiv, Ukraine, in 2015 and 2017, respectively. He is a Ph. D. student since 2017. He is a Junior Researcher and a teacher's assistant at the Department of Biomedical Radioelectronics Apparatus and Systems of Chernihiv National University of Technology. He has co-authored several publications and has obtained several patents. His area of research interests includes power electronics systems, wireless power transfer, photovoltaic systems.

Address: Chernihiv National University of Technology, Biomedical Radioelectronic Apparatus and Systems Department. Shevchenko Str. 95, 14035, Chernihiv, Ukraine.

E-mail: shevaip1990@gmail.com ORCID iD: https://orcid.org/0000-0002-9457-7454



Kostiantyn Tytelmaier received the B. sc. and M. sc. degrees in industrial electronics from Chernihiv National Technological University, Chernihiv, Ukraine, in 2012 and 2014, respectively.

He is employed as an assistant teacher at the Department of Biomedical Radioelectronics Apparatus and Systems, Chernihiv National University of Technology, Chernihiv, Ukraine. He has co-authored more than ten papers and a book chapter on power electronics and application. In addition, he holds two patents. His research interests include DC-DC converters,

implementation of the new wide bandgap semiconductors in power electronics, renewable energy conversion systems and converters for portable applications. Address: Chernihiv National University of Technology, Biomedical Radioelectronic Apparatus and Systems Department. Shevchenko Str. 95, 14035, Chernihiv, Ukraine.

E-mail: kostya.tytelmaier@gmail.com

ORCID iD: https://orcid.org/0000-0001-7582-0204



Roman Yershov received B. sc. and M. sc. diplomas in specialized computer systems at Chernihiv State Technological University, Chernihiv, Ukraine, in 2010 and 2012, respectively.

At present, he serves as a Senior Lecturer at the Department of Industrial Electronics at Chernihiv National University of Technology, Ukraine. He has prepared more than ten various applied and theoretical university courses. His scientific research interests include the digital control systems and precision position electric drive systems, an optimal FPGA-based implementation

of various algorithms and processing blocks. Address: Chernihiv National University of Technology, Biomedical Radioelectronic Apparatus and Systems Department. Shevchenko Str. 95, 14035, Chernihiv, Ukraine.

E-mail: roman.d.yershov@gmail.com

ORCID iD: https://orcid.org/0000-0002-0267-2906



Roman Kosenko received the Dipl. Eng. and M. sc. degrees in electronics from the Department of Industrial Electronics, Chernihiv State University of Technology, Chernihiv, Ukraine, in 2011 and 2013, respectively. He is currently working toward the Ph. D. degree at the Department of Electrical Engineering of Tallinn University of Technology and at the Biomedical Radioelectronic Apparatus and Systems Department of Chernihiv National University of Technology.

His fields of interest include research, design and simulation of switch mode converters for distributed power generation systems. He is author or co-author of over 20 scientific

papers and is the holder of one utility model.

Address: Department of Electrical Power Engineering and Mechatronics, Tallinn University of Technology, Ehitajate tee 5, 19086 Tallinn, Estonia.

E-mail: mr.roman.kosenko@ieee.org

ORCID iD: https://orcid.org/0000-0002-6214-3790



Dmitri Vinnikov (M'07–SM'11) received the Dipl. Eng., M. sc., and Dr. sc. techn. degrees in electrical engineering from Tallinn University of Technology, Tallinn, Estonia, in 1999, 2001, and 2005, respectively.

He is currently the Head of the Power Electronics Group, Department of Electrical Power Engineering and Mechatronics, Tallinn University of Technology (Estonia) and a Guest Researcher at the Institute of Industrial Electronics and Electrical Engineering, Riga Technical University (Latvia). He is the Head of R&D and a co-founder of Ubik Solutions LLC –

an Estonian start-up company dedicated to innovative and smart power electronics for renewable energy systems. Moreover, he is one of the founders and leading researchers of ZEBE – the Estonian Centre of Excellence for zero energy and resource-efficient smart buildings and districts. He has authored or co-authored two books, five monographs and one book chapter as well as more than 200 published papers on power converter design and development and is the holder of numerous patents and utility models in this field. His research interests include applied design of power electronic converters and control systems, renewable energy conversion systems (photovoltaic and wind), impedance-source power converters, and implementation of wide bandgap power semiconductors.

Address: Department of Electrical Power Engineering and Mechatronics, Tallinn University of Technology, Ehitajate tee 5, 19086 Tallinn, Estonia. E-mail: dmitri.vinnikov@ttu.ee

ORCID iD: https://orcid.org/0000-0001-6010-3464